HDMP-0552
Evaluation Board User's Guide

Application Note 1262

Evaluation Board Description
The Avago Technologies HDMP-0552K evaluation board is designed to demonstrate the full capabilities of the Avago Technologies HDMP-0552 Quad Port Bypass Circuit (PBC) with CDR (Clock and Data Recovery). The device contains four PBC cells within a single package.

The Avago Technologies HDMP-0552 device supports the ANSI X3T11 1.0625/2.125 Gbps FC-AL Loop Configuration.

The HDMP-0552 is packaged in a 10 x 10 mm, 64-pin Plastic Quad Flat Pack requiring a 3.3 V power supply.

This User's Guide for the Avago Technologies HDMP-0552K is intended for use in conjunction with the HDMP-0552 data sheet. The data sheet provides a detailed description of device operation, signal descriptions, and maximum ratings. The block diagram and pin definitions of the HDMP-0552 data sheet should be reviewed prior to testing.

Layout
The evaluation board is a six layer FR4 board, with the top and bottom layers used for signals while the middle layers are for the 3.3 V power supply (V_{CC} and V_{CC}HS) and GND. The layouts for top and bottom layers are included at the end of this User's Guide. (Refer to Figures 7 and 8.)

Table 1 summarizes the function of all connections and jumper options on the board. Typical setup is described in more detail under Functional Test. Table 2 lists the materials and components used in the assembly of the evaluation board.

A schematic of the evaluation board as well as the labeled pins of the HDMP-0552 are supplied within this User's Guide (Refer to Figure 6.)

A PLL capacitor of 0.1 μF is connected at pins 16 and 17 (CPLL1 and CPLL0) as close to the device as possible. Short leads reduce the chance of picking up noise from surrounding traces and components.

Port Bypass Pins
The HDMP-0552 PBC has five port bypass pins (BYPASS[0:4]) that are used as control bits implemented through jumpers on the evaluation board. When BYPASS [n]- = 1, then Disk x is in the loop and when BYPASS [n]- = 0, then Disk x is bypassed and not recognized as being in the loop. On the evaluation board, these pins are labeled as BYPASS[n] and float HIGH if the jumper is left open due to internal pull-up circuitry. The BYPASS[n] pin is set LOW if the corresponding jumper is set to GND.

Input/Output Lines
The input and output high-speed differential serial lines have 50 Ω controlled impedance lines of equal length to minimize skew.

The chip inputs and outputs are internally terminated with 150 Ω differential (75 Ω single ended). Inputs and outputs are required to be capacitively coupled. The chip will work in 75 Ω as well as 50 Ω impedence environment.

REFCLK
There are two different ways to drive the REFCLK input on the HDMP-0552. The jumper labeled H1 (Fig. 7) is used to select either an oscillator input applied through the SMA connector (labeled REF_CLK) or the on-board crystal oscillator.

When using the SMA connector, the PECL output clock from the Pattern Generator (1.0625 GHz or 2.125 GHz) can be divided by a circuit to get the desired REFCLK (106.25 MHz or 53.125 MHz) depending upon the REF_ RATE chosen.

If the REF_RATE pin is ground, then REF_CLK should be 53.125 MHz (From BERT 2.125 GHz rate use DIV/40 and 1.0625 GHz use DIV/20).

If the REF_RATE is chosen high, the REF_CLK should be 106.25 MHz (From BERT for 2.125 GHz use DIV/20 circuit and for 1.0625 GHz use DIV/10 circuit). The CDR select rate pin should be used accordingly. Refer to Table 1 for details.

Table 1. Control Pins for the Avago Technologies HDMP-0482 Evaluation Board

Signal	Typical Jumper Condition	Comments
BYPASS[n]-	Jumper to GND (Low) Open - High	High – Disk n is in the loop Low – Disk n is bypassed Note: There are five BYPASS pins: BYPASS [0:4]
REF_RATE	Open (High) Jumper to Gnd (Low)	High – REF_CLK set at 106.25 MHz. Low – REF_CLK set at 53.125 MHz.
MODE_VDD	Open (High) Jumper to Gnd (low)	High – Data Valid Check performed after CDR. FM_NODE[0] checked for data validity. Low – Data still being checked but may be from Input other than FM-NODE[0].
REF_CLK	H1 jumper to Crystal	REFCLK – Frequency is set though Oscillator SMA input from a clock generator. Use appropriate DIV BY circuit. Crystal Oscillator – Frequency is set by crystal oscillator that can be added to the through-hole footprint on the board for the CDR (106.25 MHz or 53.125 MHz).
CDR_SEL	Open (High) Jumper to Gnd	High – CDR is in the loop Low – CDR is bypassed
CDR_RATE	Open (High) Jumper to Gnd (low)	High – 2.125 GBd operation Low – 1.0625 GBd operation
EQ_SEL	Open (High) Jumper to Gnd (low)	Equalization is on all inputs Equalizaion is off in combination with ND(X) If EQ_SEL = 0 and ND(X)= 0. then equalization is off for port FM_NODE[X].
OUT_SEL	Open (High) Jumper to Gnd (Low)	Ouput can be turned on or off in combination with ND(X), i.e., if OUT_SEL = 0, NDX = 0, X output port TO_NODE[X]. is off.
FSEL	Open (High)	High – Errors in four consecutive 2^{15} bit intervals cause FM_NODE[0]_DV to go Low and no errors in four consecutive intervals cause it to go high. Low – Errors in a single 2^{15} interval cause FM_NOD[0]_DV to go low and no errors in the next interval cause it to go high.

The divide-by-10 circuit includes a PECL to TTL conversion. This 106.25 MHz clock can be applied directly to the REFCLK input. The schematic for this divide-by-10 circuit has been provided in this User's Guide. Refer to Figure 4.

The divide-by-20 circuit board is LVTTL output and can be connected to the REFCLK pin directly.

A footprint on the board is reserved for a crystal oscillator that should be either 53.125 MHz or 106.25 MHz. Both should have a ± 100 ppm tolerance.

Functional Test

A simple Bit Error Rate (BER) test of the HDMP-0552K evaluation board can be performed using the following equipment: HP 70004A display CRT, HP 70841B Pattern Generator, HP 70842B Error Detector (BERT), and HP 83480A Digital Communications Analyzer. The setup of the equipment is shown in Figure 1. Performance of the HDMP-0552K is verified by monitoring the eye diagram and evaluating the results from the BER test.

DC blocking capacitors and attenuators should be used to prevent equipment damage.

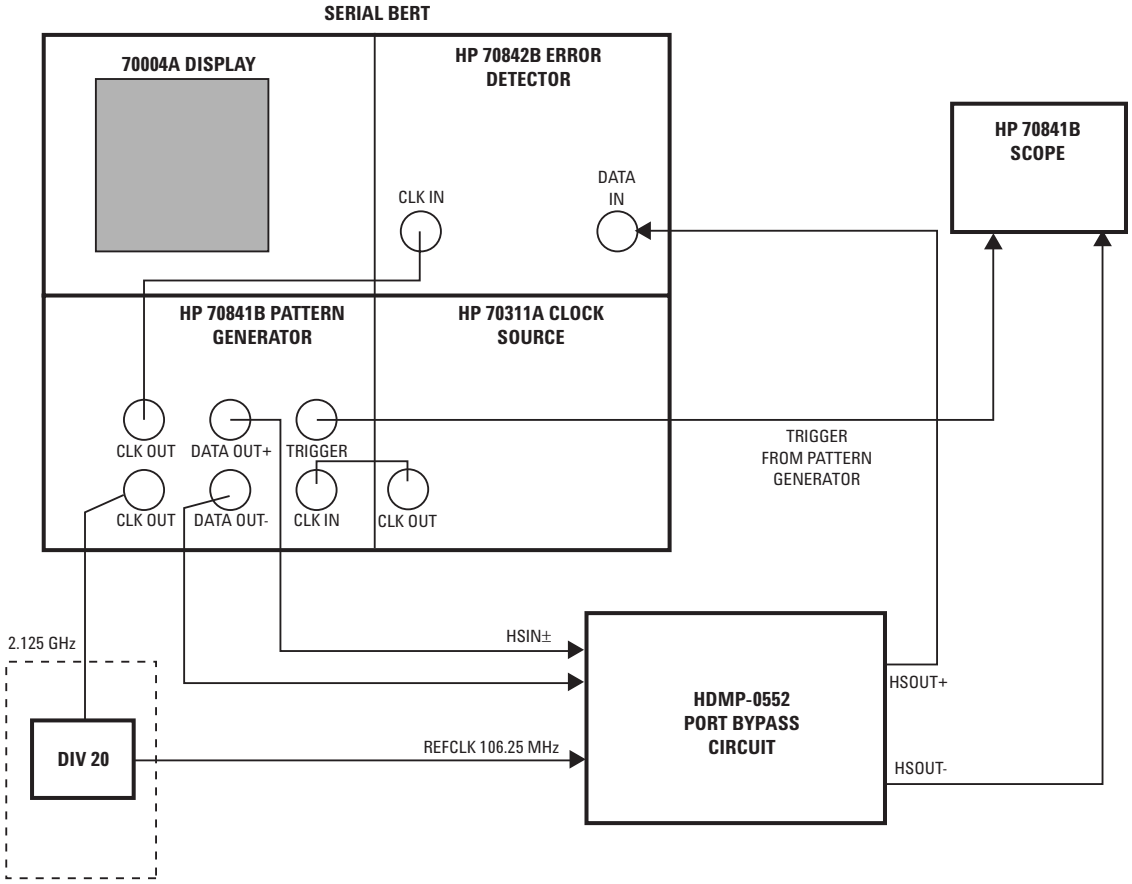

Figure 1. BER test setup using the Avago Technologies HDMP-0552 for 2.125 Gbaud

The HP 70841B Pattern Generator should be set to the PRBS pattern of 2^7-1. This is the closest instrument-supplied pattern to the 8B/10B code used in Gigabit Ethernet in terms of the longest run of zeros or ones. The output clock frequency should be set to 1.0625 GHz or 2.125 GHz for FC-AL evaluation and DIV BY clock ratio set accordingly. See Table 1 for reference.

The divide-by-20 circuit's TTL output (in case REF_RATE pin set high and 2.125 GHz data rate), is used to drive REFCLK on the evaluation board at a frequency of 106.25 MHz. The divide-by-10 circuit's TTL output (in case REF_RATE pin set high and 1.0625 GHz data rate), is used to drive REFCLK on the evaluation board at a frequency of 106.25 MHz. This provides a reference oscillator for frequency acquisition of the CDR in the HDMP-0552. If the REF_RATE pin is tied to ground, then use the 53.125 MHz clock and DIV BY circuit appropriately. It is important to verify that jumper H1 is connected to the REFCLK SMA when using an external clock.

To prevent damage to the scope, the TTL signal is DC blocked and attenuated by 20 dB before applying to the TRIGGER input. The external scale on the scope for TRIGGER should be adjusted to the same ratio of 10:1 or 20 db.

The CDR position can be altered with respect to the inputs and outputs of the hard disks. The HDMP-0552 data sheet shows the pin connection diagram for desired CDR locations.

For evaluation purposes, the CDR is typically placed at the beginning or the end of the loop. This would correspond to differential data out of the 70841B into the evaluation board SMA inputs FM_0± nodes for the beginning of the loop and FM_1± nodes for the end of the loop.

The differential outputs from the 70841B Pattern Generator (Data Out ±) should be sent into the desired port on the evaluation board. FM_0± or FM_1± are typically used for evaluation purposes making either BYPASS[0] floating High or BYPASS[1] floating High with all other BYPASS jumpers connected to GND.

The output of the evaluation board can be viewed on the HP 83480A Digital Communications Analyzer to see the eye diagram.

Table 2. Bill of Material

Capacitors

Quantity	Description		
2	0.01 µF	ceramic 603	
67	0.1 µF	ceramic 603	
2	1 µF	tantalum 603	
2	100 µF	electrolytic	
Placements:	C58	1 µF	tantalum
	C59	1 µF	tantalum
	C60	0.01 µF	ceramic
	C61	0.01 µF	ceramic
	BC	100 µF	electrolytic
	BC1	100 µF	electrolytic
	All other capacitors are 0.1 µF		

Resistors:

Quantity	Description		
1	10 kΩ	5% 603	**(OPTIONAL) (Don't Stuff)**
1	0.0 Ω	5% 603	
Placements:	R1	2 Ω	
	R10	10 kΩ	**(OPTIONAL) (Don't Stuff)**

Components:

Quantity	Description		
1	FOX	F1100H Crystal 53.125 MHz	**(OPTIONAL)**
Placements:			
XTALW/S	FOX	F1100H	**(OPTIONAL)**

SMAs

Quantity	Description
24	Must Stuff
10	**(OPTIONAL) (Don't Stuff these!)**
	T1_IN
	T1_OUT
	T2_IN+
	T2_IN-
	T2_OUT+
	T2_OUT-
	T3_IN+
	T3_IN-
	T3_OUT+
	T3_OUT-

Miscellaneous

Quantity	Description	
3	Headers 10x2 (J12, J13, J14)	
1	Headers 1x2 (H1)	**(OPTIONAL)**
1	Power Connector	
2	Test Points	
	C22 - Pin 1 or DUT Pin 16, C22 - Pin 2 or DUT Pin 17	

Notes:

1) Disregard: R2, R3, R4, R5, R6, R7 & R9

The HDMP-0552 outputs can be viewed from any port but for evaluation purposes it is easiest to use either TO_1- node or TO_0- node as outputs into the Digital Communications Analyzer. A 20 dB attenuator should be added to the input to the 83480A for protection and the external scale of the scope should be adjusted to a ratio of 10:1 or 20 dB.

If the CDR is connected at the beginning of the loop (Input = FM_0±), then TO_0- node should be used as the output to the scope. If the CDR is connected at the end of the loop (Input = FM_1±), then TO_1- node should be used as the output to the scope. This setup allows the data to go all the way through the device (each mux) for full verification.

If FM_0± nodes are used as the inputs from the BERT then BYPASS[0] should be left floating with the other BYPASS pins, BYPASS[1:4], shorted to GND via the jumper. If FM_1± nodes are used as the inputs from the BERT then BYPASS[1] should be left floating with the other BYPASS pins – BYPASS[0], BYPASS[2,3,4] – shorted to GND via the jumper.

The TO_0+ node or TO_1+ node outputs from the HDMP-0552 should be connected to DATA IN on the HP 70842B Error Detector depending on whether FM_0 or FM_1 were used for inputs. A 20 dB attenuator should be added to the input to the HP 70842B for protection.

It is recommended to view signals on the HP 83480A Digital Communications Analyzer before and after the CDR function to gain a better understanding of its effects and see how it affects the eye diagram.

Figures 2 and 3 show a typical eye diagram using the setup described for single-ended signals. In this case, the BER test was carried out for more than two hours with no errors, representing a BER better than 1.112×10^{-13}. A BER better than 1.0×10^{-14} is expected with this lab setup.

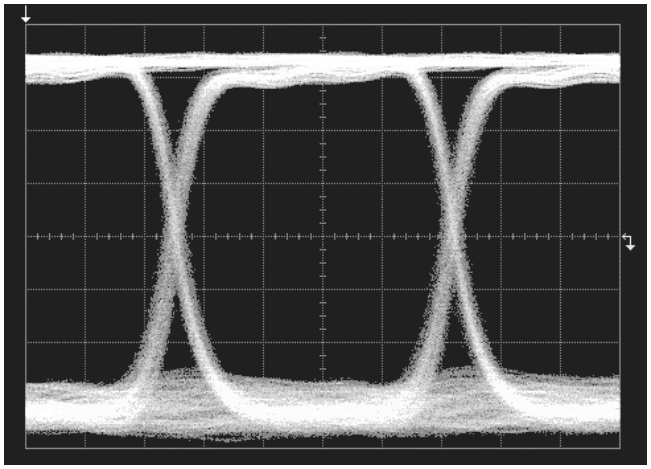

Figure 2. Eye diagram of the high-speed serial single-ended outputs from the HDMP-0552 as captured on the HP 83480A Digital Communications Analyzer for 2.125 Gbaud rate

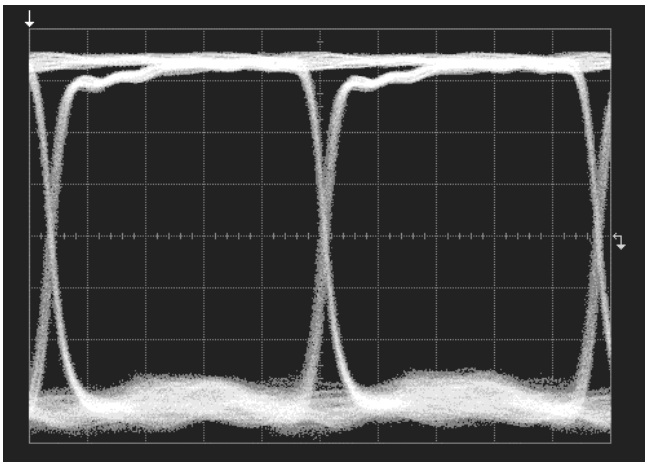

Figure 3. Eye diagram of the high-speed serial single-ended outputs from the HDMP-0552 as captured on the HP 83480A Digital Communications Analyzer for 1.0625 Gbaud rate

To view differential signals, the two signals (TO[n]±) should be sent into a Digital Communications Analyzer as two separate channels on two identical and equal length cables. If the cables are not equal length or physically different cables, the signals will not be in phase and will cancel out each other, closing the eye and increasing errors.

The Math function menu of the oscilloscope will provide the option of subtracting two waveforms from each other. The Digital Communications Analyzer subtracts the differential pair TO_[n]± and provides a new waveform with a larger amplitude since the signals are completely out of phase. Eye diagrams can be viewed in this format as well.

Filtering

Please note that each V_{CC} pin in the Schematic and Gerber file shows five 0.1 µF capacitors for filtering the noise. Avago Technologies evaluated the option of putting one 0.1 µF capacitor at each V_{CC} pin (with the exception of two 0.1 µF capacitors at V_{CCA} pin #8). Evaluation showed that the board will perform well with fewer number of capacitors.

Note:
This evaluation board is intended for evaluation purposes only. Avago Technologies does not guarantee its performance in a production environment.

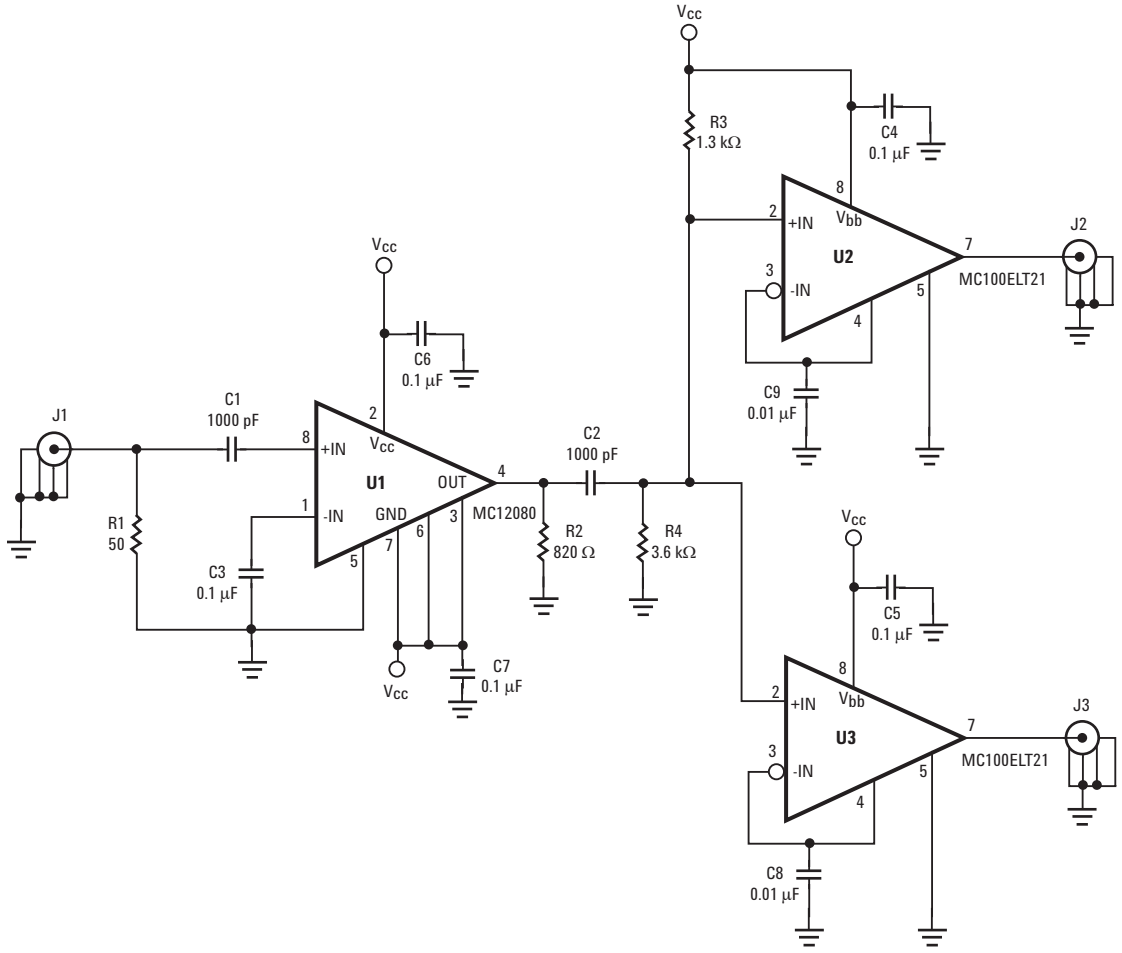

Figure 4. Divide by 10 network used with the BER Test. To get DIV/20, i.e., 2.125 MHz /20 = 106.25 MHz, DIV/2 and DIV/10 boards can be used.

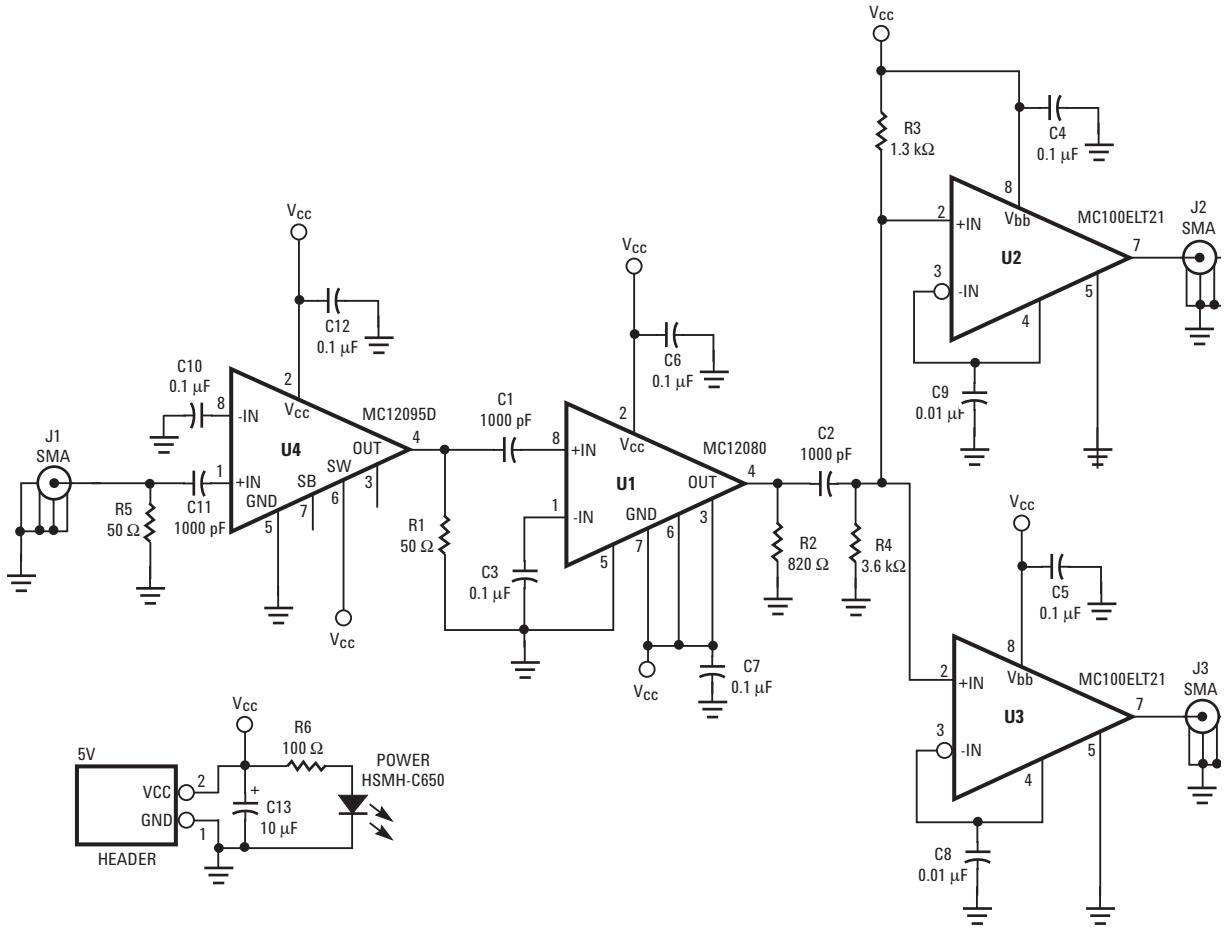

Figure 5. Divide by 20 network used with the BERT Test

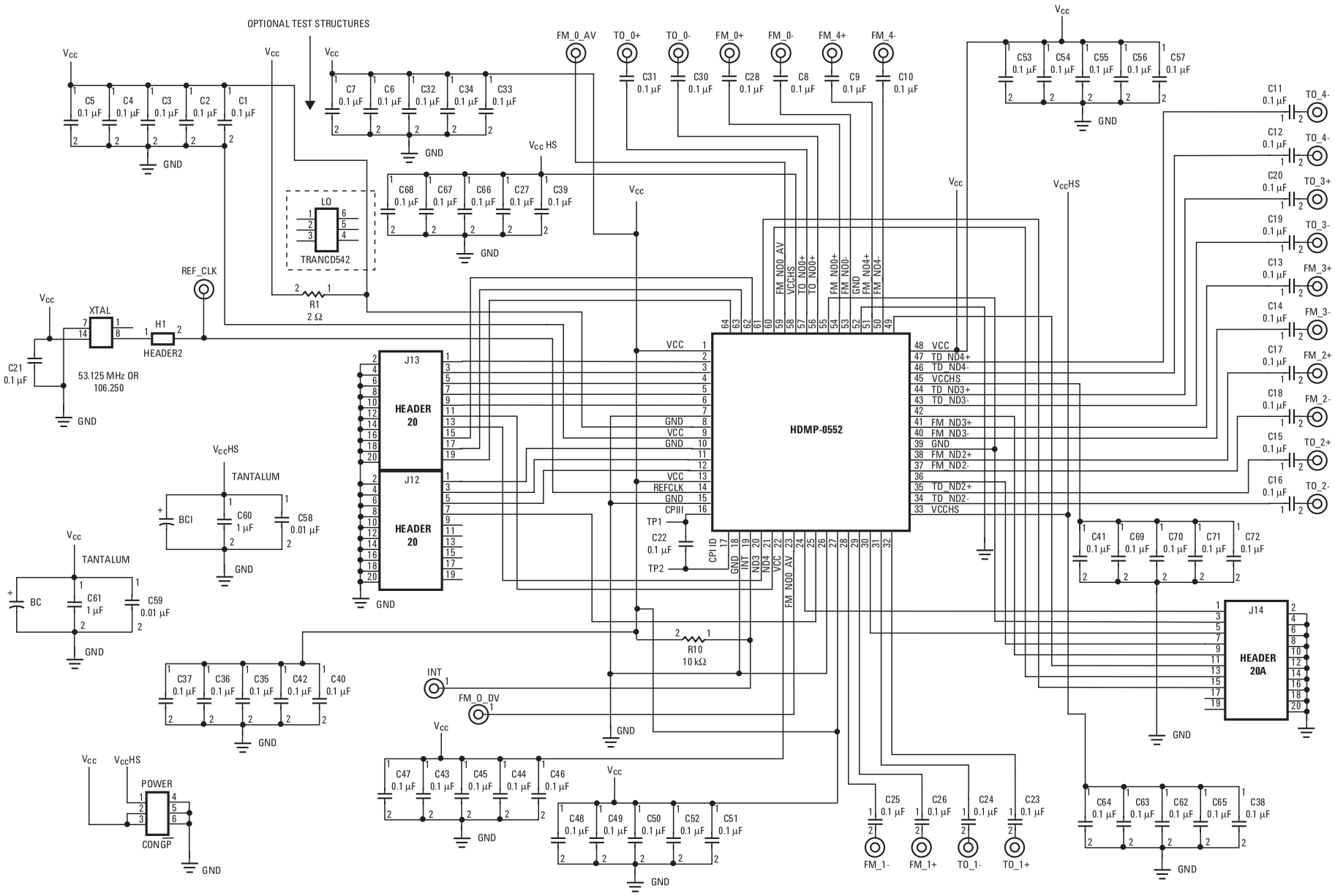

Figure 6. Circuit schematic for the evaluation board

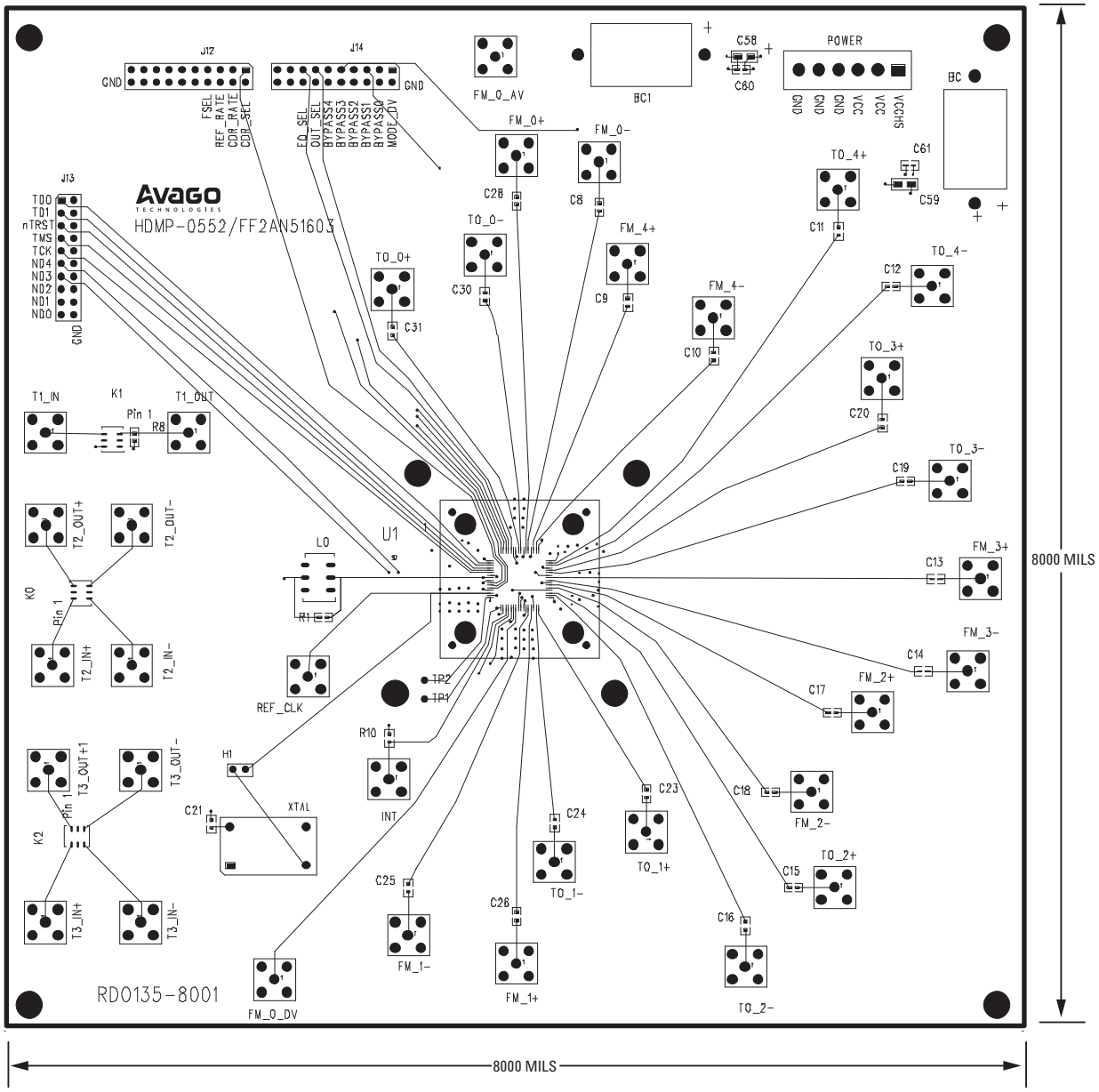

Figure 7. Top view of evaluation board

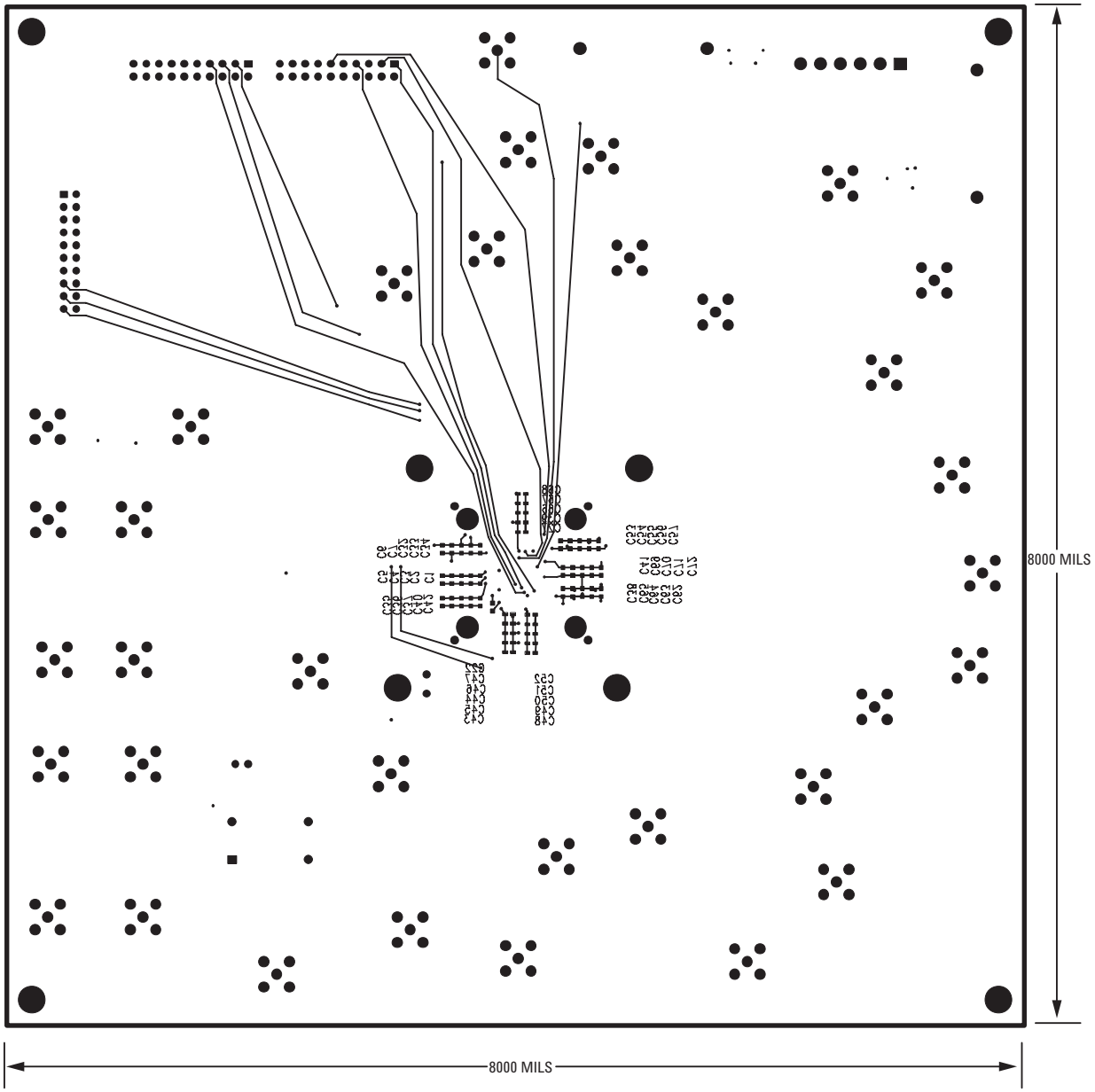

Figure 8. Bottom side of evaluation board

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