Cost Effective 820nm LED Transmitter Driver for DC-50MBd Application for 3.3V Power Supply Voltage

Application Note 5598

Introduction

Avago Technologies manufactures fiber optic components for industrial, medical, transportation, power generation and gaming markets. Its products have been adopted in various applications for years since it started producing fiber optic components. Avago Technologies offers both discrete and integrated fiber optic components that can be easily designed into customer systems. Integrated transmitters incorporate the driving circuit with the product, while discrete transmitters require customers to design the transmitter driving circuit.

The advantage of using discrete components is the flexibility in designing optical link solutions that are optimized for the target customer application.

Objective

Avago Technologies supports its customers to implement cost effective components to interface with our products. This application note (AN) discusses the logic device " 74LCX00" by "Fairchild Semiconductor" for creating LED driver circuit operating at 3.3V. This gives customers more flexibility and lesser component count in choosing the most suitable product in their application.

New Driver for 3.3 V Operations

The 74LCX00 at V_{CC}=3.3 V shows comparable performance to the 74ACTQ00 at V_{CC}=5.0 V. For best performance and optimum matching with Avago´s optical parts the "74LCX00" logic IC is discussed in this application note and shows details about LED driver circuits for Avago´s discrete fiber optic transmitters of the Miniature Link Product Family "HFBR-14xxxZ", with bare AlGaAs light emitting diode (LED) at 820 nm.

The shown LED driver circuits are recommended to create optical links with Avago Miniature Link Fiber Optic Receivers at supply voltage levels of 3.3 V, like "AFBR-24x8xZ" and "AFBR-24x9xZ".

NOTE All data shown in this AN are based on tests with one driver chip "74LCX00" from manufacturer "Fairchild Semiconductor" and three transmitter samples of the Miniature Link Product Family "HFBR-14xxxZ".

Test data shown in this AN reflect the typical behavior of the tested optic transmitters in combination with the specific driver chip.

Low Voltage Quad 2-Input NAND Gate "74LCX00"

The IC by Fairchild Semiconductor provides four low voltage 2-input NAND gates with 5 V tolerant inputs and is fabricated with advanced CMOS technology to achieve high speed operations. At a supply voltage of 3.3 V, the used NAND Gate "74LCX00" is compatible to electrical (LV)TTL input levels. The recommended current load per output is up to ±24 mA for 3.3 V operation. In the following discussed circuits, one of the four gates is used as common input to drive the other three gates, which provide the LED driver current in parallel.

Therefore the current load on the three parallel gates should not exceed 72 mA (3 × 24 mA), which corresponds to the LED driver current.

Due to the used CMOS technology the output voltage levels of the NAND gates at electrical output state "LOW" are above GND level. For simplification this specific voltage drop is called "V_{gate}".

The used "74LCX00" IC shows following Vgate characteristic at T_A=25 °C in combination with fiber optic transmitters with bare LED of the Miniature Link Family "HFBR-14xxxZ" for 3.3 V operation:

Equation 1

$$Vgate = (0.0023(V/mA) \times I_{LED\ peak}\ (mA)) + 0.016V$$

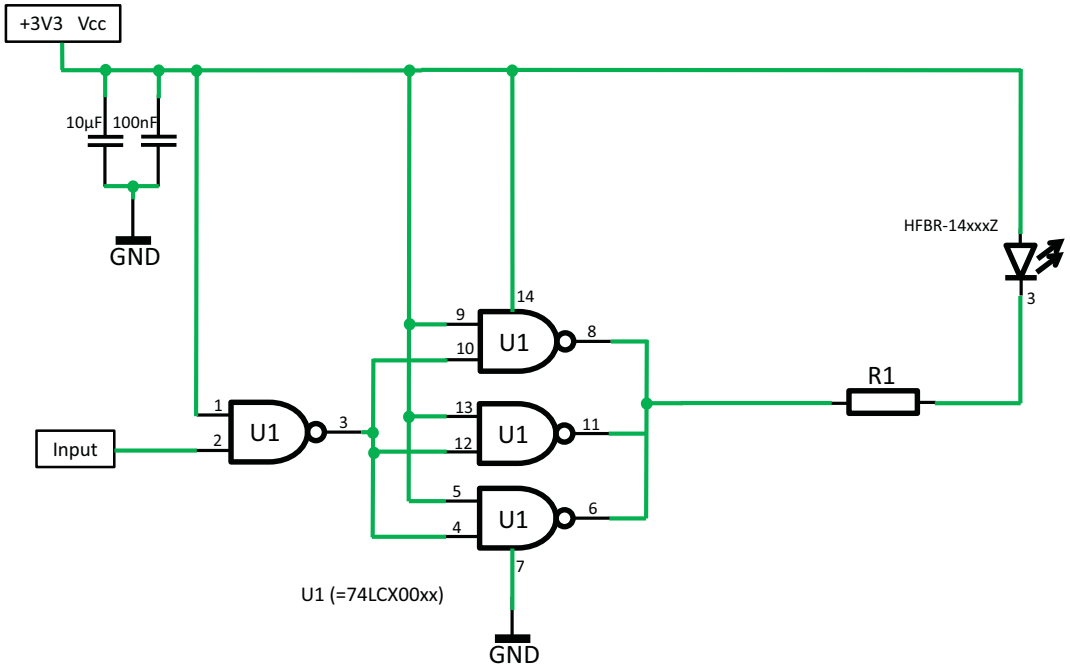
The preceding formula is based on test data of one single IC. For more details about the typical IC performance, please contact the manufacturer of the IC you actually wish to use for your application.

Because of the low supply voltage of 3.3 V already relative small voltage differences have a measurable influence to the typical driver circuit behavior. Therefore the individual gate voltage ("V_{gate}") of the used driver IC and the individual forward voltage ("V_f") of the LED at the specific driver current should be used for the calculations mentioned on the next pages.

NOTE The following information is only valid when using discrete fiber optic transmitters of the Avago Miniature Link Family "HFBR-14xxxZ" with bare LED in combination with the NAND Gate "74LCX00". This AN should be seen as guidance for creating LED driver circuits to support the individual needs of customer´s specific applications.

Driver Circuit for HFBR-14xxxZ (820 nm LED Discrete Fiber Optic Transmitter) Optimized for Low Current Consumption

Figure 1 Driver Circuit for HFBR-14xxxZ at V_{cc}=3.3 V



The shown driver circuit (Figure 1) has inverse logic, which means an electrical Input level of "HIGH" will result in LED "OFF", and vice versa. Supply line capacitances (10 µF and 100 nF) have a noise filter effect and are recommended. Typically, the optical fall time of the LED is shorter than the optical rise time, this is related to the inner LED structure and the driver circuit. This unbalanced switching times of the LED may lead to duty cycle distortion (DCD), which limits the maximum data rate of this circuit.

The benefit of this driver circuit is the very low current consumption when the LED is OFF (when electrical input level is "HIGH"), which is typically below 1 mA, independent of the selected LED driver current.

In this circuit, no switching behavior optimization components are installed, therefore the optical switching times could vary from LED to LED and the switching behavior becomes slower when low LED driver currents are selected.

With a driver current of around 60 mA (peak) the typical optical rise and fall times of the discrete fiber optic transmitters should be around 5ns over the entire temperature range from –40 °C to +85 °C, which generally allows data rates up to 50 MBd. The maximum data rate also depends on the individual link requirements and communication standards that need to be fulfilled, therefore an individual check of the optical output signal quality of the used optic transmitter is recommended during the circuit design.

The driver current (peak value) at T_A=25 °C can be calculated by following formula:

Equation 2

$$I_{LED\ peak}\ (mA) = (V_{cc}\ (V) - (V_f\ (V) + V_{gate}\ (V))) / (R1\ (\Omega) \times 0.001)$$

Equation 3

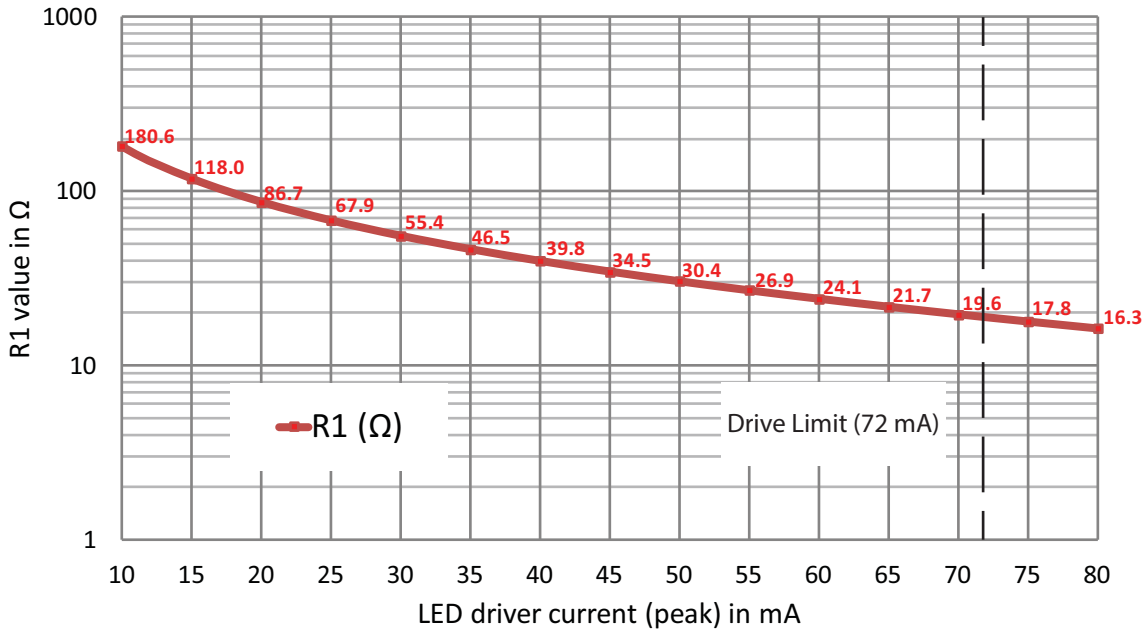
$$R1\ (\Omega) = (V_{cc}\ (V) - (V_f\ (V) + V_{gate}\ (V))) / (I_{LED\ peak}\ (mA) \times 0.001)$$

NOTE The recommended DC load of this IC in combination with the shown driver circuits is max. 72 mA.

Where "V_{cc}" is the supply voltage, "R1" is the current limiting resistor value, "V_f" is the forward voltage of the used LED at target driver current and "V_{gate}" is the voltage drop across the IC outputs at target driver current, when they are low. As more accurate the resistor value (tolerance class) as better the accordance between theoretical calculated and actual LED driver current in the application.

The following diagram (Figure 2) can be used to select the resistor value R1 for individual peak driver currents at T_A = 25 °C for the driver circuit shown in Figure 1. The diagram is based on the previous formula, therefore it is only valid for operation at V_{cc} = 3.3 V and only if HFBR-14xxxZ (bare LED) transmitters are used.

Figure 2 Resistor Value Selection "R1" for Driver Circuit Shown in Figure 1



NOTE In Figure 2, the recommended DC load of this IC in combination with the shown driver circuits is max. 72mA!

For example, if a peak LED driver current of about 60 mA is needed, following calculations are required to ensure the correct R1 component value for the mentioned LED driver circuit (Figure 1).

The forward voltage "V_f" of HFBR-14xxxZ can be found in the corresponding product data sheet; at 60 mA driver current, it is 1.70 V (typ.). The gate voltage of the used IC is around 0.154 V for 60 mA load at 3.3 V operation, based on the formula mentioned previously. Therefore a R1 value of 24.1 Ω at V_{cc}=3.3 V will realize the needed LED driver current of around 60 mA (peak). If the calculated resistor value is not available or not desired the next closer resistor value should be chosen, but then a recalculation of the LED driver current is needed.

For example, if a 25 Ω resistor for R1 is preferred the corresponding LED driver current would be slightly reduced to around 58 mA (peak).

Equation 4

$$I_{LED\ peak}\ (mA) = (V_{cc}\ (V) - (Vf\ (V) + V_{gate}\ (V))) / (R1\ (\Omega) \times 0.001) = (3.3\ V - (1.7\ V + 0.15\ V)) / (25\ \Omega \times 0.001) = 58\ mA$$

The following eye diagrams are of the opto-electrical converted transmitter signal of "HFBR-1414Z" installed in the driver circuit (Figure 1) with components for 58 mA LED peak current.

V_{cc} = 3.3V; electrical input pattern: PRBS2^15-1 at 50 MBd
Component installed: R1 = 25 Ω

Figure 3 T_A = 85 °C (t_r = 5.0 ns (typ.); t_f = 2.8 ns (typ.); Horizontal = 5 ns/div)

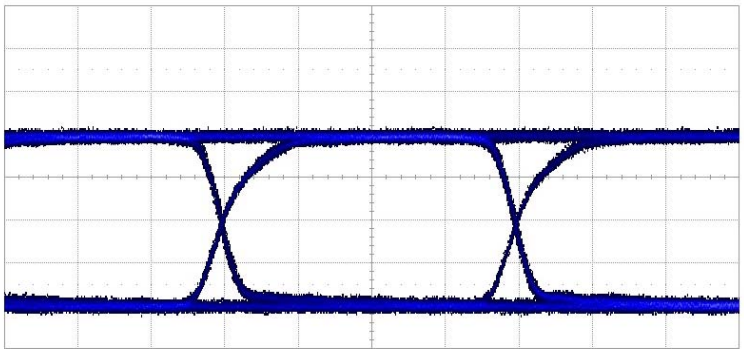


Figure 4 T_A = 25 °C (t_r = 4.9ns (typ.); t_f = 2.7ns (typ.); Horizontal = 5 ns/div)

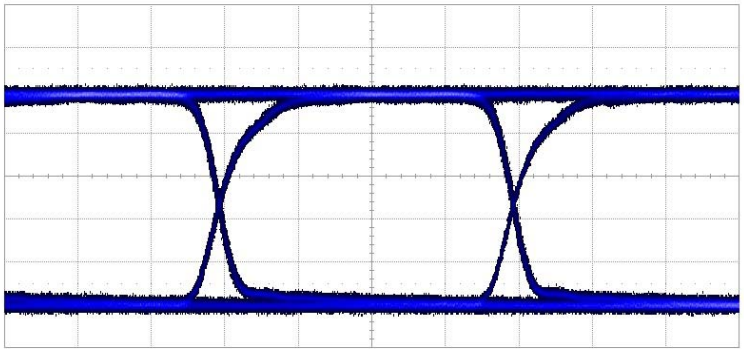
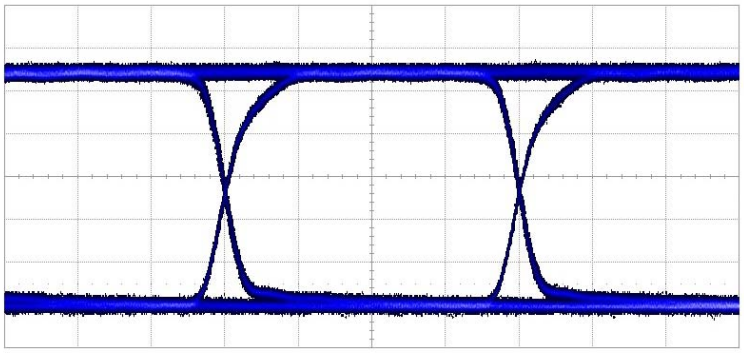
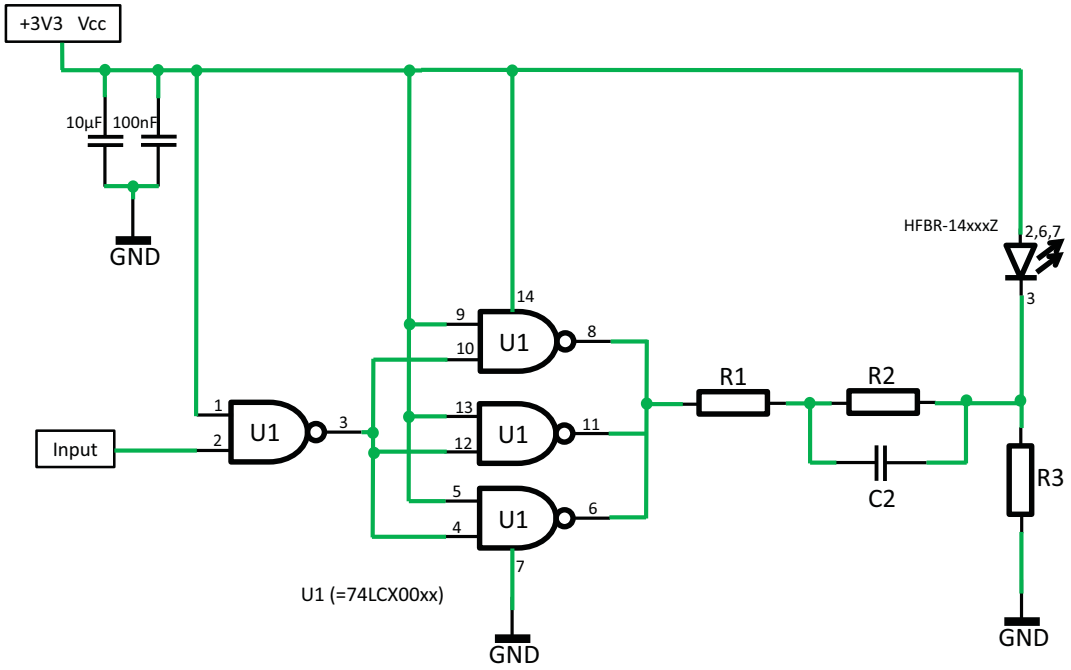


Figure 5 T_A = –40 °C (t_r = 4.2 ns (typ.); t_f = 2.7 ns (typ.); Horizontal = 5 ns/div)



Driver Circuit for HFBR-14xxxZ (820 nm LED Discrete Fiber Optic Transmitter) for Data Rates up to 50 MBd

Figure 6 Recommended Driver Circuit for Data Rates up to 50MBd at V_{cc}=3.3V



Three more components are added to the circuit shown in Figure 1 to enhance the switching performance of the LED to enable operation at higher data rates. This circuit shows inverse logic, same as for the previous circuit: at electrical input signal "HIGH" the LED is OFF and vice versa.

Supply line capacitances (10 µF and 100 nF) have a noise filter effect and are recommended.

R2 and C2 realize a current peaking of the LED forward currents which increases the optical rise times (t_r) of the LED. R3 enables a quiescent current, which hold the LED on a specific voltage level, when the LED is OFF. This helps to decrease the optical fall times (t_f) of the LED. Careful selection of R2, C2, and R3 allows aligning of the optical rise and fall times to similar values, which helps to reduce the negative effect of duty cycle distortion (DCD) and enables higher data rates up to 50 MBd. The typical performance of the driver circuit (Figure 6) enables even higher maximum data rates. With a driver current of around 60 mA (peak) the typical optical rise and fall times of the discrete fiber optic transmitters should be around 3.5 ns over the entire temperature range from –40 °C to +85 °C, which generally allows data rates up to 100 MBd.

The maximum data rate also depends on the individual link requirements and communication standards that need to be fulfilled, therefore an individual check of the optical output signal quality of the used optic transmitter is recommended during the circuit design.

For highest driver performance and reliability the LED peak current should be above 20 mA, but below the recommended maximum current load of 72 mA for the three used NAND-Gates.

The driver current (peak value) at T_A=25 °C can be calculated by following formula.

Equation 5

$$I_{LED\ peak}\ (mA) = (V_{cc}\ (V) - (V_f\ (V) + V_{gate}\ (V))) / (R\_result\ (\Omega) \times 0.001)$$

Equation 6

$$R\_result\ (\Omega) = (V_{cc}\ (V) - (V_f\ (V) + V_{gate}\ (V))) / (I_{LED\ peak}\ (mA) \times 0.001)$$

Where "V_{cc}" is the supply voltage, "R_result" is the effective current limiting resistor value for condition LED = ON, "V_f" is the forward voltage of the LED at target driver current and "V_{gate}" is the gate voltage drop across the IC outputs at target driver current, when they are low. More information can be found on the next pages.

Optimization rules for fast optical switching times when using 74LCX00 and Avago´s discrete fiber optic transmitters of the Miniature Link Product Family "HFBR-14xxxZ".

Equation 7

$$R1 = R\_result \times 0.6;$$

$$R3 = 10 \times R1;$$

$$R1 = R2\ ;$$

$$C2\ (\text{pF}) = (3\ (pF/mA)) \times (I_{LED\ peak}\ (mA))$$

NOTE Using a higher capacitance value for "C2" will result in higher current peaking effect that creates faster LED rise times, but also higher optical overshoot. If the circuit is to be used for data rates below 10 MBd, the C2 value can be reduced. The LED capacitance, the individual capacitance of the PCB layout and the tolerances of the used board components influence the actual switching capacity and the peaking effect. *Therefore an individual check of the optical output signal quality is recommended during the circuit design*.

For example, if a LED driver current of 58 mA (peak) at T_A=25 °C is required, following calculations are needed to ensure the correct component values for the mentioned LED driver circuit (Figure 6).

The forward voltage "V_f" of HFBR-14xxxZ can be found in the corresponding product data sheet; at 58 mA driver current it is typ. 1.70 V.The gate voltage of the NAND Gate is around 0.15 V for 58 mA load at 3.3 V operation, based on the formula mentioned previously. The effective current limiting resistance "R_result" at driver condition LED=ON, can be calculated as follows.

Equation 8

$$\text{R\_result}(\Omega) = (V_{cc}\ (\text{V}) - (V_f\ (\text{V}) + V_{gate}\ (\text{V}))) / (I_{\text{LED peak}}\ (\text{mA}) \times 0.001) = (3.\ 3\text{V} \times (1.70\ \text{V} + 0.15\ \text{V})) / (58\ \text{mA} \times 0.001) = 25\Omega$$

By using the optimization rules for this circuit, following component values can be calculated.

Equation 9

$$R1 = \text{R\_result}\ (\Omega) \times 0.6 = 15\Omega;$$

$$R2 = R1 = 15\Omega;$$

$$R3 = 10 \times R1 = 150\Omega;$$

$$C2\ (\text{pF}) = 3\ (\text{pF/mA}) \times 58\ (\text{mA}) = 174\ \text{pF}$$

More Details about the Recommended Driver Circuit (Figure 6)

Capacitance "C2" builds the peaking component, which helps to decrease the optical rise time of the LED. To reach comparable LED rise and fall times a specific level of optical overshoot is required, therefore value C2 should not be chosen too low. By using the recommended value for C2 a sufficient high overshoot level for 3.3V operation should be provided for most applications. If the recommended C2 value is not available the closer one should be selected. Please note that higher C2 values will result in higher optical overshoot.

LED "ON":

An electrical driver input "LOW" results in electrical output state "LOW" of the three IC gates, due to the NAND logic of the used IC (see Figure 7). R1 and R2 are in parallel to R3 and reduce the effective resistance (R_result) in the LED current path by a fixed value-ratio of "10" between resistors R1/R2 and resistor R3 (see the optimization rules).

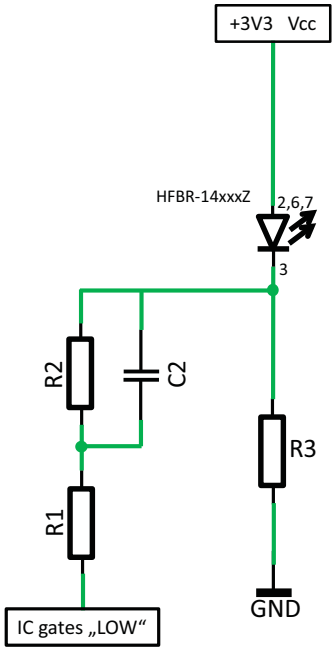
For calculation of the LED peak driver current (= LED "ON") at T_A = 25 °C following formula can be used:

Equation 10

$$R\_result(\Omega)=((R1\ (\Omega)\ +\ R2\ (\Omega))\times R3(\Omega))\ /\ (R1\ (\Omega)\ +\ R2\ (\Omega)\ +\ R3\ (\Omega))\ ;$$

$$I_{LED\ peak}\ (mA)\ =(V_{cc}\ (V)-(V_f\ (V)+V_{gate}\ (V)))\ /\ (R\_result\ (\Omega)\times 0.001)$$

Figure 7 Circuit Illustration at IC Outputs Electrical "LOW"



LED "OFF":

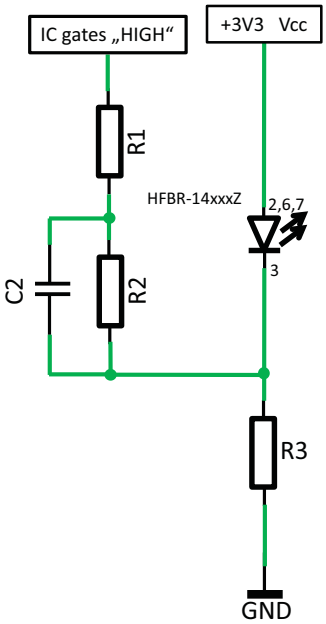
An electrical driver input "HIGH" results in electrical output state "HIGH" of the three IC gates due to the NAND logic of the used IC (see Figure 8).

NOTE If the applied voltage drop over a LED is forced below the individual forward voltage of this LED the discrete optic transmitter will not emit light.

Resistors R1 and R2 build a voltage divider with resistor R3. Because R1 and R2 are in parallel to the LED, the resistors force a fix voltage drop over the LED.

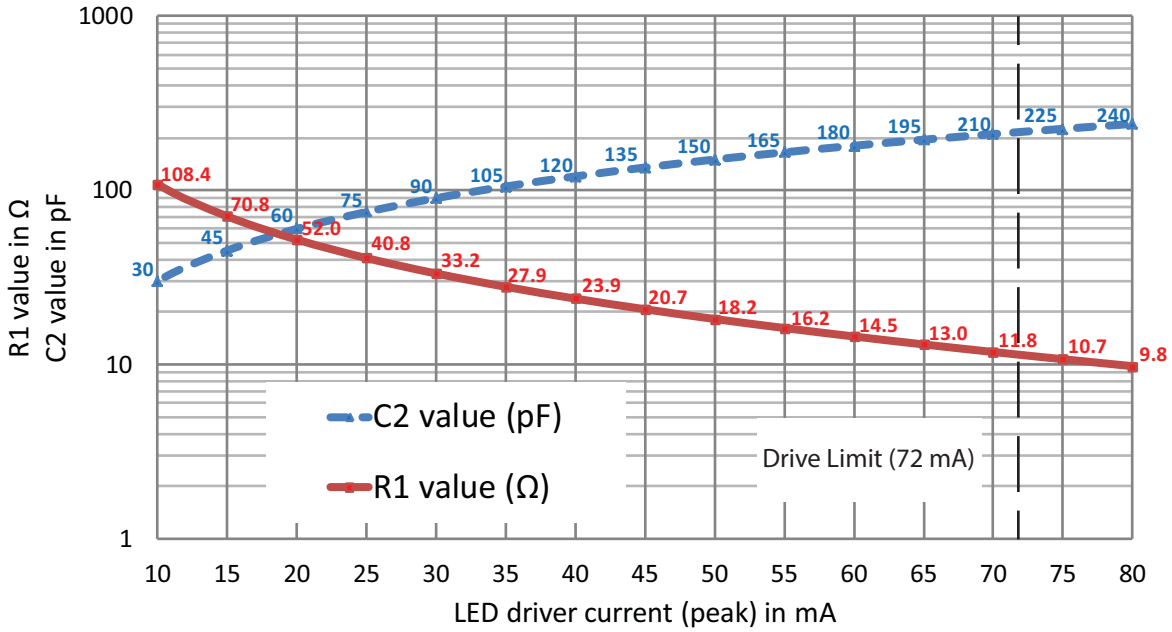
This LED voltage drop is clear below the typical forward voltage of the discrete 820 nm LED transmitter of the product family "HFBR-14xxxZ", this guarantees that the LED switch OFF completely when the electrical driver input signal is "HIGH". A fixed value-ratio of "10" between resistors R1/ R2 and resistor R3 (please see optimization rules) build a sufficient low voltage drop, but not equal to GND, which implements a specific quiescent voltage level over the LED even when the LED is OFF. This helps to decrease the switching times of LED´s falling edges, this effect is often called "clamping". Therefore faster fall times result in the need of a quiescent current generated by the voltage divider, so this driver circuit consumes current even when the LED is OFF.

Figure 8 Circuit Illustration at IC Outputs Electrical "HIGH"



The following diagram (Figure 9) can be used to find the resistor value R1 and capacitor value C2 for individual peak driver currents at T_A=25 °C based on the driver circuit (Figure 6). The diagram is generated by using the mentioned optimization rules, therefore it is only valid for operation at V_{CC} = 3.3 V and only if HFBR-14xxxZ (bare LED) transmitters are used.

Figure 9 Component Value Selection for Driver Circuit Shown in Figure 6



NOTE In Figure 9, the recommended DC load of this IC in combination with the shown driver circuits is max. 72mA!

The following tables show average test data of three "HFBR-14xxxZ" optic transmitters, placed in driver circuit (Figure 6) with components for adjusted LED peak current of 58 mADC at V_{CC} = 3.3 V. The tables reflect the typical behavior of the tested three samples within this specific test circuit and are not general valid. Individual performance tests are recommended.

Components installed: R1=R2=15 Ω; R3=150 Ω; C2=180 pF.

Table 1 T_A=85 °C at 50MBd PRBS 2^15-1 (Typical Values)

V_{CC} (V)	DCD (ns)	Optical t_r (ns)	Optical t_f (ns)	Optical Overshoot (%)	I_{CC} at Light OFF (mA)	I_{CC} at Light ON (mA)
3.0	1.5	3.7	3.1	8.3	16.1	49.1
3.3	1.3	3.6	3.2	7.2	17.8	58.5
3.6	1.2	3.5	3.3	6.5	19.4	68.0

Table 2 T_A = 25 °C at 50MBd PRBS 2^15-1 (Typical Values)

V_{CC} (V)	DCD (ns)	Optical t_r (ns)	Optical t_f (ns)	Optical Overshoot (%)	I_{CC} at Light OFF (mA)	I_{CC} at Light ON (mA)
3.0	1.3	3.2	3.0	9.6	16.1	49.3
3.3	1.2	3.2	3.2	9.3	17.6	59.0
3.6	1.1	3.2	3.2	8.2	19.2	68.7

Table 3 T_A = –40 °C at 50MBd PRBS 2^15-1 (Typical Values)

V_{cc} (V)	DCD (ns)	Optical t_r (ns)	Optical t_f (ns)	Optical Overshoot (%)	I_{cc} at Light OFF (mA)	I_{cc} at Light ON (mA)
3.0	1.1	2.5	3.0	15.6	16.4	49.7
3.3	1.1	2.5	3.1	14.5	18.0	59.8
3.6	1.0	2.5	3.2	12.9	19.7	69.9

Where "V_{cc}" is the supply voltage and "I_{cc}" is the current consumption of the driver circuit under operation. The duty cycle distortion (DCD), the optical rise time (t_r) and optical fall time (t_f) of the discrete transmitters and the optical overshoot can be also found in the tables.

When the LED is ON parallel loads are typically negligible small, therefore parameter "I_{cc} at Light ON" reflects the LED driver current very close.

The tables show, that the driver circuit (Figure 6) provides very constant and stable LED driver currents over temperature. Also the quiescent current (when LED is OFF) is stable over temperature. The peaking effect decreases with temperature, so at low temperatures the peaking effect will be higher.

Variation in the supply voltage level "V_{cc}" of the driver circuit has significant influence to the LED driver current level. V_{cc} fluctuations of around ±9.1% (3.3 V ± 0.3 V) result in typically around ±16.5% variation of the LED driver current. The reduction of optical output power over temperature is related to the LED characteristics itself and is already included in the Avago "HFBR-14xxxZ" data sheet specifications; the influence of the driver circuit regarding driver current stability over temperature is negligible small for most applications.

The following eye diagrams are of the opto-electrical converted transmitter signal of "HFBR-1414Z" installed in the recommended driver circuit (Figure 6) with components for 58 mA LED peak current.

V_{cc} = 3.3 V; electrical input pattern: PRBS2^15-1 at 50 MBd;
Components installed: R1=R2=15 Ω; R3=150 Ω; C2=180 pF

Figure 10 T_A = 85 °C (t_r = 3.3 ns (typ.); t_f = 3.0 ns (typ.); Optical Overshoot = 7.1% (typ.); Horizontal = 5 ns/div)

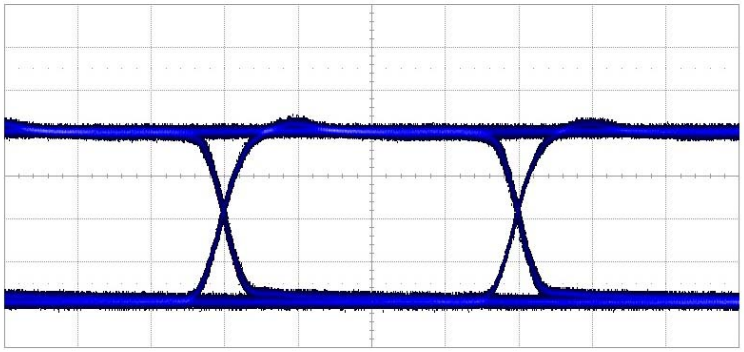


Figure 11 T_A = 25 °C (t_r = 3.2 ns (typ.); t_f = 3.0 ns (typ.); Optical Overshoot = 9,1% (typ.); Horizontal = 5 ns/div)

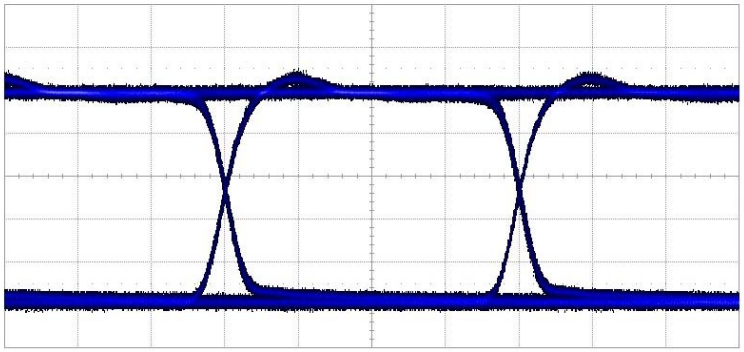
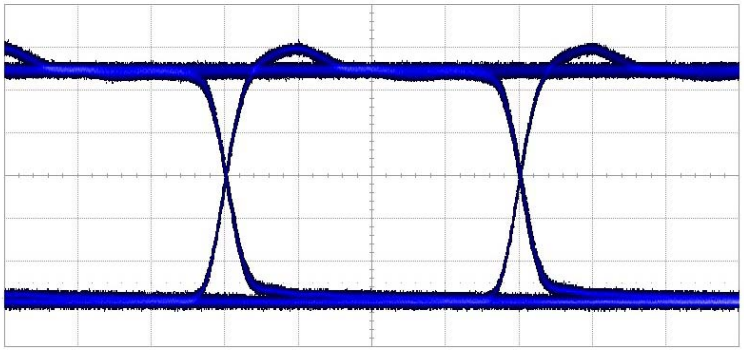


Figure 12 T_A= –40°C (t_r = 2.8 ns (typ.); t_f = 3.0 ns (typ.); Optical Overshoot = 11,2% (typ.); Horizontal = 5 ns/div)



Terminology

An opto-electrical ("O/E") converter	is used to convert the optical signal to an electrical signal. In order to measure the characteristics of the optic transmitter performance the output of the O/E converter is connected to an oscilloscope.
Duty Cycle distortion (""DCD")	is the mean difference between width of positive going pulses (low to high to low) and negative going pulses (high to low to high) measured over all pulses acquired waveform. DCD values mentioned in this AN are based on widths measured at 50% of the O/E converted signal amplitude.
Optical overshoot	is the amount of overshoot following a rising edge of the O/E converted signal.
Optical rise time ("t_r")	is the transition time from 10% to 90% for a rising edge of the O/E converted signal.
Optical fall time ("t_f")	is the transition time from 90% to 10% for a falling edge of the O/E converted signal.
PRBS	stands for "Pseudo Random Binary Sequence" and is a common used test pattern generated by a Pulse Pattern Generator connected to the electrical input of the driver circuit. By selecting "PRBS2^15-1" the generator is using 15 tabs of an internal linear-feedback shift register to create random bits of 1 and 0. The sequence length is determined by the number of used tabs (l=2^N - 1). With a selected data rate of 50MBd (pulse width = 20 ns) the PRBS sequence restarts each ≅ 0.655ms (=2^15-1 x 20 ns). The electrical input line of the driver circuits were terminated with 50 Ω and following electrical input levels were selected: LOW level=0V; HIGH level=2.0V.

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