AFBR-725AMMZ

SFP28 for Multi-Mode Optical Fiber
Digital Diagnostic SFP, 850nm, Low Voltage (3.3V)
Extended Temperature Multi-Rate CRPI and
Ethernet Optical Transceiver

Data Sheet- Preliminary

Description

Avago Technologies' AFBR-725AMMZ optical transceiver supports high speed serial links over multi-mode optical fiber for 25G CPRI and Ethernet Applications. The product is compliant with Small Form Pluggable industry agreements SFP and SFP28 for mechanical and low speed electrical specifications. High speed electrical and optical specifications are compliant with IEEE802.3 for 25GBASE-SR.

The AFBR-725AMMZ is a 850nm transceiver which ensures compliance with 25GBASE-SR specifications. Per the requirements of 25GE, internal clock and data recovery circuits (CDRs) are present on both electrical input and electrical output of this transceiver. These CDRs will lock at 24.33 Gb/s or 25.78Gb/s. The CDRs can be bypass to enable 10G data rate transmission.

Digital diagnostic monitoring information (DMI) is present in the AFBR-725AMMZ per the requirements of SFF-8472, providing real time monitoring information of transceiver laser, receiver and environment conditions over a SFF-8419 2-wire serial interface.

Related Products

- AFBR-725SMZ: 850nm SFP28 for 25GBASE-SR, 0/70C
- AFBR-89CDDZ: 850nm QSFP28 for 100GBASE-SR4
- AFBR-79EQDZ: 850nm QSFP+ for 40GBASE-SR4, 100m
- AFBR-79E3PZ: 850nm QSFP+ for 40GBASE-SR4, 300m
- AFBR-709ISMZ: 850nm SFP+ for 10GBASE-SR/SW, -40/85C
- AFBR-709SMZ: 850nm SFP+ for 10GBASE-SR/SW, 0/70C
- AFCT-709SM: 1310nm SFP+ for 10GBASE-LR, 0/70C

Patent - www.avagotech.com/patents

Features

- Compliant to RoHS directives
- 850nm Vertical Cavity Surface Emitting Laser (VCSEL)
- Class 1 eye safe per IEC60825-1 and CDRH
- Extended temperature range (-20°C to 85°C) with cold start capability as low as -40°C.
- LC duplex connector optical interface conforming to ANSI TIA/EIA604-10 (FOCIS 10A)
- Diagnostic features per SFF-8472 "Diagnostic Monitoring Interface for Optical Transceivers"
- Enhanced operational features including variable electrical EQ/emphasis settings
- Real time monitoring of:
  - -Transmitter average optical power
  - -Received average optical power
  - -Laser bias current
  - -Temperature
  - -Supply Voltage
- SFP28 mechanical specifications per SFF-8432
- SFP28 compliant low speed interface per SFF-8419
- 25GBASE-SR compliant optical link distances

Applications

- Ethernet switches (director, stand alone, blade)
- Base Station CPRI interconnects
- Ethernet NIC Cards/Adapters
- Port side connections
- Inter-switch or inter-chassis aggregated links

Transmitter Section

The transmitter section includes a Transmitter Optical Sub-Assembly (TOSA), laser driver circuit, Clock and Data Recovery circuit (CDR) and an electrical input stage with variable equalization controls. The TOSA contains a 850nm Vertical Cavity Surface Emitting Laser (VCSEL) light source with integral light monitoring function and imaging optics to assure efficient optical coupling to the LC connector interface. The TOSA is driven by a laser driver IC, which uses the differential output from an integral Tx CDR stage to modulate and regulate VCSEL optical power. As mandated by 802.3, the integral CDR cleans up any incoming jitter accumulated from the host ASIC, PCB traces and SFP electrical connector. Between the SFP electrical connector and Tx CDR is a variable, 2-wire serial controlled, equalization circuit to optimize SFP performance with non ideal incoming electrical waveforms.

Receiver Section

The receiver section includes a Receiver Optical Sub-Assembly (ROSA), pre-amplification and post-amplification circuit, Clock and Data Recovery Circuit and an electrical output stage with variable emphasis controls. The ROSA, containing a high speed PIN detector, pre-amplifier and imaging optics efficiently couple light from the LC connector interface and perform an optical to electrical conversion. The resulting differential electrical signal passes through a post amplification circuit and into a Clock and Data Recovery circuit (CDR) for cleaning up accumulated jitter.

Digital Diagnostics

The AFBR-725AMMZ is compliant to the Diagnostic Monitoring Interface (DMI) defined in document SFF-8472. These features allow the host to access, via 2- wire serial, real time diagnostic monitors of transmit optical power, received optical power, temperature, supply voltage and laser operating current.

Low Speed Interfaces

Conventional low speed interface I/Os are available as defined in documents SFF-8419 to manage coarse and fine functions of the optical transceiver. On the transmit side, a Tx_DISABLE input is provided for the host to turn on and off the outgoing optical signal. A transmitter fault indicator output, Tx_FAULT, is available for the SFP to signal a host of a transmitter operational problem. A received optical power loss of signal indicator, RX_LOS, is available to advise the host of a receiver operational problem – such as a low optical input condition.

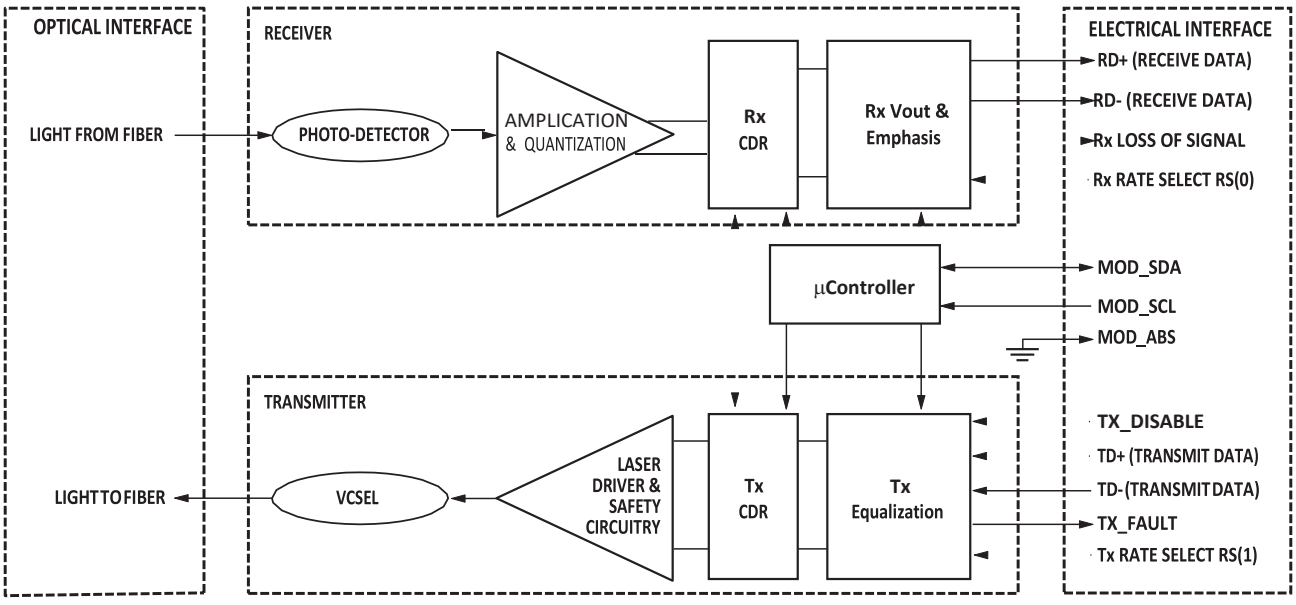


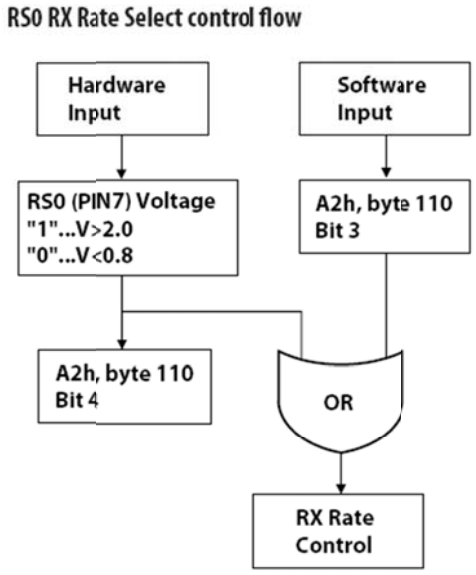
Figure 1. Transceiver functional diagram.

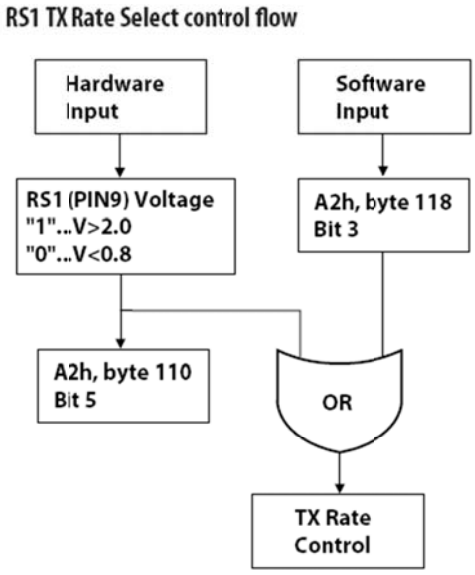
Rate Select Function

Function	State	Operation
Tx Rate Select RS(1)	High	Transmit Rate Select HIGH is defined for 24.33Gb/s and 25.78Gb/s operation with auto-detect. It configures the Tx CDR to lock on 24.33Gb/s or 25.78Gb/s, sets the Tx optical power and linear bandwidth for 25GE or CPRI option 10 operation. FEC is expected for 24.33Gb/s and 25.78Gb/s.
	Low	Transmit Rate Select LOW auto configures the internal Tx CDR for 10.3125Gb/s with the CDR bypassed. Transmit optical power and linear bandwidth are optimized accordingly. FEC is not expected for 10.3125Gb/s. When set low, the SFP behaves like a legacy SFP.
Rx Rate Select RS(0)	High	Receive Rate Select HIGH is defined for 24.33Gb/s and 25.78Gb/s operation with auto-detect. It configures the Rx CDR to lock on 24.33Gb/s or 25.78Gb/s, sets the Rx optical sensitivity and linear bandwidth for 25GE or CPRI option 10 operation. FEC is expected for 24.33Gb/s or 25.78Gb/s.
	Low	Receive Rate Select LOW auto configures the internal Rx CDR 10.3125Gb/s with the CDR bypassed. Receiver optical sensitivity and linear bandwidth are optimized accordingly. FEC is not expected for 10.3125Gb/s. When set low, the SFP behaves like a legacy SFP.

Rate Select Control

RX and RX rates can be independently controlled by either hardware input pins or via register writes. Module electrical input pins 7 and 9 are used to select RX and TX rate respectively. Status of each logic level is reflected to register byte 110 bit 4 and 5 on address A2h as shown in the diagram below. RX and TX rates can also be controlled via register writes to bytes 110 bit 3 and 118 bit 3. Power on default of these bits are logic low. Hardware and software control inputs are OR'd to allow flexible control.





RS0 Control Input		RX Operation	
Hardware	Software		
0	0	10GE, CPRI option 7 or 8	Rx CDR bypass
0	1	25GE, CPRI Option 10	Rx CDR engaged and auto detect
1	0	25GE, CPRI Option 10	Rx CDR engaged and auto detect
1	1	25GE, CPRI Option 10	Rx CDR engaged and auto detect

RS1 Control Input		TX Operation	
Hardware	Software		
0	0	10GE, CPRI option 7 or 8	Tx CDR bypass
0	1	25GE, CPRI Option 10	Tx CDR engaged and auto detect
1	0	25GE, CPRI Option 10	Tx CDR engaged and auto detect
1	1	25GE, CPRI Option 10	Tx CDR engaged and auto detect

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	EN61000-4-2, Criterion B	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure
Laser Eye Safety and Equipment Type Testing TÜV Rheinland Product Safety | BAUART GEPRÜFT / TYPE APPROVED	US FDA CDRH AEL Class 1 US21 CFP, Subchapter J per Paragraphs 1002.10 and 1002.12 (IEC) EN60825-1:1994 +A11 +A2 (IEC) EN60825-2:1994 +A1 (IEC) EN60950:1992 +A1 +A2 +A3 +A4 +A11	CDRH Certification 9720151-155 TUV File: R72121699
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E173874
RoHS Compliance		Less than 1000 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls (PPB) and polybrominated biphenyl ethers (PBDE).

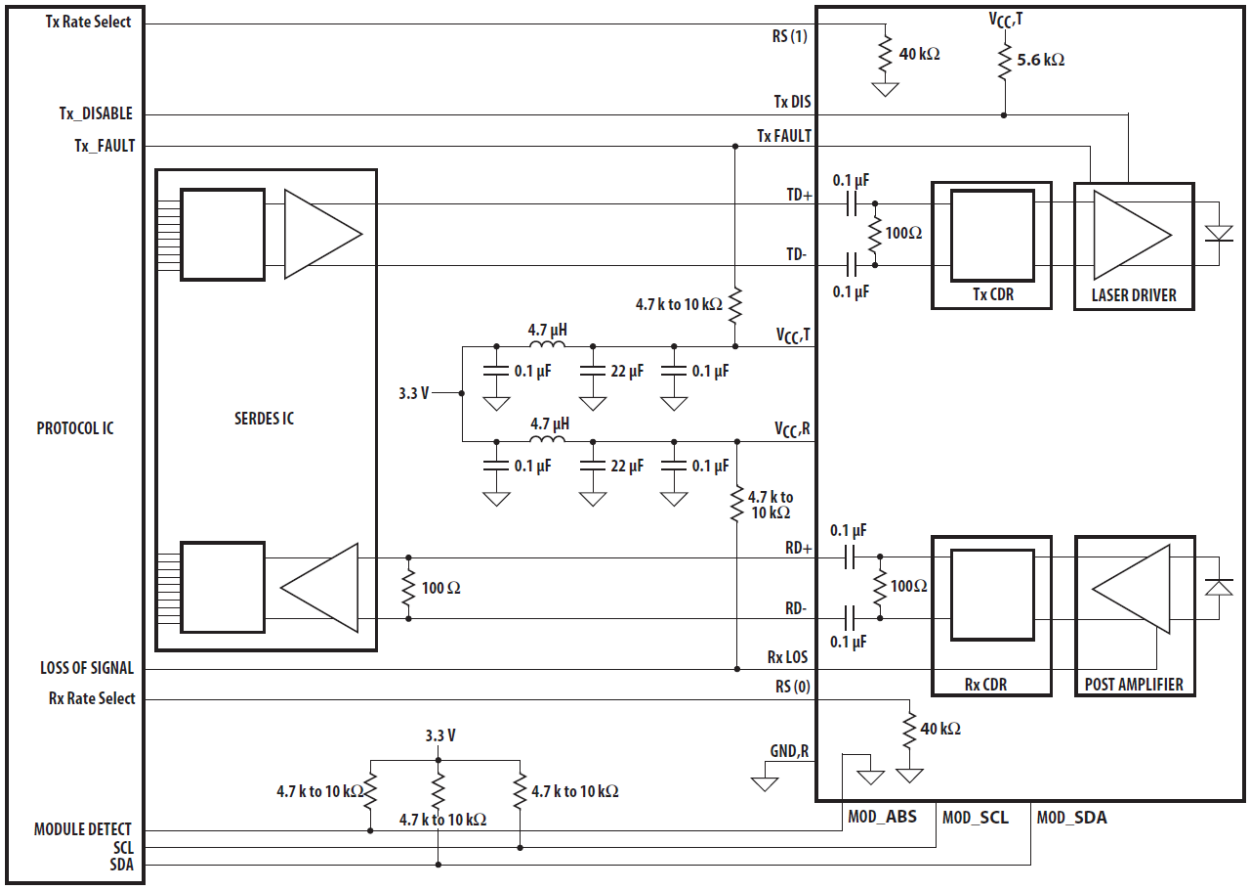
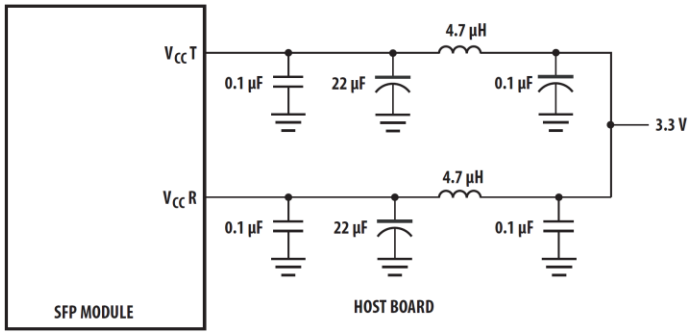


Figure 2. Typical application configuration



NOTE: INDUCTORS MUST HAVE LESS THAN 0.5Ω SERIES RESISTANCE TO LIMIT VOLTAGE DROP TO THE SFP MODULE.

Figure 3. Recommended power supply filter

Table 2. Pin Description

Pin	Name	Function/Description	Notes
1	VeeT	Transmitter Ground	
2	TX_FAULT	Transmitter Fault Indication – High indicates a fault condition	Note 1
3	TX_DISABLE	Transmitter Disable – Module optical output disables on high or open	Note 2
4	MOD_SDA	Module Definition 2 – Two wire serial ID interface data line (SDA)	Note 3
5	MOD_SCL	Module Definition 1 – Two wire serial ID interface clock line (SCL)	Note 3
6	MOD_ABS	Module Definition 0 – Grounded in module (module present indicator)	Note 3
7	Rx Rate Select, RS(0)	See Special Rate Select Function	
8	RX_LOS	Loss of Signal – High indicates loss of received optical signal	Note 4
9	Tx Rate Select, RS(1)	See Special Rate Select Function	
10	VeeR	Receiver Ground	
11	VeeR	Receiver Ground	
12	RD-	Inverse Received Data Out	Note 5
13	RD+	Received Data Out	Note 5
14	VeeR	Receiver Ground	
15	VccR	Receiver Power + 3.3 V	Note 6
16	VccT	Transmitter Power + 3.3 V	Note 6
17	VeeT	Transmitter Ground	
18	TD+	Transmitter Data In	Note 7
19	TD-	Inverse Transmitter Data In	Note 7
20	VeeT	Transmitter Ground	

Notes

1. TX_FAULT is an open collector/drain output, which must be pulled up with a 4.7k – 10kΩ resistor on the host board. When high, this output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.
2. TX_DISABLE is an input that is used to shut down the transmitter optical output. It is internally pulled up (within the transceiver) with a 5.6kΩ resistor.
   Low (0 – 0.8V): Transmitter on
   Between (0.8V and 2.0V): Undefined
   High (2.0 – Vcc max) or OPEN: Transmitter Disabled
3. The signals Mod_ABS, SCL, SDA designate the two wire serial interface pins. They must be pulled up with a 4.7k – 10kΩ resistor on the host board.
   Mod_ABS is grounded by the module to indicate the module is present
   Mod_SCL is serial clock line (SCL) of two wire serial interface
   Mod_SDA is serial data line (SDA) of two wire serial interface
4. RX_LOS (Rx Loss of Signal) is an open collector/drain output that must be pulled up with a 4.7k – 10kΩ resistor on the host board. When high, this output indicates the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.
5. RD-/+ designate the differential receiver outputs. They are AC coupled 100Ω differential lines which should be terminated with 100Ω differential at the host SERDES input. AC coupling is done inside the transceiver and is not required on the host board. The voltage swing on these lines will be between 50 and 900 mV differential (25 – 450 mV single ended) when properly terminated.
6. VccR and VccT are the receiver and transmitter power supplies. See SFF-8419 for the details.
7. TD-/+ designate the differential transmitter inputs. They are AC coupled differential lines with 100Ω differential termination inside the module. The AC coupling is done inside the module and is not required on the host board. The inputs will accept differential swings of 40 – 1200 mV (20 – 600 mV single ended), though it is recommended that values between 50 and 900 mV differential (25 – 450 mV single ended) be used for best EMI performance.

Table 3. Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min.	Max.	Units	Reference
Storage Temperature	T_S	-40	85	°C	Note 1
Case Operating Temperature	T_C	-40	85	°C	
Relative Humidity	RH	5	95	%	
Supply Voltage	V_{CC}	-0.5	3.63	V	
Low Speed Input Voltage	V_I	-0.5	VCC+0.5, 3.63	V	

Table 4. Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min.	Typ.	Max.	Units	Reference
Case Operating Temperature	Tc	-20		85	°C	Note 2
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate			24.33024	25.78125	Gb/s	Note 3
Two Wire Serial (TWS) Interface Clock Rate				400	kHz	Note 4

Table 5. Transceiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Reference
Transceiver Power Consumption				1.0	W	
Transceiver Power Supply Current				319	mA	
Power Supply Noise Rejection (peak-peak)	PSNR			66	mV	Note 5
TX_FAULT, RX_LOS	I_{OH}	-50		37.5	µA	Note 6
	V_{OH}	-0.3		0.4	V	
TX_DIS, RS0, RS1	V_{IH}	2.0		V_{CC}+0.3	V	
	V_{IL}	-0.3		0.8	V	
MOD_SCL, MOD_SDA	V_{OH}	VCC_Hst-0.5		VCC_Hst+0.3	V	Note 7
	V_{OL}	0.0		0.4	V	
	V_{IH}	VccT*0.7		VccT+0.5	V	
	V_{IL}	-0.3		VccT*0.3	V	

Notes:

1. Absolute maximum ratings are those values beyond which damage to the device may occur if these limits are exceeded for other than a short period of time. See Reliability Data Sheet for specific reliability performance. Between Absolute Maximum Ratings and the Recommended Operating Conditions functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time.
2. The position of case temperature measurement is shown in Figure 8. Continuous operation at the maximum Recommended Operating Case Temperature should be avoided in order not to degrade reliability.
3. 25GE requires FEC RS(528,514) encoding per IEEE 802.3.
4. With 500us clock stretch per SFF-8419.
5. Filter per SFP specification is required on the host board to remove 10Hz to 2MHz content.
6. Measured with a 4.7k load pulled up to the host board to 3.3V
7. Mod_SCL and Mod_SDA must be pulled up externally with a 4.7k-10kΩ resistor on the host board to host VCC (3.14 < VCC_Hst < 3.46V).

Table 6. High Speed Electrical Module Input Characteristics

From 25GAUI C2M Clause 109B. The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate	TP1		24.33024	25.78125	GBd/s	± 100 ppm
Differential pk-pk Input Voltage Tolerance	TP1a	900			mV	
Differential Input Return Loss. min	TP1		Eq 83E-5		dB	802.3bm
Common Mode to Differential Input Return Loss, Min	TP1		Eq 83E-6		dB	802.3bm
Differential Termination Mismatch	TP1			10	%	
Module stressed input test	TP1a		83E.3.4.2			802.3bm, below
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode output voltage	TP1a	-0.350		2.85	V	Note 8
Electrical Input LOS Assert Threshold, Differential Peak-to-Peak Voltage Swing	ΔVdi pp los	50			mVpp	
LOS Hysteresis		0.5		4	dB	Note 9

Parameter	Value	Units	Notes/Conditions
Module stressed input test			Note 10
Eye width	0.46	UI	
Applied pk-pk sinusoidal jitter	Table 88-13		
Eye height	95	mV	

Notes:

8. DC common mode voltage generated by the host. Specific tion includes effects of ground offset voltage.
9. LOS Hysteresis is defined as 20*Log(LOS De-assert Level / LOS Assert Level).
10. Module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1

Table 7. Reference Points

Test Point	Description
TP0	Host ASIC transmitter output at ASIC package pin on a DUT board
TP1	Input to module compliance board through mated module compliance board and module connector. Used to test module input
TP1A	Host ASIC transmitter output across the Host Board and Host Edge Card connector at the output of the host compliance board
TP2	Optical transmitter output as measured at the end of a 2-5m patch cord mated to the optical module
TP3	Optical test point as measured at the end of an optical fiber cable; closest test point to the presumed optical receiver input.
TP4	Module output through mated module and host edge card connector through module compliance board
TP4A	Input to host compliance board through mated host compliance board and host edge card connector. Used to test host input
TP5	Input to host ASIC

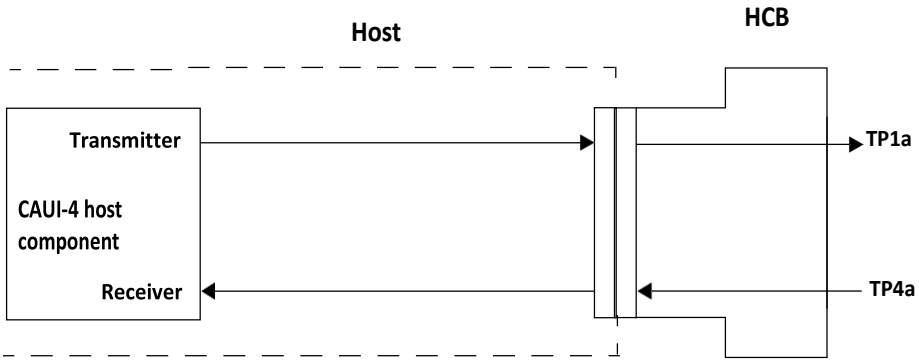


Figure 83E–4—Host CAUI-4 Compliance Points

Figure 4. IEEE 802.3bm CAUI-4 compliance points TP1a, TP4a

Note a reference receiver is used to measure host eye width and eye height at TP1a. The reference receiver includes a selectable continuous time linear equalizer (CTLE) which is described by Equation (83E–4, below) with coefficients given in Table 83E–2.

$$H(f) = \frac{GP_1P_2}{Z_1}$$

where:
H(f) is the CTLE transfer function, *f* is the frequency in GHz
G is the CTLE gain
P_1, P_2 are the CTLE poles in Grad/s
Z_1 is the CTLE zero in Grad/s

Table 83E-2 - Reference CTLE coefficients

Peaking (dB)	G	$P_1/2\pi$	$P_2/2\pi$	$Z_1/2\pi$
1	0.89125	18.6	14.1	8.364
2	0.79433	18.6	14.1	7.099
3	0.70795	15.6	14.1	5.676
4	0.63096	15.6	14.1	4.9601
5	0.56234	15.6	14.1	4.358
6	0.50119	15.6	14.1	3.844
7	0.44668	15.6	14.1	3.399
8	0.39811	15.6	14.1	3.012
9	0.35481	15.6	14.1	2.672

Table 8. High Speed Electrical Module Output Characteristics

From 25GAUI C2M Clause 109B. The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate	TP4		24.33024	25.78125	GB/s	± 100 ppm
Common Mode AC Output Voltage, RMS	TP4			17.5	mV, rms	
Differential Output Voltage	TP4			900	mV	
Eye Width	TP4	0.57			UI	
Eye Height, Differential	TP4	228			mV	
Vertical Eye Closure	TP4			5.5	dB	
Differential Output Return Loss, min	TP4		Eq 83E-2		dB	802.3bm
Common to Differential Mode Conversion, min	TP4		Eq 83E-3		dB	802.3bm
Differential termination mismatch	TP4			10	%	
Transition Time (20% to 80%)	TP4	12			ps	
DC common mode voltage	TP4	-0.35		2.85	V	Note 11

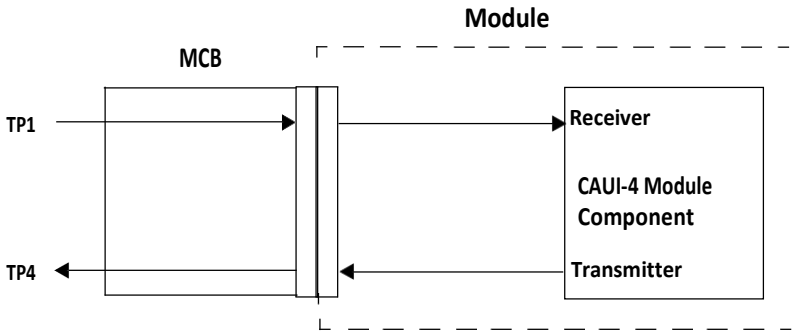


Figure 83E–5—Module CAUI-4 Compliance Points

Figure 5. IEEE 802.3bm CAUI-4 compliance points TP1, TP4

Notes:

11. DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

Table 9. High Speed Optical Transmitter Characteristics

From 25GBASE-SR, 802.3by Clause 112. The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point*	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate			24.33024	25.78125	GB/s	± 100ppm
Center wavelength range	TP2	840		860	nm	
RMS spectral width [12]	TP2			0.60	nm	
Average launch power	TP2	-8.4	-	+2.4	dBm	
Optical Modulation Amplitude (OMA)	TP2	-6.4 [13]	-	+3.0	dBm	
Launch Power in OMA minus TDEC	TP2	-7.3			dBm	
Transmitter and dispersion eye closure (TDEC)	TP2			4.3	dB	
Average launch power of OFF transmitter	TP2	-		-30	dBm	
Extinction ratio	TP2	2	-	-	dB	
Optical return loss tolerance	TP2			12	dB	
Encircled Flux [14]	TP2	≥ 86% at 19um ≤ 30% at 4.5um				Type A1a.2 50um Fiber per IEC 61280-1-4
Transmitter Eye Mask definition: {X1, X2, X3, Y1, Y2, Y3}	TP2	SPECIFICATION VALUES {0.3, 0.38, 0.45, 0.35, 0.41, 0.5}				Hit Ratio 1.5 x 10^{-3} hits per sample

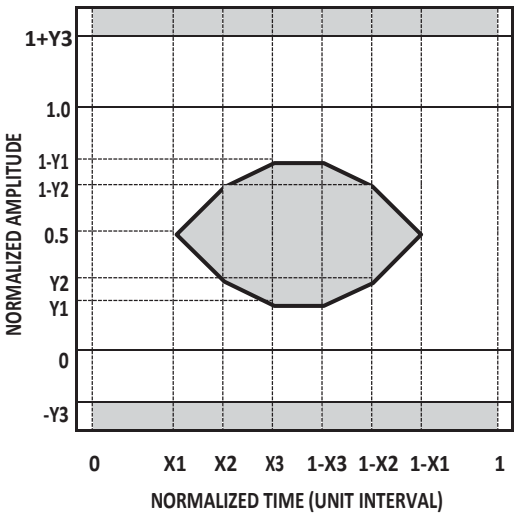


Figure 6. Transmitter eye mask definitions

Notes:

12. RMS spectral width is the standard deviation of the spectrum.

13. Even if the TDEC < 0.9dB, the OMA (min) must exceed this value.

14. If measured into type A1a.2 50um fiber in accordance with IEC 61280-1-4.

Table 10. High Speed Optical Receiver Characteristics

From 25GBASE-SR, 802.3by Clause 112. The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point*	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate			24.33024	25.78125	Gb/s	± 100ppm
Center wavelength range	TP3	840		860	nm	
Damage Threshold [15]	TP3	+3.4			dBm	
Average Receive Power[16]	TP3	-10.3		+2.4	dBm	
Receive Power (OMA)	TP3			+3.0	dBm	
Receiver Reflectance	TP3			-12	dB	
Stressed Receiver Sensitivity OMA [17]	TP3			-5.2	dBm	
Conditions of stressed receiver sensiti vity test [18]						
Stressed eye closure (SEC)			4.3		dB	
Stressed eye J2 jitter			0.39		UI	
Stressed eye J4 jitter			0.53		UI	
Stressed Receiver Eye mask definition: X1, X2, X3, Y1, Y2, Y3			SPECIFICATION VALUES {0.28, 0.50, 0.50, 0.33, 0.33, 0.40}			Hit Ratio $5x10^{-5}$ hits per sample
LOS Assert - OMA	TP3	-30			dBm	
LOS De-Assert - OMA	TP3			-9.1	dBm	
LOS Hysteresis	TP3	0.5			dB	

Notes:

15. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level. The receiver does not have to operate correctly at this input power

16. Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value can-not be compliant; however, a value above this does not ensure compliance.

17. Measured with conformance test signal at TP3 (see 802.3bm section 95.8.8) for BER specified in 802.3bm section 95.1.1.

18. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver

Table 11. Transceiver SOFT DIAGNOSTIC Timing Characteristics

(TC = -20°C to 85°C, VccT, VccR = 3.3V ± 5%)

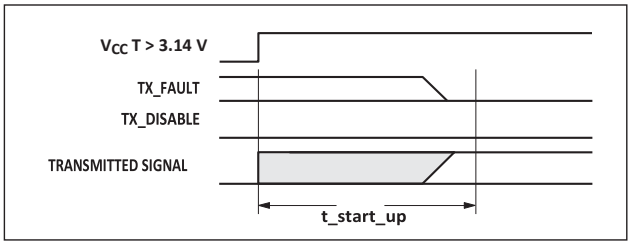
Parameter	Symbol	Min.	Max.	Unit	Notes
Hardware TX_DISABLE Assert Time	t_off		100	µs	Note 1
Hardware TX_DISABLE Negate Time	t_on		2	ms	Note 2
Time to initialize, including reset of TX_FAULT	t_init		300	ms	Note 3
Hardware TX_FAULT Assert Time	t_fault		1	ms	Note 4
Hardware TX_DISABLE to Reset	t_reset	10		µs	Note 5
Hardware RX_LOS DeAssert Time	t_loss_on		100	µs	Note 6
Hardware RX_LOS Assert Time	t_loss_off		100	µs	Note 7
Software TX_DISABLE Assert Time	t_off_soft		100	ms	Note 8
Software TX_DISABLE Negate Time	t_on_soft		100	ms	Note 9
Software Tx_FAULT Assert Time	t_fault_soft		100	ms	Note 10
Software Rx_LOS Assert Time	t_loss_on_soft		100	ms	Note 11
Software Rx_LOS De-Assert Time	t_loss_off_soft		100	ms	Note 12
Analog parameter data ready	t_data		1000	ms	Note 13
Serial bus hardware ready	t_serial		300	ms	Note 14
Serial bus buffer time	t_buf	20		µs	Note 15
Complete Single or Sequential Write up to 4 Byte	twR		40	ms	Note 16
Complete Sequential Write of 5-8 Byte	twR		80	ms	
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	µs	Note 17
Serial ID Clock Rate	f_serial_clock		400	kHz	Note 18

Notes

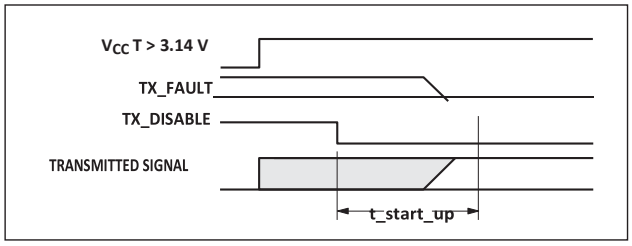
1. Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal.
2. Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal.
3. Time from power on or falling edge of Tx_Disable to when the modulated optical output rises above 90% of nominal.
4. From occurrence of fault to assertion of TX_FAULT.
5. Time TX_DISABLE must be held high to reset the laser fault shutdown circuitry.
6. Time from loss of optical signal to Rx_LOS Assertion.
7. Time from valid optical signal to Rx_LOS De-Assertion.
8. Time from two-wire interface assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output falls below 10% of nominal. Measured from falling clock edge after stop bit of write transaction.
9. Time from two-wire interface de-assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output rises above 90% of nominal.
10. Time from fault to two-wire interface TX_FAULT (A2h, byte 110, bit 2) asserted.
11. Time for two-wire interface assertion of Rx_LOS (A2h, byte 110, bit 1) from loss of optical signal.
12. Time for two-wire interface de-assertion of Rx_LOS (A2h, byte 110, bit 1) from presence of valid optical signal.
13. From power on to data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates analog monitoring circuitry is functional.
14. Time from power on until module is ready for data transmission over the serial bus (reads or writes over A0h and A2h).
15. Time between START and STOP commands.
16. Time from stop bit to completion of a 1-8 byte write command.
17. Maximum time the SFP+ module may hold the SCL line low before continuing with a read or write operation.
18. With a maximum Clock Stretch of 500us. A maximum of 100kHz operation can be supported without a Clock Stretch.

Table 12. Transceiver Digital Diagnostic Monitor (Real Time Sense) Characteristics
(T_C = -20 °C to 85 °C, $V_{CC}T$, $V_{CC}R$ = 3.3 V ± 5%)

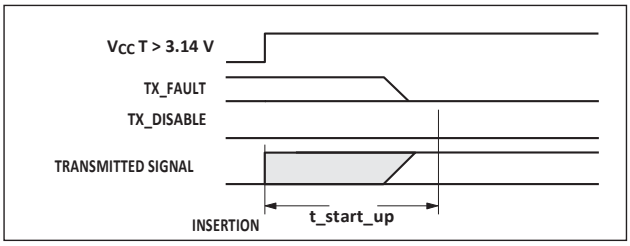
Parameter	Symbol	Min.	Units	Notes
Transceiver Internal Temperature Accuracy	T_{INT}	±3.0	°C	Temperature is measured internal to the transceiver. Valid from = -20°C to 85 °C case temperature.
Transceiver Internal Supply Voltage Accuracy	V_{INT}	± 0.1	V	Supply voltage is measured internal to the transceiver and can, with less accuracy, be correlated to voltage at the SFP Vcc pin. Valid over 3.3 V ± 5%.
Transmitter Laser DC Bias Current Accuracy	I_{INT}	± 10	%	IINT is better than ± 10% of the nominal value.
Transmitted Average Optical Output Power Accuracy	P_T	± 3.0	dB	Coupled into 50um multi-mode fiber. Valid from -8.4dBm to +2.4dBm avg.
Received Optical Input Power Accuracy	P_R	± 3.0	dB	Coupled from 50um multi-mode fiber. Valid from -10.3dBm to +2.4dBm avg.



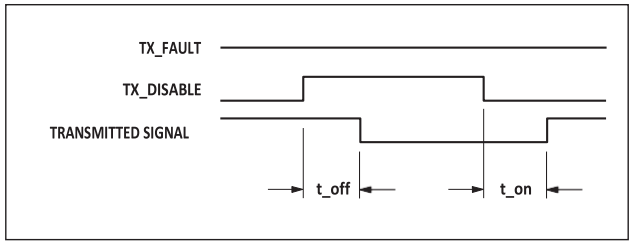
t_start_up: TX DISABLE NEGATED



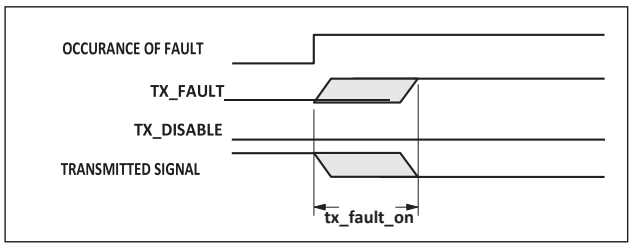
t_start_up: TX DISABLE ASSERTED



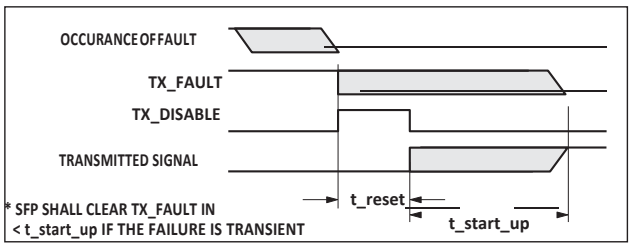
t_start_upt: TX DISABLE NEGATED, MODULE HOT PLUGGED



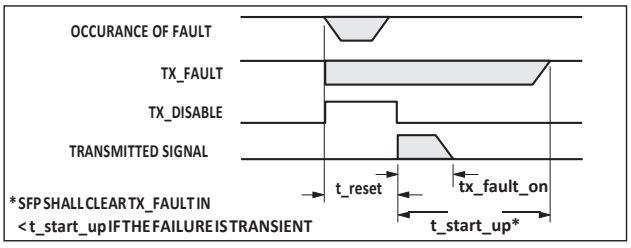
t-off & t-on: TX DISABLE ASSERTED THEN NEGATED



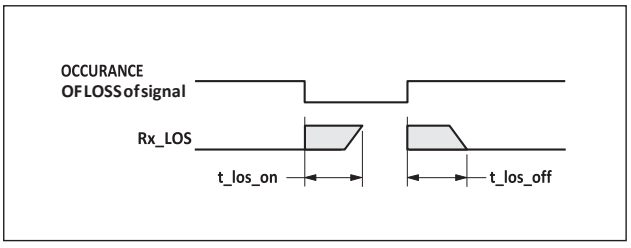
tx_fault_on: TX FAULT ASSERTED, TX SIGNAL NOT RECOVERED



t_reset: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL RECOVERED



tx_fault_on: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL NOT RECOVERED



t_los_on & t_los_off

Figure 7. Transceiver timing diagrams (module installed except where noted)

Table 13. EEPROM Serial ID Memory Contents – Address A0h

Byte # Decimal	Hex	Description	Byte # Decimal	Hex	Description
0	03	SFP physical device	37	00	Hex Byte of Vendor OUI [1]
1	04	SFP function defined by serial ID only	38	17	Hex Byte of Vendor OUI [1]
2	07	LC optical connector	39	6A	Hex Byte of Vendor OUI [1]
3	00		40	41	"A" - Vendor Part Number ASCII Character
4	00		41	46	"F" - Vendor Part Number ASCII Character
5	00		42	42	"B" - Vendor Part Number ASCII Character
6	00		43	52	"R" - Vendor Part Number ASCII Character
7	00		44	2D	"-" - Vendor Part Number ASCII Character
8	40	Shortwave laser without OFC (open fiber control)	45	37	"7" - Vendor Part Number ASCII Character
9	04	Multi-mode 50um optical media	46	32	"2" - Vendor Part Number ASCII Character
10	00		47	35	"5" - Vendor Part Number ASCII Character
11	06	64B/66B data	48	41	"A" - Vendor Part Number ASCII Character
12	FF	Greater than 25.0Gb/s (See Address 66)	49	4D	"M" - Vendor Part Number ASCII Character
13	00		50	4D	"M" - Vendor Part Number ASCII Character
14	00		51	5A	"Z" - Vendor Part Number ASCII Character
15	00		52	20	" " - Vendor Part Number ASCII Character
16	00		53	20	" " - Vendor Part Number ASCII Character
17	00		54	20	" " - Vendor Part Number ASCII Character
18	0A	100m of OM4 50/125um fiber at 25GE	55	20	" " - Vendor Part Number ASCII Character
19	07	70m of OM3 50/125um fiber at 25GE	56	20	" " - Vendor Revision ASCII Character
20	41	"A" - Vendor Name ASCII Character	57	20	" " - Vendor Revision ASCII Character
21	56	"V" - Vendor Name ASCII Character	58	20	" " - Vendor Revision ASCII Character
22	41	"A" - Vendor Name ASCII Character	59	20	" " - Vendor Revision ASCII Character
23	47	"G" - Vendor Name ASCII Character	60	03	Hex Byte of Laser Wavelength [2]
24	4F	"O" - Vendor Name ASCII Character	61	52	Hex Byte of Laser Wavelength [2]
25	20	" " - Vendor Name ASCII Character	62	00	
26	20	" " - Vendor Name ASCII Character	63		Checksum for Bytes 0-62 [3]
27	20	" " - Vendor Name ASCII Character	64	08	CDRs present. 1W power class
28	20	" " - Vendor Name ASCII Character	65	3A	Hardware Tx_Disable, Tx_Fault, Rx_LOS, Rate Select
29	20	" " - Vendor Name ASCII Character	66	67	25.78 Gbit/sec nominal bit rate (25GE)
30	20	" " - Vendor Name ASCII Character	67	00	
31	20	" " - Vendor Name ASCII Character	68 - 83		Vendor Serial Number ASCII characters [4]
32	20	" " - Vendor Name ASCII Character	84 - 91		Vendor Date Code ASCII characters [5]
33	20	" " - Vendor Name ASCII Character	92	68	Digital diagnostics, Internal Cal, Rx Pwr Avg
34	20	" " - Vendor Name ASCII Character	93	F8	Alarms/Warnings, Software Tx_Disable, Tx-Fault, Rx_LOS, Rate Select
35	20	" " - Vendor Name ASCII Character	94	08	SFF-8472 compliance to revision 12.2
36	02	25GBASE-SR	95		Checksum for Bytes 62-94 [3]
			96 – 255	00	

Notes:

1. The IEEE Organizationally Unique Identified OUI) assigned to Avago Technologies is 00-17-6A (3 bytes of hex).
2. Laser Wavelength is represented in 16 unsigned buts. The hex representation of 850nm is 0352.
3. Addresses 63 and 95 are checksums calculated (per SFF-8472 and SFF-8074) and stored prior to product shipment.
4. Address 68-83 specify the AFBR-725AMMZ ASCII serial number and will vary on a per unit basis.
5. Address 84-91 specify the AFBR-725AMMZ ASCII data code and will vary on a per date code basis.

Table 14. EEPROM Serial ID Memory Contents - Enhanced SFP Memory (Address A2h)

Byte # Decimal	Notes	Byte # Decimal	Notes	Byte # Decimal	Notes
0	Temp H Alarm MSB [1]	26	Tx Power L Alarm MSB [4]	104	Real Time Rx Power MSB [5]
1	Temp H Alarm LSB [1]	27	Tx Power L Alarm LSB [4]	105	Real Time Rx Power LSB [5]
2	Temp L Alarm MSB [1]	28	Tx Power H Warning MSB [4]	106	Reserved
3	Temp L Alarm LSB [1]	29	Tx Power H Warning LSB [4]	107	Reserved
4	Temp H Warning MSB [1]	30	Tx Power L Warning MSB [4]	108	Reserved
5	Temp H Warning LSB [1]	31	Tx Power L Warning LSB [4]	109	Reserved
6	Temp L Warning MSB [1]	32	Rx Power H Alarm MSB [5]	110	Status/Control – See Table 15
7	Temp L Warning LSB [1]	33	Rx Power H Alarm LSB [5]	111	Reserved
8	Vcc H Alarm MSB [2]	34	Rx Power L Alarm MSB [5]	112	Flag Bits – See Table 16
9	Vcc H Alarm LSB [2]	35	Rx Power L Alarm LSB [5]	113	Flag Bits – See Table 16
10	Vcc L Alarm MSB [2]	36	Rx Power H Warning MSB [5]	114	Tx Input EQ Control - See Table 19, 20
11	Vcc L Alarm LSB [2]	37	Rx Power H Warning LSB [5]	115	Rx Output Emphasis Control - See Table 21, 22
12	Vcc H Warning MSB [2]	38	Rx Power L Warning MSB [5]	116	Flag Bits – See Table 16
13	Vcc H Warning LSB [2]	39	Rx Power L Warning LSB [5]	117	Flag Bits – See Table 16
14	Vcc L Warning MSB [2]	40-55	Optional Alarm and Warning	118	Status/Control – See Table 17
15	Vcc L Warning LSB [2]	56-94	External Calibration Constants [6]	119	CDR Loss of Lock Status - See Table 18
16	Tx Bias H Alarm MSB[3]	95	Checksum for Bytes 0-94 [7]	120-126	Reserved
17	Tx Bias H Alarm LSB[3]	96	Real Time Temperature MSB [1]	127	Page Select Control
18	Tx Bias L Alarm MSB [3]	97	Real Time Temperature LSB [1]	128-247	Customer Writable
19	Tx Bias L Alarm LSB[3]	98	Real Time Vcc MSB [2]	248-255	Vendor Specific
20	Tx Bias H Warning MSB[3]	99	Real Time Vcc LSB [2]		
21	Tx Bias H Warning LSB[3]	100	Real Time Tx Bias MSB [3]		
22	Tx Bias L Warning MSB [3]	101	Real Time Tx Bias LSB [3]		
23	Tx Bias L Warning LSB[3]	102	Real Time Tx Power MSB [4]		
24	Tx Power H Alarm MSB [4]	103	Real Time Tx Power LSB [4]		
25	Tx Power H Alarm LSB [4]				

Notes:

1. Temperature (Temp) is decoded as a 16 bit signed two's complement integer in increments of 1/256 °C.
2. Supply Voltage (Vcc) is decoded as a 16 bit unsigned integer in increments of 100 μV.
3. Tx bias current (Tx Bias) is decoded as a 16 bit unsigned integer in increments of 2 μA.
4. Transmitted average optical power (Tx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 μW.
5. Received average optical power (Rx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 μW.
6. Bytes 56-94 are not intended for use, but have been set to default values per SFF-8472.
7. Byte 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.

Table 15. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 110)

Bit #	Status/Control Name	Description	Notes
7	TX_DISABLE State	Digital state of TX_DISABLE Input Pin (1 = TX_DISABLE asserted)	Note 1
6	Soft TX_DISABLE Control	Read/write bit for changing digital state of TX_DISABLE function	Note 1, 2
5	RS(1) State	Digital state of SFP input pin AS(1) per SFF-8079 or RS(1) per SFF-8431	
4	Rate_Select State [aka. "RS(0)"]	Digital state of the SFP Rate_Select Input Pin.	
3	Soft Rate_Select Select [aka. "RS(0)"]	See Special Rate Select Function section	
2	TX_FAULT State	Digital state of TX_FAULT Output Pin (1 = TX_FAULT asserted)	Note 1
1	RX_LOS State	Digital state of SFP RX_LOS Output Pin (1 = RX_LOS asserted)	Note 1
0	Data Ready (Bar)	Indicates transceiver is powered and real time sense data is ready (0 = Data Ready)	

Notes:
1. The response time for soft commands of the AFBR-725AMMZ is 100msec as specified by MSA
2. Bit 6 is logic OR'd with the SFP TX_DISABLE input pin 3 …. either asserted will disable the SFP transmitter.

Table 16. EEPROM Serial ID Memory Contents – Alarms and Warnings (Address A2h, Bytes 112, 113, 116, 117)

Byte	Bit	Flag Bit Name	Description
112	7	Temp High Alarm	Set when transceiver internal temperature exceeds high alarm threshold.
	6	Temp Low Alarm	Set when transceiver internal temperature exceeds low alarm threshold.
	5	Vcc High Alarm	Set when transceiver internal supply voltage exceeds high alarm threshold.
	4	Vcc Low Alarm	Set when transceiver internal supply voltage exceeds low alarm threshold.
	3	Tx Bias High Alarm	Set when transceiver laser bias current exceeds high alarm threshold.
	2	Tx Bias Low Alarm	Set when transceiver laser bias current exceeds low alarm threshold.
	1	Tx Power High Alarm	Set when transmitted average optical power exceeds high alarm threshold.
	0	Tx Power Low Alarm	Set when transmitted average optical power exceeds low alarm threshold.
113	7	Rx Power High Alarm	Set when received average optical power exceeds high alarm threshold.
	6	Rx Power Low Alarm	Set when received average optical power exceeds low alarm threshold.
	0-5	reserved	
116	7	Temp High Warning	Set when transceiver internal temperature exceeds high warning threshold.
	6	Temp Low Warning	Set when transceiver internal temperature exceeds low warning threshold.
	5	Vcc High Warning	Set when transceiver internal supply voltage exceeds high warning threshold.
	4	Vcc Low Warning	Set when transceiver internal supply voltage exceeds low warning threshold.
	3	Tx Bias High Warning	Set when transceiver laser bias current exceeds high warning threshold.
	2	Tx Bias Low Warning	Set when transceiver laser bias current exceeds low warning threshold.
	1	Tx Power High Warning	Set when transmitted average optical power exceeds high warning threshold.
	0	Tx Power Low Warning	Set when transmitted average optical power exceeds low warning threshold.
117	7	Rx Power High Warning	Set when received average optical power exceeds high warning threshold.
	6	Rx Power Low Warning	Set when received average optical power exceeds low warning threshold.
	0-5	reserved	

Table 17. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 118)

Bit #	Status/Control Name	Description	Notes
4-7	Reserved		
3	Soft RS(1) Select	See Special Rate Select Function section	
2	Reserved		
1	Power Level State	Always set to zero. Value of zero indicates Power Level 1 operation (1 Watt max)	
0	Power Level Select	Unused. This device supports power level zero (1 Watt max) only.	

Table 18. EEPROM Serial ID Memory Contents – CDR Loss of Lock (LOL) Status Indicators (Address A2h, Byte 119).

Bit #	Status/Control Name	Description
7-2	Reserved	
1	Tx CDR LOL Flag	A value of 0 indicates the CDR is locked. A value of 1 indicates CDR loss of lock.
0	Rx CDR LOL Flag	A value of 0 indicates the CDR is locked. A value of 1 indicates CDR loss of lock.

Table 19. EEPROM Serial ID Memory Contents – Transmitter Input Electrical Equalization Control (Address A2h, Byte 114).

Bit #	Status/Control Name	Description
7-4	TX EQ	Selects an input equalization value per Table 9-13 of SFF-8472
3-0	Reserved	

Table 20. Transmitter Input Equalization Control Values (Address A2h, Byte 114)

From Table 9-13 of SFF-8472

	Transmitter Input Equalization	
Code	**Nominal**	**Units**
11xx	Reserved	
1011	Reserved	
1010	10	dB
1001	9	dB
1000	8	dB
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	No Equalization

Table 21. EEPROM Serial ID Memory Contents – Receiver Output Electrical Emphasis Control (Address A2h, Byte 115).

Bit #	Status/Control Name	Description	Notes
7-4	RX EMPH	Selects an output emphasis value per Table 9-14 of SFF-8472	
3-0	Reserved		

Table 22. Receiver Output Emphasis Control Values (Address A2h, Byte 115)

From Table 9-14 of SFF-8472

	Receiver Output Emphasis At nominal Output Amplitude	
Code	**Nominal**	**Units**
1xxx	Vendor Specific	
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	No Emphasis

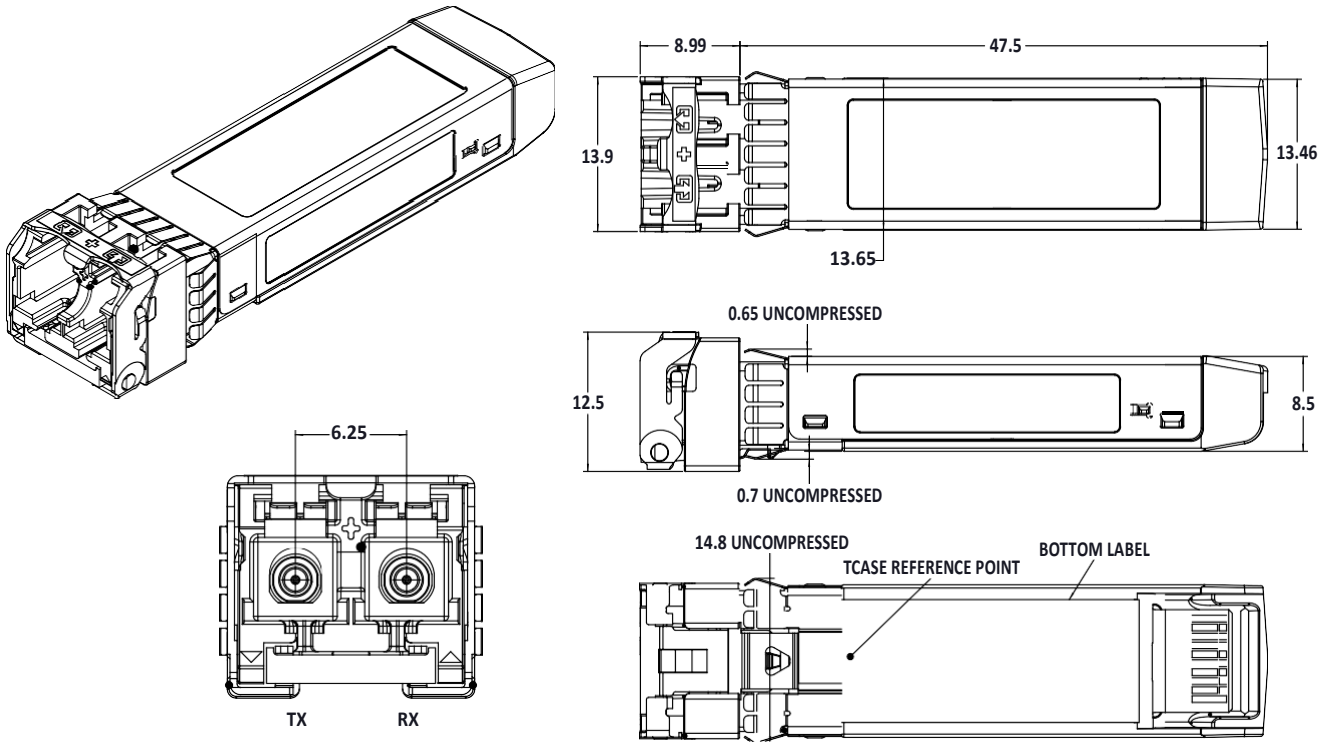
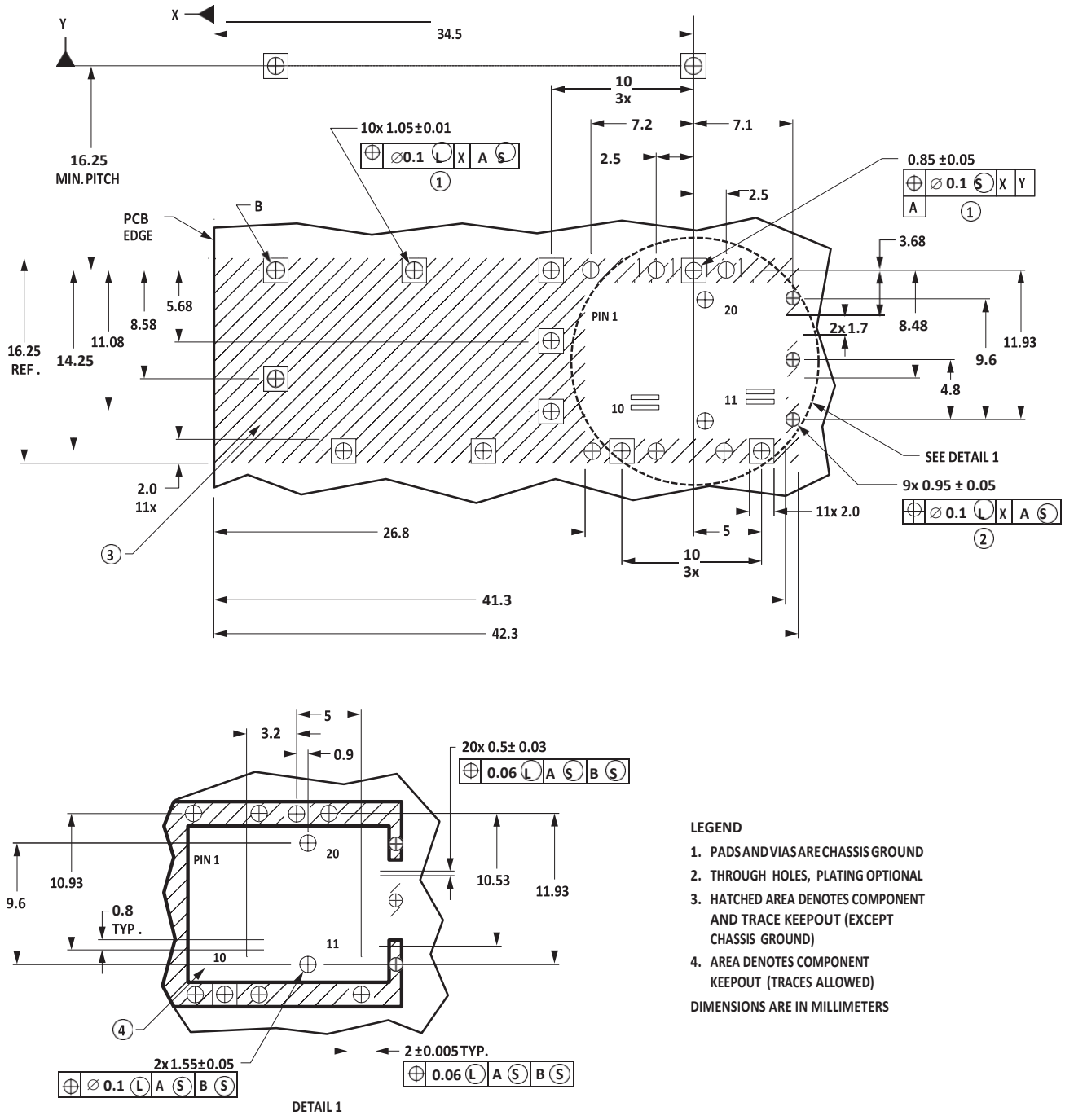


Figure 8. Module drawing

Figure 9. Module Label



LEGEND

1. PADS AND VIAS ARE CHASSIS GROUND
2. THROUGH HOLES, PLATING OPTIONAL
3. HATCHED AREA DENOTES COMPONENT AND TRACE KEEPOUT (EXCEPT CHASSIS GROUND)
4. AREA DENOTES COMPONENT KEEPOUT (TRACES ALLOWED)

DIMENSIONS ARE IN MILLIMETERS

Figure 10. SFP host board mechanical layout

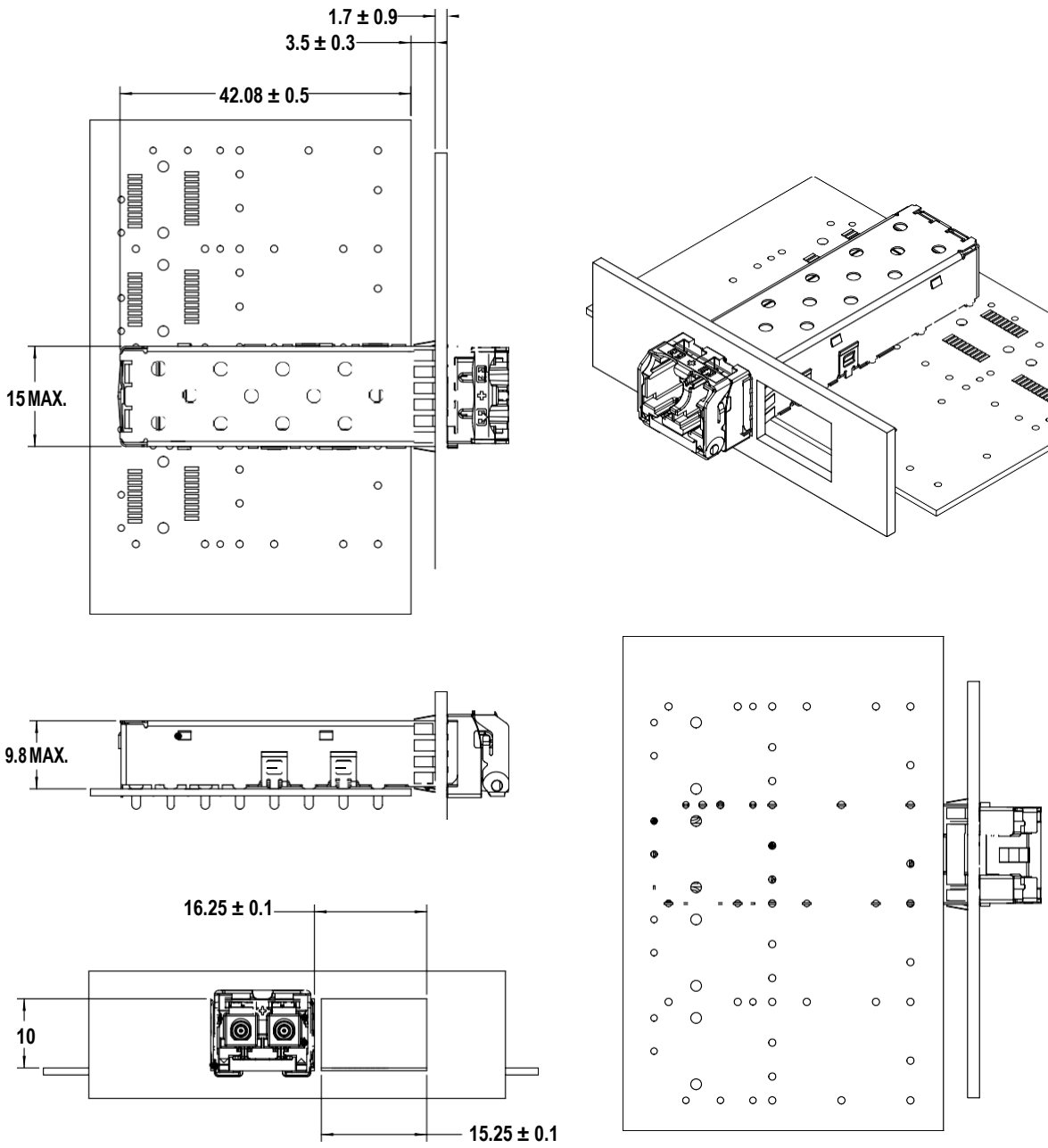


Figure 11. SFP Assembly drawing

Customer Manufacturing Processes

This module is pluggable and is not designed for aqueous wash, IR reflow, or wave soldering processes.

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