ExpressLane PEX 8548-AA
Quick Start Hardware Design Guide

Version 1.4

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Website: www.plxtech.com
Support: www.plxtech.com/support
Phone: 800 759-3735
408 774-9060
Fax: 408 774-2169

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Revision History

Date	Version	Comments
February 2, 2007	1.0	Initial release.
April 12, 2007	1.1	Revised Section 2. Added I2C_INTA_ENABLE# information to Section 9. Corrected the pull-up resistor value in Section 10. Added new Section 11, “PEX_INTA# and FATAL_ERR#,” and renumbered subsequent sections. Miscellaneous enhancements throughout document.
July 3, 2007	1.2	Added Link State error information to Section 11. Updated VDD10 and VDD10S current requirements in Section 12.1. Updated Data Book revision listed in Section 13. Added the *I²C Specification* to Section 13.
January 2, 2008	1.3	Added support for the PEX 8548S-AA switch. Updated Data Book name and revision listed in Section 13.
January 18, 2008	1.4	Removed all information pertaining to the PEX 8548S-AA switch – the device is no longer supported.

Introduction

This quick start hardware design guide is an overview of PLX Technology's ExpressLane™ PEX 8548 PCI Express Gen 1 Switch, and provides examples of how to connect to the various interfaces.

1 Interfaces

The PEX 8548 is a 48-lane, 9-port, 3-station PCI Express Gen 1 switch designed for high-availability, high-performance systems. The PEX 8548 signal interfaces are grouped into the following functional blocks:

- PCI Express Lanes running at 2.5 Gbps
- Hot Plug Controller interface signals for the three Hot Plug-capable ports
- Reference Clock input
- Fundamental Reset input
- Port Status Indicator signals
- Serial EEPROM Interface signals
- JTAG Interface signals
- I^2C Interface signals
- Strapping balls
- PEX_INTA# and FATAL_ERR# signals
- Power and Ground

Figure 1 illustrates the PEX 8548 external ball interface. The PEX 8548 has 48 PCI Express lanes, which run at a line rate of 2.5 Gbps. Each lane consists of both Transmit and Receive differential pairs (four physical signals).

The PEX 8548 allows multiple lanes to be logically grouped through Strapping balls or serial EEPROM configuration. These lanes constitute a common signal interface between two PCI Express ports (*that is*, a PCI Express link).

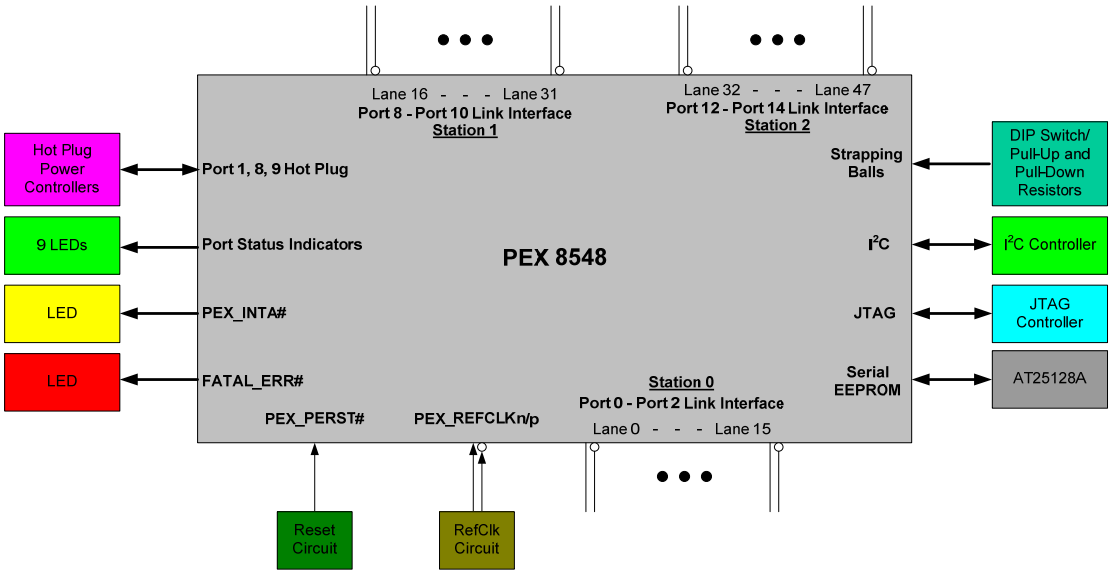

Figure 1. PEX 8548 Interfaces

2 PCI Express Interface

The PEX 8548 lanes are implemented using a SerDes I/O (Serializer/De-serializer). The PEX 8548 is compliant to the *PCI Express Base Specification, Revision 1.1*; therefore, the data rate of each transmitter is 2.5 Gbps and the bit time or unit interval is 400 ps. RefClk is used by the PEX 8548 to generate the PCI Express data rates. The rise and fall time of the transmitter is near 100 ps for transition bits; the knee frequency of the signal is approximately 3.5 GHz ($f_{3db} = 0.35/t_{rise}$). At these frequencies, PCB transmission lines behave as low-pass filters due to frequency-dependent dielectric and conductor losses. Ensure that the physical interconnect between devices produces as little signal loss and jitter as possible.

PCI Express serial links are differential, AC-coupled, transmission lines. Because differential transmission lines reject common mode noise, lay out the differential pairs so that differential noise across the two lines of a pair is minimized. AC-coupling capacitors are required on all transmitters, to isolate the DC component of a signal between a transmitter and receiver. PCI Express signal transmission utilizes 8b/10b encoding; therefore, the minimum frequency content of a signal is 125 MHz. To pass the required frequency components, the *PCI Express Base Specification, Revision 1.1*, requires that the AC-coupling capacitors be within the range of 75 to 200 nF. AC-coupling capacitor size and footprint dictate high-frequency cutoff due to inductance. It is recommended to use 0402- or 0603-size ceramic capacitors, to reduce inductance and impedance discontinuities.

2.1 Programmable De-Emphasis

The PEX 8548 provides a number of ways to optimize the SerDes drive characteristics, to aid in meeting application needs. Each SerDes drive contains a first-order equalization function, which allows for the de-emphasis of non-transition bits within a data pattern. The PEX 8548 provides two 32-bit registers (**SerDes Drive Equalization Level Select 1** and **SerDes Drive Equalization Level Select 2** registers, offsets 254h and 258h, respectively), partitioned into sixteen, 4-bit sub-registers (one per SerDes of each station). These registers allow the equalization ratio to be programmed through serial EEPROM loading or register writes. The default value, coming out of reset, is 8h, which sets non-transition bit de-emphasis to -3.35 dB. Equalization is intended to help reduce Inter Symbol Interference (ISI) and loss by providing a stronger drive for transition bits compared to non-transition bits. This aids in boosting the higher-frequency components of the transmitted data pattern, to counter the low-pass filter effects of FR4 transmission lines.

2.2 Programmable SerDes Drive Current

The PEX 8548 also provides a programmable drive current for each SerDes. The PEX 8548 provides a 32-bit register (**SerDes Nominal Drive Current Select** register, offset 248h) partitioned into 16, 2-bit sub-registers (one per SerDes of each station). These registers allow the drive's nominal current (I_{nom}) to be set at 10, 20, or 28 mA. The default value, coming out of power-on reset, is 00b (20 mA). This default value can be overwritten, by way of serial EEPROM load or through register Writes.

The actual drive current (I_{tx}) is a scaled multiple of the nominal current. The PEX 8548 provides two 32-bit registers (**SerDes Drive Current Level 1** and **SerDes Drive Current Level 2** registers, offsets 24Ch and 250h, respectively), partitioned into 16, 4-bit sub-registers (one per SerDes of each station). *For example*, the bits in register offset 24Ch[3:0] scale the drive current for Lane 0 (Station 0), Lane 16 (Station 1), and Lane 32 (Station 2). These register values set the actual-to-nominal current ratio. This register allows the actual current to be linearly scaled up to 135%, or scaled down to 60%, of the nominal. The default value, coming out of reset, is 0h (I_{tx}/I_{nom} = 1.00, or 100%). This feature can be used to reduce power consumption, in applications where the physical link is short, or boost drive current, for longer transmission lines. The transmitter's output voltage swing is determined by multiplying the fixed lane termination resistance of both the transmitter and receiver (25 ohms) by the actual drive current; hence, the voltage swing can be reduced by lowering the programmable drive current ($V_{TX\text{-}DIFFp} = I_{TX} * Z_T/2$).

Note: $V_{TX\text{-}DIFFp}$ is the single-ended voltage swing.

2.3 Adjustable VTT Settings

In addition to adjusting the drive current, the SerDes termination supply voltage (VTT_PEX[23:0]) can range from 1.35 to 1.8V. This supply voltage determines the drive's common mode voltage and limits the output voltage swing ($V_{TX\text{-}CM} = V_{TT} - V_{TX\text{-}DIFFp}$). The system designer should simulate their system designs to determine the best fit for their application. It is acceptable to tie all VTT_PEX*x* balls together.

2.4 PCI Express Layout Considerations

Differential signaling reduces the effects of common mode noise. When laying out differential pairs, take notice of the common mode return current path. If a signal pair transitions from one signal layer to another, ensure that there is a low-inductance path between the corresponding reference planes for the return current. If the signal is referencing a ground plane, and transitions through a via to another layer that references a different ground plane, provide a ground or "stitching" via (connecting the ground planes) near the signal via, to allow the return current to remain near the signals. BGA ball field ground connections and connector pin field ground connections provide ground vias for signals that change layers near those devices. Figure 2 illustrates how return currents can utilize stitching vias to change reference planes.

If a signal is referencing a DC power plane and changes layers to reference a DC ground plane, provide an AC return path by placing stitching capacitors near the signal transition points.

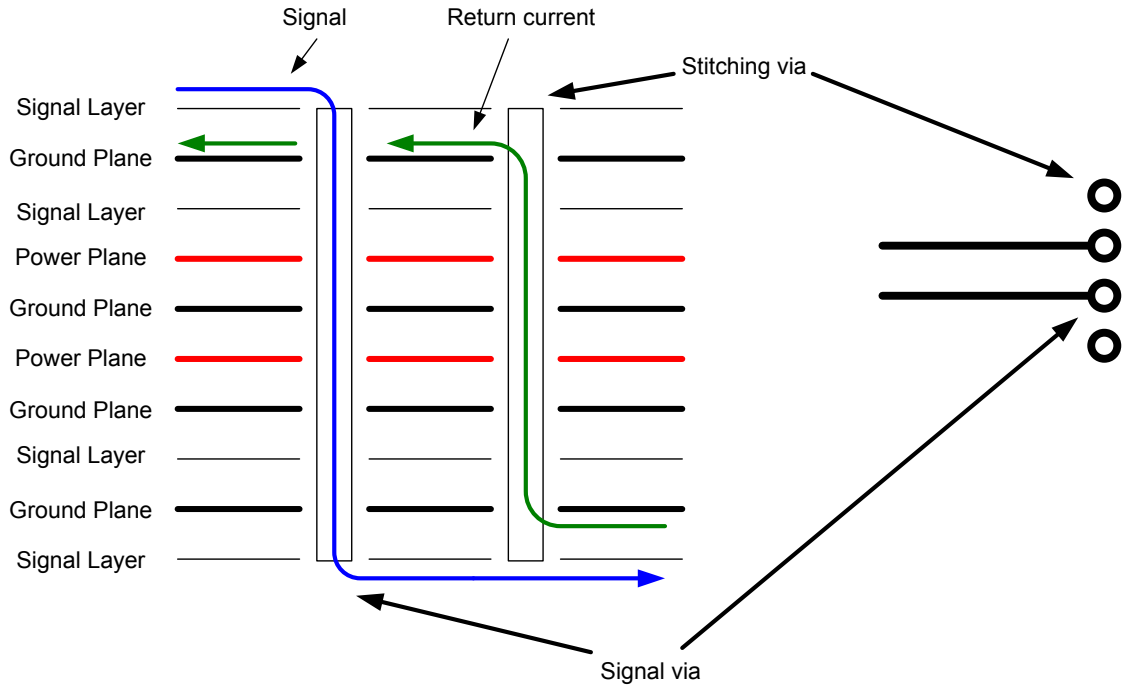

Figure 2. Return Current Path Utilizing Stitching Vias

3 Reference Clock (REFCLKn/p) Circuitry

PEX_REFCLKn/p is a differential Current Mode Logic (CML) Clock input that receives a 100-MHz (±300 ppm) clock source. The PEX_REFCLKn/p receiver input has an internal biasing circuit and integrated 110-ohm differential termination. The biasing circuit sets the receiver's common mode voltage to 0.65V. The PEX 8548 Reference Clock input must be AC-coupled, to isolate the drive and receiver DC common mode voltages. Capacitor values in the range of 75 to 200 nF are recommended. AC-coupling capacitor size and footprint dictate high-frequency cutoff due to inductance. It is recommended to use 0402- or 0201-size ceramic capacitors, to reduce inductance and impedance discontinuities.

A number of vendors provide PCI Express RefClk generators and buffers. Take care when selecting a synthesizer/buffer, because it must meet the PEX 8548 PEX_REFCLKn/p jitter requirements.

4 Fundamental Reset (PEX_PERST#) Circuitry

PEX_PERST# serves as a Fundamental Reset (Cold and Warm) to the PEX 8548. This signal is typically generated using a power-on reset circuit. The circuit can optionally have a manual reset capability, to generate a Warm Reset. Typical PCI Express applications, which provide a system-generated PERST# signal, hold the signal asserted for at least 100 ms after board power stabilizes. PEX_PERST# does not have internal de-bounce circuitry; therefore, guarantee that the signal maintains a smooth monotonic edge when it is asserted or de-asserted.

5 Port Status Indicators

The PEX 8548 provides a Port Status indicator signal for each PCI Express port on the device (PEX_PORT_GOOD[14:12, 10:8, 2:0]#). These signals are Active-Low and can be used to drive discrete LEDs, thereby providing a visual indicator of which ports are active. However, the signals do not provide information regarding the width of the active ports. *For example*, assume that the PEX 8548 switch's Port 0 is configured as a x4 PCI Express link, and the device at the other end of the link is x2. After link training completes, the link between the two devices will be x2. Although the width is not what was configured for Port 0, PEX_PORT_GOOD0# will assert, indicating that the link between the two devices is up. The actual width to which the PEX 8548's ports are configured can be read from the **Link Status and Control** register, offset 78h. The Port Good Output buffers can sink up to 8 mA; therefore, use either low-current LEDs, or size the series resistor to current limit the circuit.

6 Hot Plug Circuitry

The PEX 8548 has the capability to be a PCI Express Hot Plug Master on three downstream ports – Ports 1, 8, and 9. The Hot Plug interface (refer to Figure 3) on each of these three ports consists of nine signals (for a total of 27 signals):

- HP_ATNLED[9, 8, 1]#
- HP_BUTTON[9, 8, 1]#
- HP_CLKEN[9, 8, 1]#
- HP_MRL[9, 8, 1]#
- HP_PERST[9, 8, 1]#
- HP_PRSNT[9, 8, 1]#
- HP_PWREN[9, 8, 1]#
- HP_PWRFLT[9, 8, 1]#
- HP_PWRLED[9, 8, 1]#

The PEX 8548 Hot Plug Controller inputs have internal pull-up resistors on-chip (approximately 50K ohms); therefore, unused Hot Plug balls can remain unconnected. If an MRL (Manually operated Retention Latch) sensor is not present, tie HP_MRL*x*# to HP_PRSNT*x*#. If a Hot Plug-capable port is selected as the upstream port, the Hot Plug interface signals for that port are driven inactive – they are not floated. Many vendors, *such as* Intersil Corporation, Texas Instruments, and Micrel Semiconductor, provide PCI Express Hot Plug Power Controller solutions that can easily interface to a PEX 8548 Hot Plug Controller.

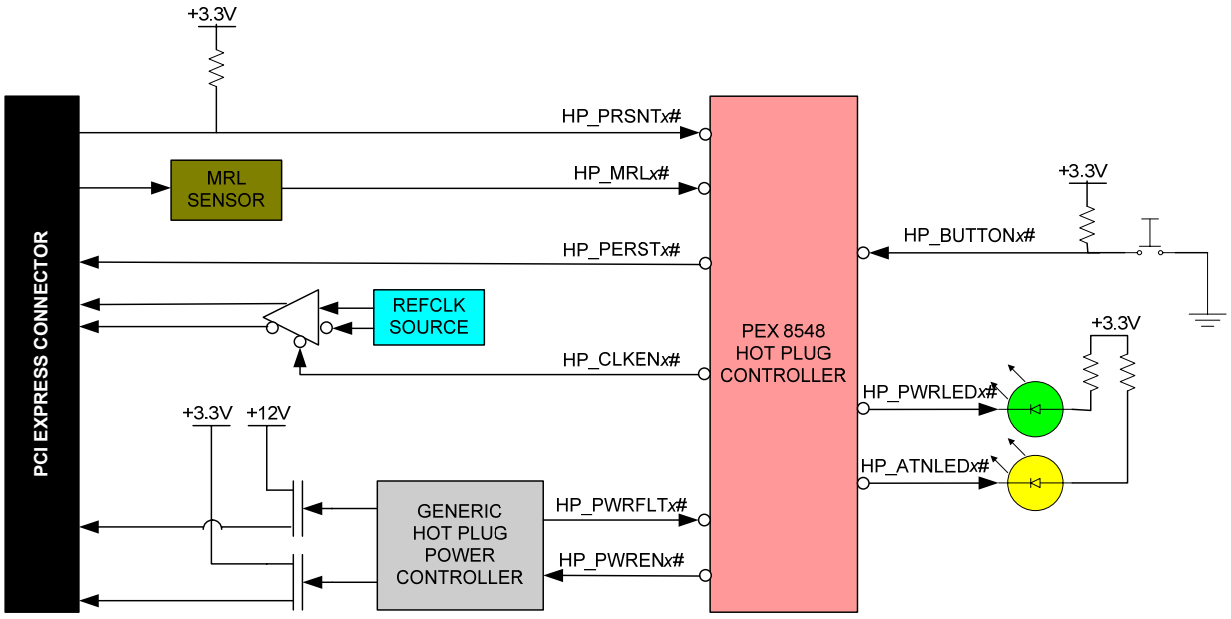

Figure 3. PEX 8548 Hot Plug Controller Interface

7 Serial EEPROM Interface

The PEX 8548 has an embedded SPI EEPROM Controller, which works with devices *such as* the Atmel AT25128A serial EEPROM. A 1-KB serial EEPROM is sufficient. (Refer to Figure 4.)

The PEX 8548 directly interfaces to the serial EEPROM. The PEX 8548 provides the 7.8-MHz Serial Clock (EE_SK), Chip Select (EE_CS#), and Data Input (EE_DI) for the serial EEPROM and receives Data Output (EE_DO) from the serial EEPROM. The PEX 8548 has a weak internal pull-up resistor (approximately 50K ohms) on the EE_DO signal, to restrain the serial EEPROM inputs/outputs from floating when not being actively driven. A stronger pull-up resistor (3K to 10K ohms) can be added on the EE_DO line.

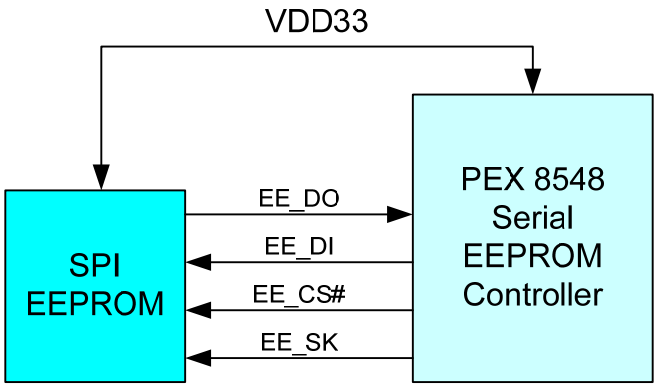

Figure 4. PEX 8548 SPI EEPROM Interface

8 JTAG Interface

The PEX 8548 supports a five-ball JTAG Boundary Scan interface, which consists of the following signals:

- JTAG_TCK
- JTAG_TDI
- JTAG_TDO
- JTAG_TMS
- JTAG_TRST#

At the board level, pull up JTAG_TCK, JTAG_TDI, and JTAG_TMS to VDD33 with 3K- to 10K-ohm resistors, and pull down JTAG_TRST# to VSS (GND) with a 3K- to 10K-ohm resistor. A 33-ohm series termination resistor can be added to JTAG_TDO, to improve signal quality. JTAG TCK can be pulled down if the system architecture requires it. Figure 5 illustrates a generic JTAG interconnection.

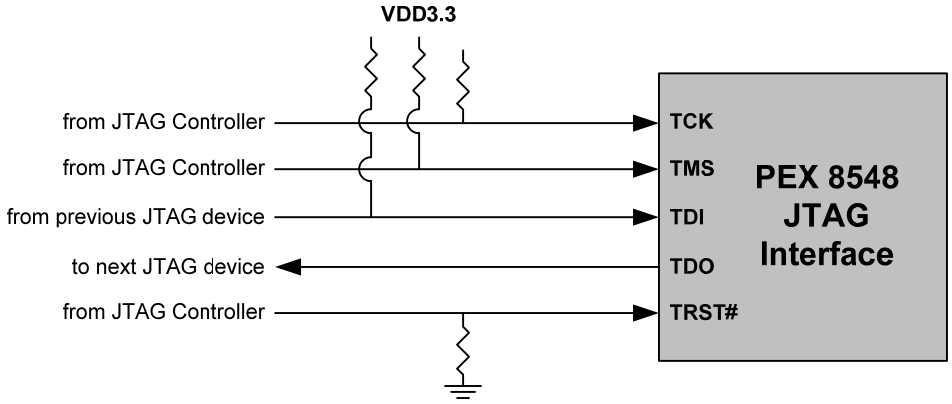

Figure 5. Generic JTAG Interface

9 I²C Interface

The PEX 8548 supports a five-ball I^2C interface when I2C_INTA_ENABLE# is strapped Low. The I^2C interface consists of the following signals:

- I2C_ADDR[2, 1, 0]
- I2C_SCL
- I2C_SDA

At the board level, pull up or pull down I2C_ADDR[2, 1, 0], to set the PEX 8548 I^2C Slave address. Also, I2C_SCL and I2C_SDA may require pull-up resistors, depending upon the system configuration. If required, the value of these resistors is dependent upon the I^2C Bus loading; however, a typical value is 2.26K ohms.

10 Configuration Strapping Balls

The PEX 8548 has a number of Configuration Strapping signals that allow configuration of various switch operating modes, by way of a hardware-only mechanism. All Configuration Strapping signals have a weak internal pull-up resistor (50K ohms), to restrain the undriven inputs from floating; however, it is recommended that a stronger external pull-up resistor value (3K to 10K ohms) be used on these lines.

Various PEX 8548 Strapping signal balls are for PLX ***Factory Test Only***; therefore, provide a means to disable the functionality of these balls. (Refer to Section 3.4.4, "Strapping Signals" in the *PEX 8548-AA Data Book*, for strapping requirements.)

11 PEX_INTA# and FATAL_ERR#

When I2C_INTA_ENABLE# is strapped High, PEX_INTA# is held Low. When I2C_INTA_ENABLE# is strapped Low, PEX_INTA# is an Open Drain output that is asserted when one or more Hot Plug, Link State, or Device-Specific errors occur. Refer to the *PEX 8548-AA Data Book* for details.

FATAL_ERR# is asserted Low when a Fatal error is detected in the PEX 8548.

12 Power Supplies, Sequencing, and De-Coupling

The PEX 8548 maximum power consumption could be as high as approximately 7W. Special cooling requirements may exist, depending upon the system environment. Refer to the *PEX 8548-AA Data Book*.

12.1 Power Supplies

The PEX 8548 has the following Power ball groups:

- VDD10 – Digital core logic supply
- VDD10A – SerDes analog supply used for PLLs, biasing circuitry, and PEX_REFCLK Input buffer
- VDD10S – SerDes digital supply
- VDD33 – I^2C, PEX Hot Plug, serial EEPROM, JTAG, Strapping signals, Port Status indicators
- VDD33A – PEX_REFCLK PLL supply
- VTT_PEX – SerDes Transmitter termination supply

At the board level, VDD10 and VDD10S can share a common 1.0V power plane. The current demands for these supplies are relatively high (approximately 1.81A for VDD10 and 2.58A for VDD10S); therefore, ensure that the power plane is sufficiently sized, to support the specified operating current. For best performance, the 1.0V plane must have an adjacent ground plane that provides an interplane capacitor to supply high-frequency transient currents. Provide a sufficient number of discrete capacitors for mid- and low-frequency de-coupling. Ceramic capacitors, ranging from 0.001 to 0.1 µF, and larger tantalum capacitors, ranging from 10 to 22 µF, should be used for this supply rail.

VDD10A has a lower noise tolerance than the digital supplies. Therefore, VDD10A might require additional filtering, depending upon the 1.0V power plane noise. For frequency components less than 600 kHz, VDD10A can tolerate noise levels up to 100 mVp-p. Between the frequency range 600 kHz to 320 MHz, the noise level must be less than 50 mVp-p. For frequency components above 320 MHz, VDD10A can tolerate noise up to 100 mVp-p. Ensure that the VDD10A Power balls do not share vias with other 1.0V Power balls routed to the power plane.

VDD33 power is used for single-ended I/O buffers. These buffers drive LED indicators, as well as the various out-of-band communication interfaces (*that is*, the serial EEPROM, Strapping signals, JTAG, and I^2C). As such, they are low-speed and low-power.

VDD33A and VSSA_PLL are used to power the internal Reference Clock PLL. This ball might require additional filtering circuitry if the VDD33 plane is experiencing significant noise. VDD33A can tolerate ripple from -100 to +100 mV, for frequencies above 10 MHz. If additional filtering circuitry is necessary, a wide trace (0.254 to 0.381 mm; 0.010 to 0.015 inches) can be used to power this supply ball. Use a 0-ohm resistor (0603 or 0805) in series with the main VDD33 supply, along with one or more 0.1 and/or 0.01 µF capacitors after the resistor, near the ball. If the VDD33 plane couples significant noise into the VDD33A supply, exchange the resistor for a ferrite bead, to aid in filtering the supply noise. In designs where VDD33A ties directly to the VDD33 power plane, ensure that VDD33A has its own dedicated via to the plane. Similarly, allow VSSA_PLL to have its own dedicated via to the main ground plane.

Note: *Placing ferrite beads in a power supply path is not a preferred method of filtering noise for supply rails. Power supplies isolated through the use of ferrite beads typically have limited access to interplane capacitance, which might have an adverse effect on a given supply rail.*

The VTT_PEX[23:0] balls are used to set the SerDes transmitter pair's common mode voltage, and limit the output swing. The allowable voltage range is from 1.35 to 1.8V. This voltage controls the maximum allowable $V_{TX\text{-}DIFFp}$ for the PCI Express transmitters. Refer to the *PEX 8548-AA Data Book* for further details. It is acceptable to tie the VTT_PEX*x* balls together.

12.2 Power Sequencing

For reliable operation, the VDD10, VDD10S, and VDD10A supplies should power-up first and power-down last. No specific sequence is required between the VTT_PEX, VDD33, and VDD33A supplies. All supply rails should power-up within 50 ms of one another.

12.3 Board-Level De-Coupling

Board-level power supply de-coupling exists primarily in two forms:

- Parallel plane capacitance
- Use of discrete capacitors

Parallel plane capacitance exists between a PCB's DC power and ground planes. PCB reference planes have a small amount of series inductance; therefore, their effective frequency range is much higher than that of discrete capacitors. Low-valued discrete capacitors can typically be effective for frequencies up to 250 MHz. For frequency components higher than 250 MHz, plane capacitance provides the only effective means for de-coupling. Figure 6 illustrates attenuation curves measured for the PEX 8548 emulation board. Above approximately 200 MHz, attenuation is provided only by board capacitance. Design the system such that power-rail signal attenuation, from 100 kHz to approximately 200 MHz, is 55 dBm or greater.

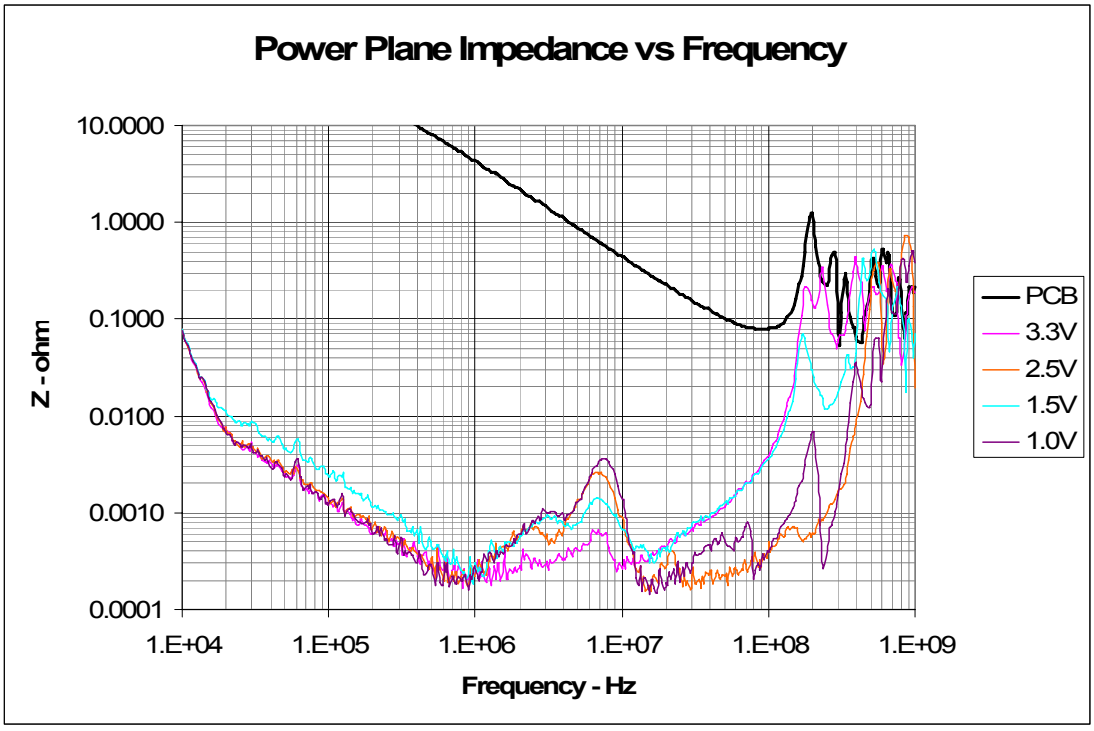

Figure 6. Power Plane Impedance Versus Frequency

A power and ground plane separation of 0.254 mm (0.010 inches) results in approximately 100 pF/in^2, while a separation of 0.102 mm (0.004 inches) provides approximately 200 pF/in^2. Plane capacitors provide other important benefits, *such as* a low-impedance path for AC return currents, in cases where a given reference plane has a discontinuity.

As for discrete capacitors, the footprint and physical size of discrete capacitors has a significant effect on the frequencies in which the capacitors provide effective de-coupling. To minimize series inductance, use smaller-packaged ceramic capacitors (*such as* 0402 or 0603) for mid-ranged frequency de-coupling (20 to 250 MHz). Use a mixed selection of capacitor values, *such as* 0.1 and 0.01 µF, to lower the impedance across a wide frequency range.

A combination of tantalum and ceramic capacitors can be used, to provide power de-coupling at frequencies less than 200 MHz. Capacitor footprint layout is important, because it can minimize the series inductance from pad to plane. Figure 7 illustrates examples of how various footprints for 0603-size capacitors can change series inductance. Power plane inductance is quite low; therefore, the proximity of higher-value capacitors ($\geq$ 1 µF) to the PEX 8548 is not critical. (Refer to *Right the First Time: A Practical Handbook on High Speed PCB and System Design,* by Lee Ritchie.)

Avoid adding trace segments from the capacitor pads to the vias. These segments add more series inductance, thereby lowering the discrete capacitor LC resonant frequency. If a plane capacitor is used, the placement of small discrete capacitors is not critical. Place the capacitors on the solder side of the board, under the BGA footprint (in the solder ball void area) and directly outside the BGA matrix. If a plane capacitor is not possible (this is typically the case for 4- and 6-layer boards), place the capacitors as close to the balls as possible. If a PCB layer stackup is such that plane capacitors are not possible, add power or ground fill areas on the signal layers, as follows:

- If a signal layer is referencing a DC ground plane, fill with power
- If a signal layer is referencing a DC power plane, fill with ground

These copper fill areas tie to the main power and ground planes, through the component balls.

Use tantalum capacitors (*such as* 10 to 22 µF) for bulk de-coupling of lower-frequency components. The proximity of these capacitors is not critical; therefore, they can be placed outside the BGA matrix.

It is strongly recommended to measure the attenuation versus frequency profile of each power rail on a completed board that is loaded only with bypass capacitors. This serves to confirm that there are no attenuation holes in the power-de-coupling design.

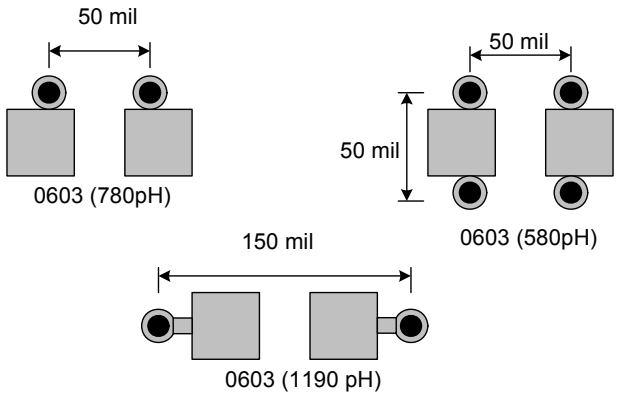

Figure 7. Capacitor Footprint Effects on Series Inductance

13 References

The following is a list of documentation to provide further details.

- PLX Technology, Inc.
  870 W Maude Avenue, Sunnyvale, CA 94085 USA
  Tel: 800 759-3735 (domestic only) or 408 774-9060, Fax: 408 774-2169, www.plxtech.com
  - *PEX 8548-AA Data Book, Version 1.5* or higher
- PCI Special Interest Group (PCI-SIG)
  3855 SW 153rd Drive, Beaverton, OR 97006 USA
  Tel: 503 619-0569, Fax: 503 644-6708, www.pcisig.com
  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI Bus Power Management Interface Specification, Revision 1.2*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2*
  - *PCI Express Base Specification, Revision 1.1*
  - *PCI Express Card Electromechanical (CEM) Specification, Revisions 1.0a and 1.1*
- *NXP Semiconductors*
  www.standardics.nxp.com
  - *The I2C-Bus Specification, Version 2.1*
- *Right the First Time: A Practical Handbook on High Speed PCB and System Design*, by Lee Ritchie