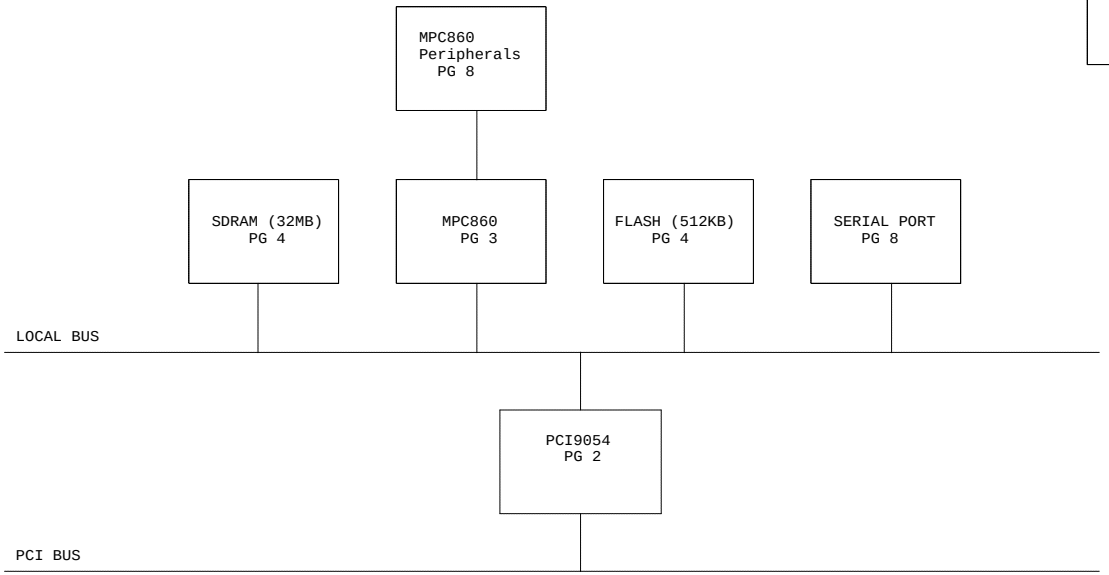
PCI9054RDK-860 BLOCK DIAGRAM

ECN HISTORY

ECN NUMBER	DATE	NOTE
xxx-xxx	04/30/98	1. BDM signals added: R60, R61, R62, and R63 to include VFLS[1:0] and FRZ to the BDM connector. 2. Added pull up to D11 and D12: R64, R65, R66, R67, U29, and U30.
xxx-xxx	06/22/98	1. SDRAM: added ADDR MUX(U31,U32,U33): Changed MA[0:11] to SDRAM, Added R68 and R69 for A7 and A8. Changed WE#(GPL_A1#). 2. FLASH: Added 3.3V or 5V(VCC) PS Option. Changed WE#(BS_B0#). 3. SRAM: added BDIP# signal to the glue. 4. Power UP config: added D7,D9,D10 (U34,U35,U36) for the power up configurations. 5. Changed the PU/PD (R)s for the Power Up Configurations. 6. Added PU/PD (R)s for the MPC860 JTAG Port.
xxx-xxx	07/02/98	Added R78 & R79 (Wait control input to UPM)
xxx-xxx	08/08/98	1. Removed SRAM: Lattice and SRAMs. 2. Changed R5 to 1K (EEDI/O pull down R). 3. Added Pull-Up Resistor(510 ohm) for BB#. 4. Added Pull-Down Resistor for TCK and TRST#(1K ohm). 5. Fixed SDRAM address MUX unit.
xxx-xxx	08/21/98	1. TSIZ0 (pin 92) and TSIZ1 (pin 91) were swapped.
xxx-xxx	6/25/02	1. Correct pull-up resistor at U1-166. It was R81, now is R83 2. Update BOM to reflect PCB board Rev 90-0002-300-A, and Document Number

NOTE: (otherwise specified)
1. All resistors are EIA case style 0805, 5% tolerance.
2. All .1uF caps are EIA case style 0805, 10% tolerance.
3. All 0K0 resistors are 1210 type and less than 0.01 ohms

(*** indicates default, do not install other)



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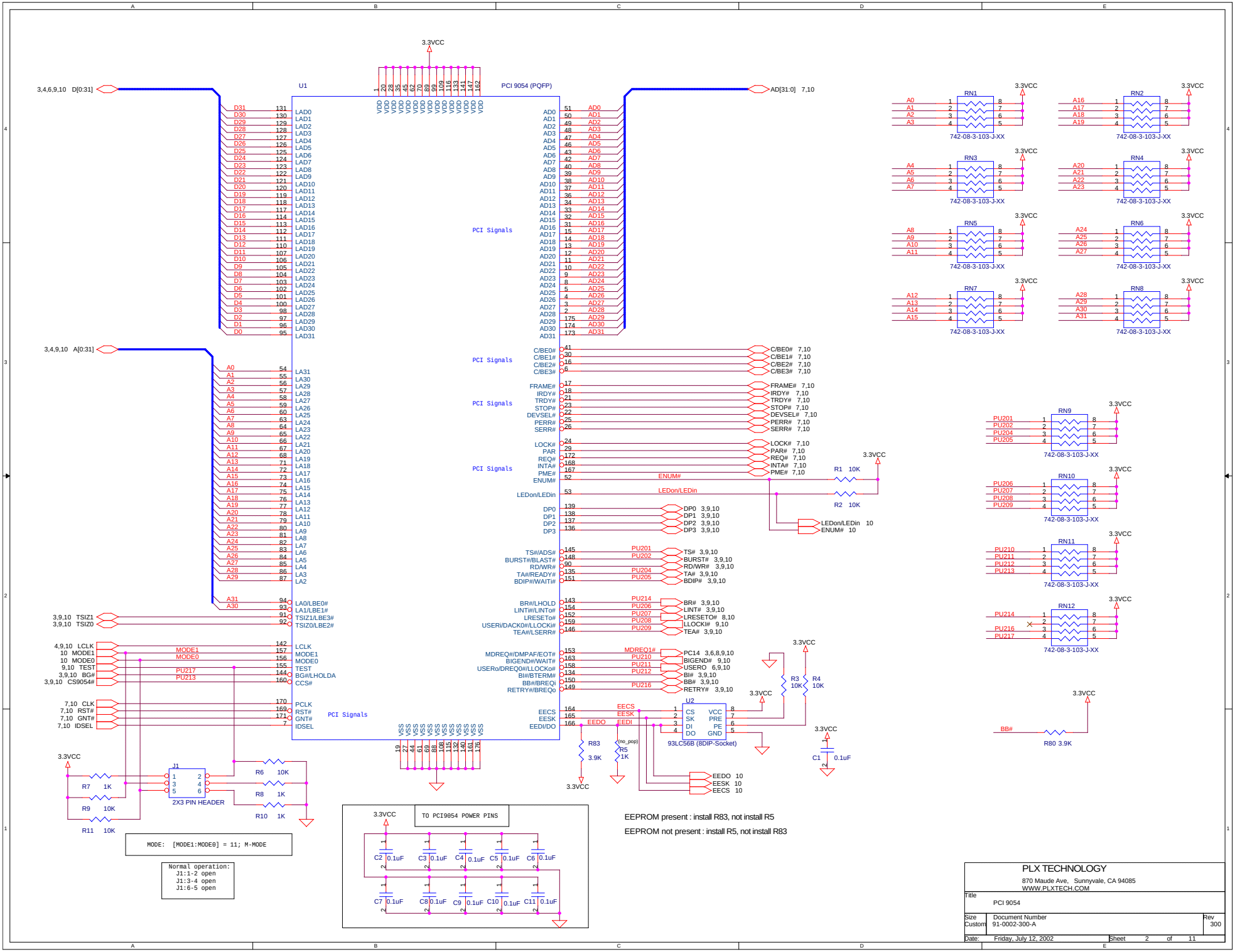
U1
PCI 9054 (PQFP)
3.3VCC
3,4,6,9,10 D[0:31]
AD[31:0] 7,10
3,4,9,10 A[0:31]
PCI Signals
LAD0
LAD1
LAD2
LAD3
LAD4
LAD5
LAD6
LAD7
LAD8
LAD9
LAD10
LAD11
LAD12
LAD13
LAD14
LAD15
LAD16
LAD17
LAD18
LAD19
LAD20
LAD21
LAD22
LAD23
LAD24
LAD25
LAD26
LAD27
LAD28
LAD29
LAD30
LAD31
LA31
LA30
LA29
LA28
LA27
LA26
LA25
LA24
LA23
LA22
LA21
LA20
LA19
LA18
LA17
LA16
LA15
LA14
LA13
LA12
LA11
LA10
LA9
LA8
LA7
LA6
LA5
LA4
LA3
LA2
LA0/LBE0#
LA1/LBE1#
TSIZ1/LBE3#
TSIZ0/LBE2#
LCLK
MODE1
MODE0
TEST
BG#/LHOLDA
CCS#
PCLK
RST#
GNT#
IDSEL
C/BE0#
C/BE1#
C/BE2#
C/BE3#
FRAME#
IRDY#
TRDY#
STOP#
DEVSEL#
PERR#
SERR#
LOCK#
PAR
REQ#
INTA#
PME#
ENUM#
LEDon/LEDin
DP0
DP1
DP2
DP3
TS#/ADS#
BURST#/BLAST#
RD/WR#
TA#/READY#
BDIP#/WAIT#
BR#/LHOLD
LINT#/LINTo#
LRESETo#
USERi/DACK0#/LLOCKi#
TEA#/LSERR#
MDREQ#/DMPAF/EOT#
BIGEND#/WAIT#
USERo/DREQ0#/LLOCKo#
BI#/BTERM#
BB#/BREQi
RETRY#/BREQo
EECS
EESK
EEDI/DO
VSS
VDD
RN1
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
RN10
RN11
RN12
742-08-3-103-J-XX
R1 10K
R2 10K
R3 10K
R4 10K
R5 1K
R6 10K
R7 1K
R8 1K
R9 10K
R10 1K
R11 10K
R80 3.9K
R83 3.9K
C1 0.1uF
C2 0.1uF
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
U2
93LC56B (8DIP-Socket)
CS
SK
DI
DO
VCC
PRE
PE
GND
J1
2X3 PIN HEADER
(no_pop)
TO PCI9054 POWER PINS
MODE: [MODE1:MODE0] = 11; M-MODE
Normal operation:
J1:1-2 open
J1:3-4 open
J1:6-5 open
EEPROM present : install R83, not install R5
EEPROM not present : install R5, not install R83
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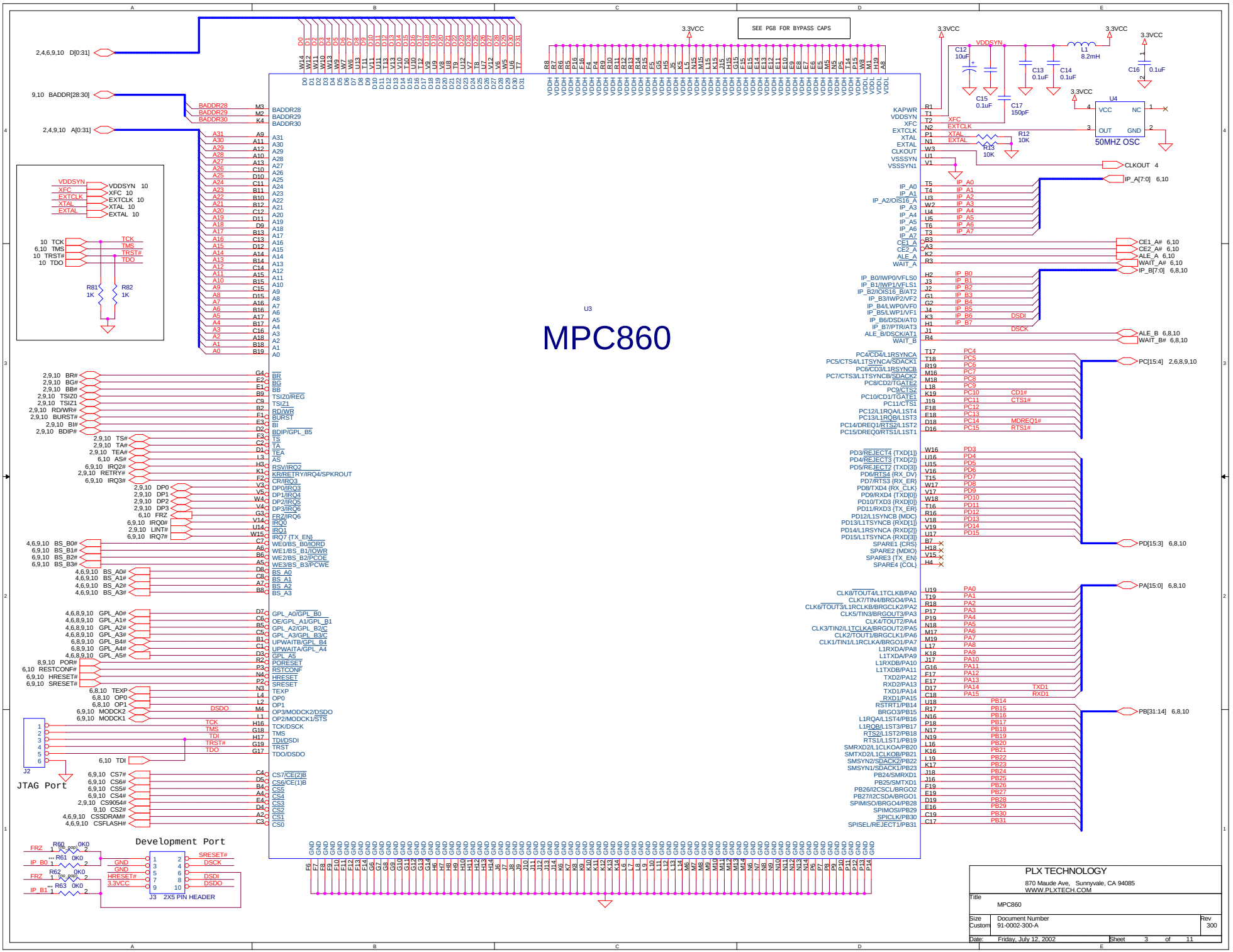
MPC860
U3
SEE PG8 FOR BYPASS CAPS
3.3VCC
JTAG Port
J2
Development Port
J3 2X5 PIN HEADER
50MHZ OSC
U4
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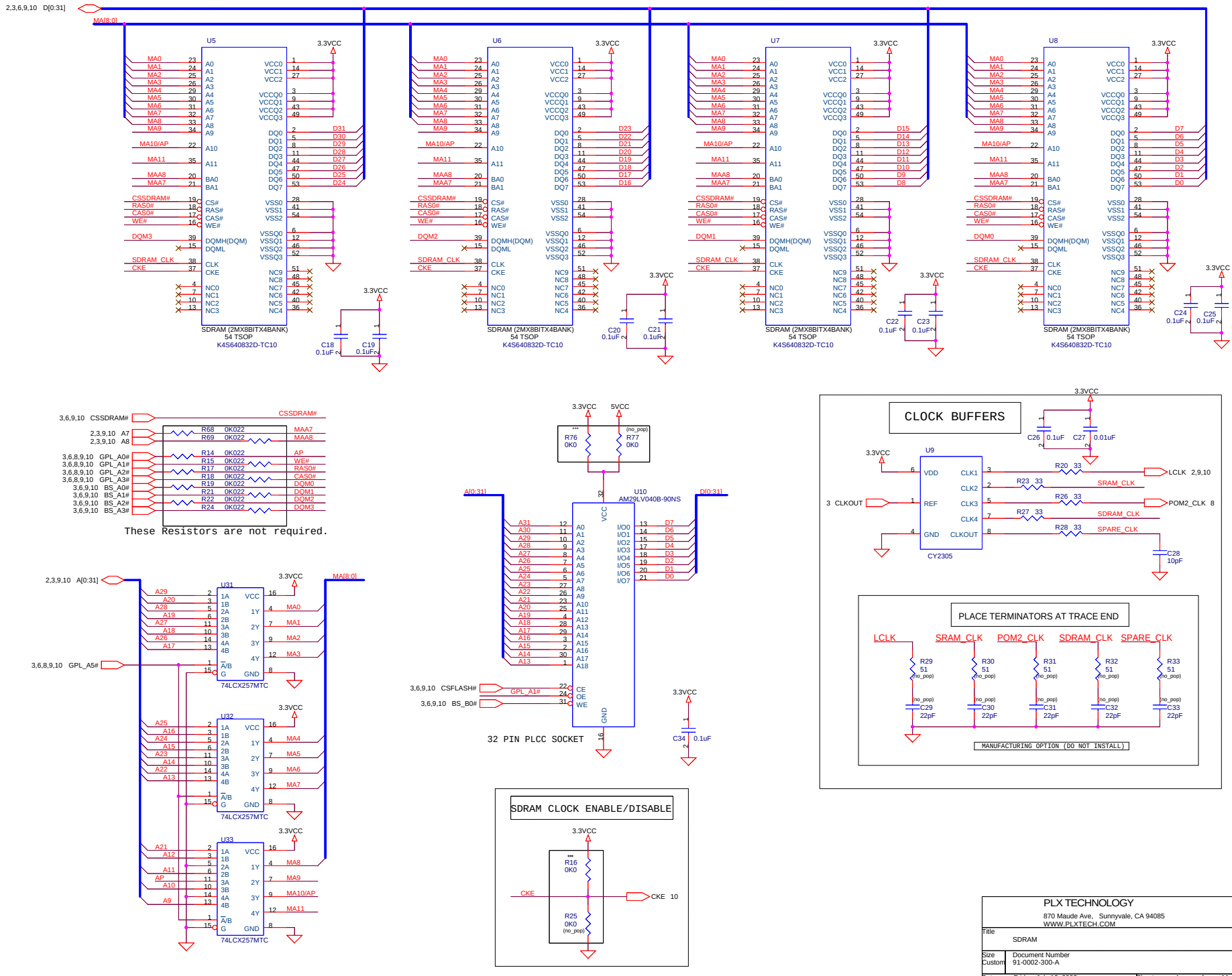
2,3,6,9,10 D[0:31]
MA[8:0]
U5
U6
U7
U8
3.3VCC
SDRAM (2MX8BITX4BANK)
54 TSOP
K4S640832D-TC10
C18 0.1uF
C19 0.1uF
C20 0.1uF
C21 0.1uF
C22 0.1uF
C23 0.1uF
C24 0.1uF
C25 0.1uF
3,6,9,10 CSSDRAM#
2,3,9,10 A7
2,3,9,10 A8
3,6,8,9,10 GPL_A0#
3,6,8,9,10 GPL_A1#
3,6,8,9,10 GPL_A2#
3,6,8,9,10 GPL_A3#
3,6,9,10 BS_A0#
3,6,9,10 BS_A1#
3,6,9,10 BS_A2#
3,6,9,10 BS_A3#
These Resistors are not required.
5VCC
U10
AM29LV040B-90NS
32 PIN PLCC SOCKET
3,6,9,10 CSFLASH#
3,6,9,10 BS_B0#
GPL_A1#
2,3,9,10 A[0:31]
3,6,8,9,10 GPL_A5#
U31
U32
U33
74LCX257MTC
SDRAM CLOCK ENABLE/DISABLE
CKE
CKE 10
CLOCK BUFFERS
U9
CY2305
3 CLKOUT
LCLK 2,9,10
POM2_CLK 8
SRAM_CLK
SDRAM_CLK
SPARE_CLK
PLACE TERMINATORS AT TRACE END
LCLK
SRAM_CLK
POM2_CLK
SDRAM_CLK
SPARE_CLK
MANUFACTURING OPTION (DO NOT INSTALL)
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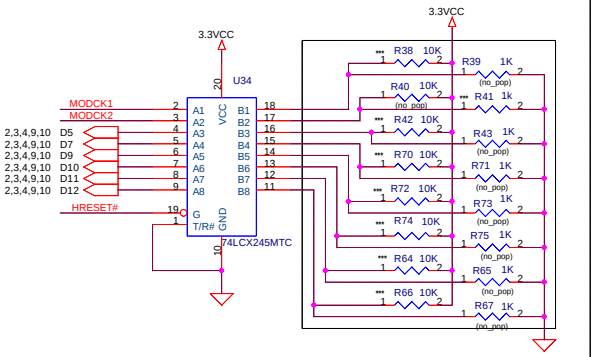
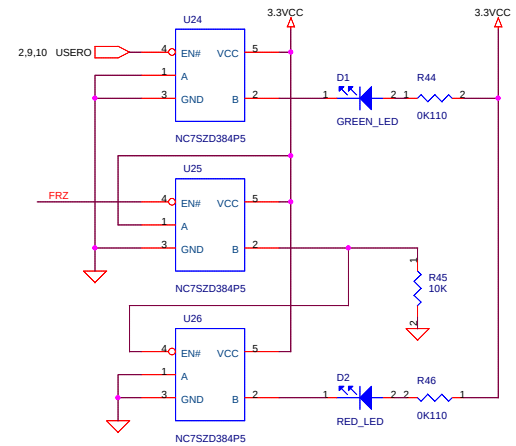
Power Up Configuration

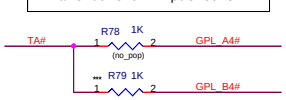
OSC (f)	MODCK1	MODCK2
4Mhz OSC	1	1
50Mhz OSC	1	0

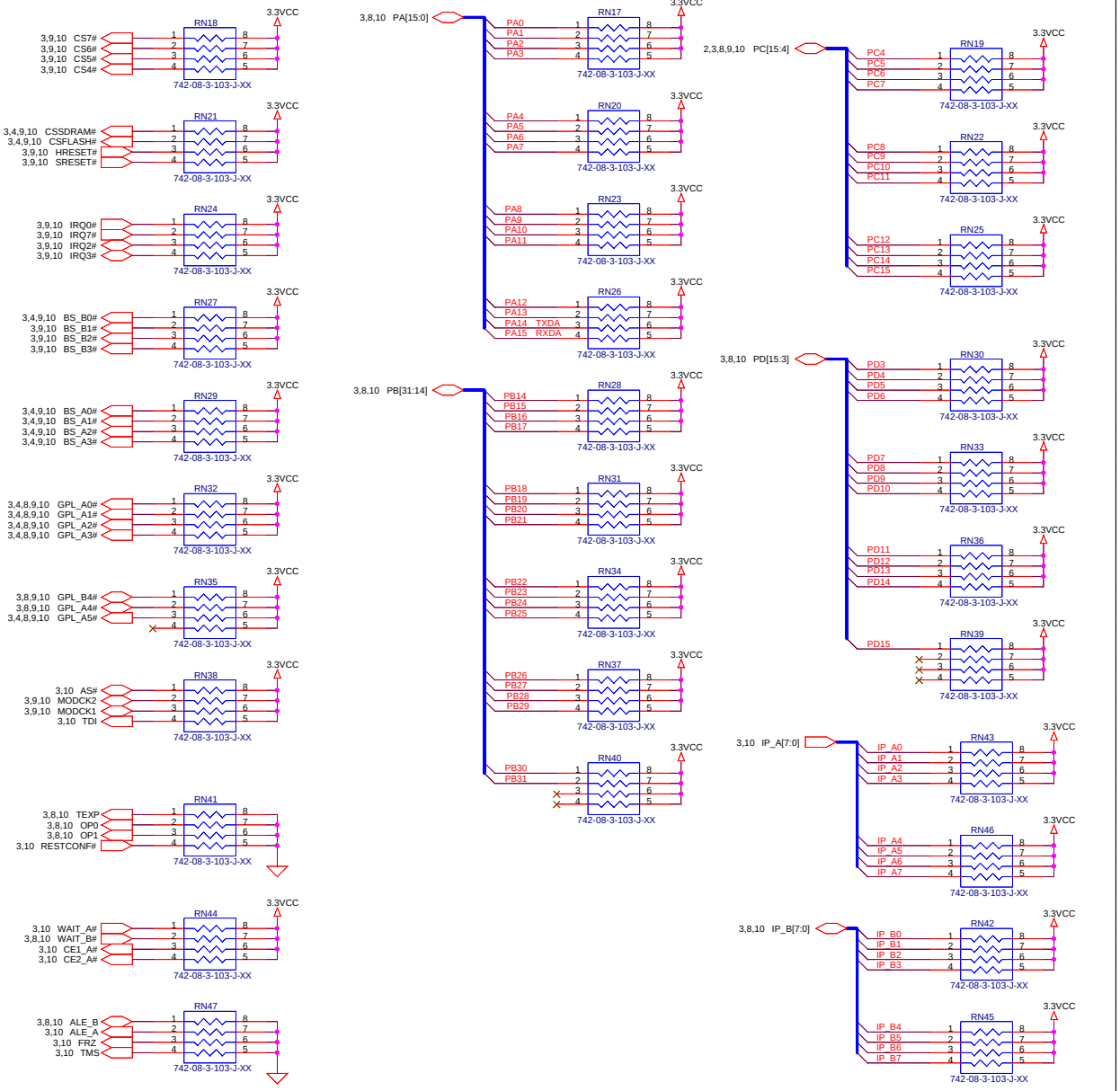


Indicator LEDs



Wait Control Input to UPM





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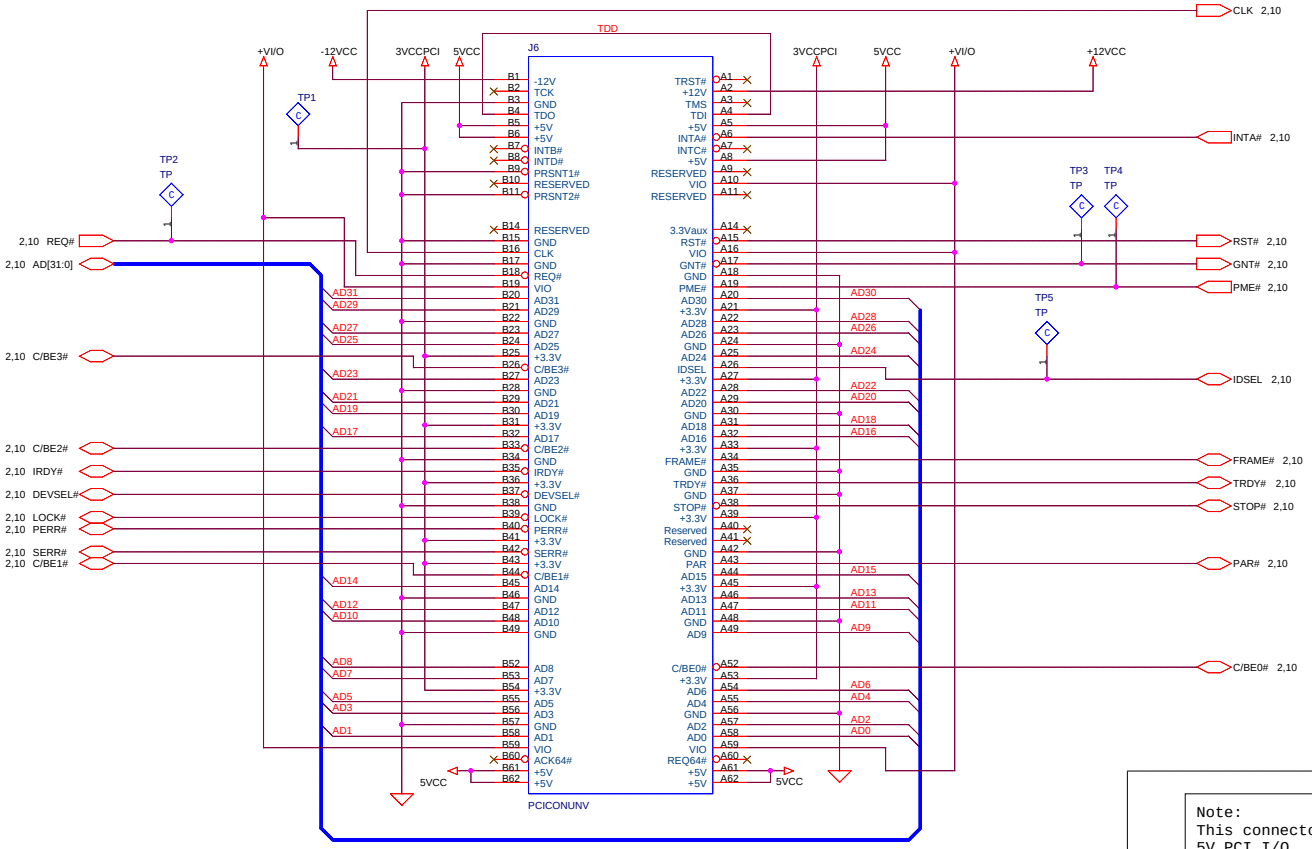
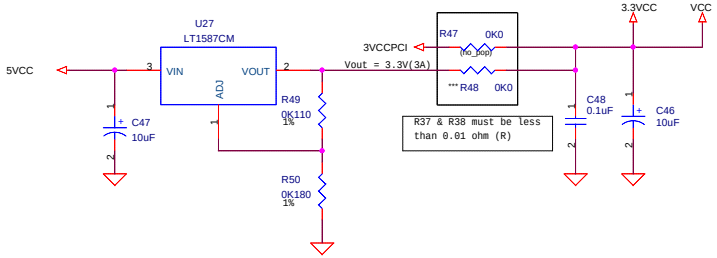
PCI Edge Connector



Local Bus Power Source



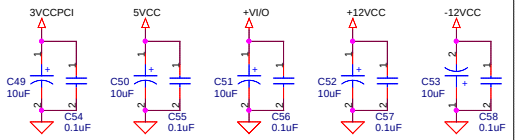
U27 option:
1. If LT1587CM (adjustable) is used, install R49 and R50 (default).
2. If LT1587CM-3.3 is used, do not install R49 and replace R50 with a jumper.

Local Bus 3.3VCC is selectable at manufacturing (R47 or R48):
Populate R47 if using 3.3V supply from the PCI connector
Populate R48 if using 3.3V supply from the Voltage regulator (default)

Note:
This connector is keyed for both 3.3V and 5V PCI I/O

Each power supply group pins must be tied together and have bypass capacitors (+5V, +12V,-12V, and +3.3V).

Each power group has .1uF and 10uF caps.



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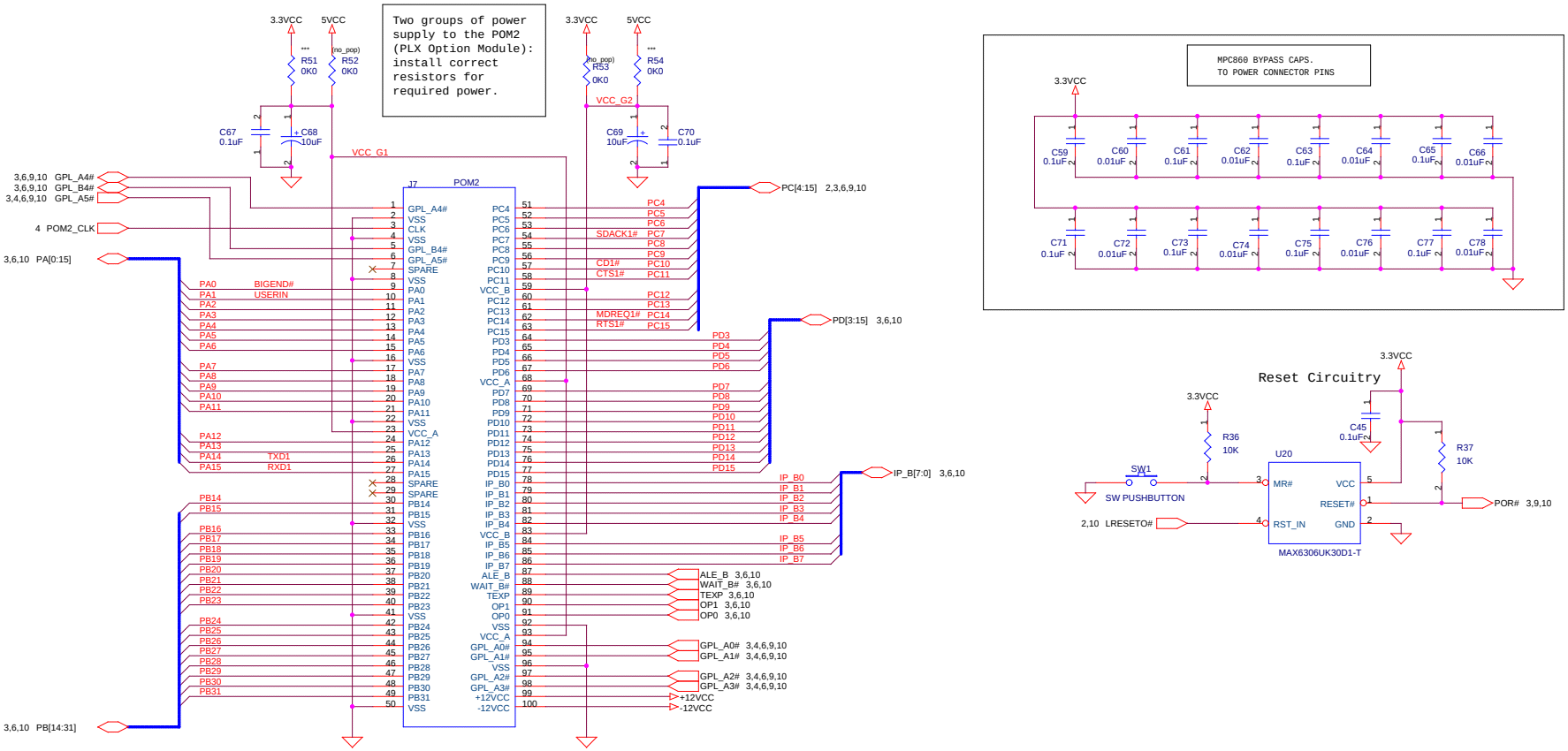

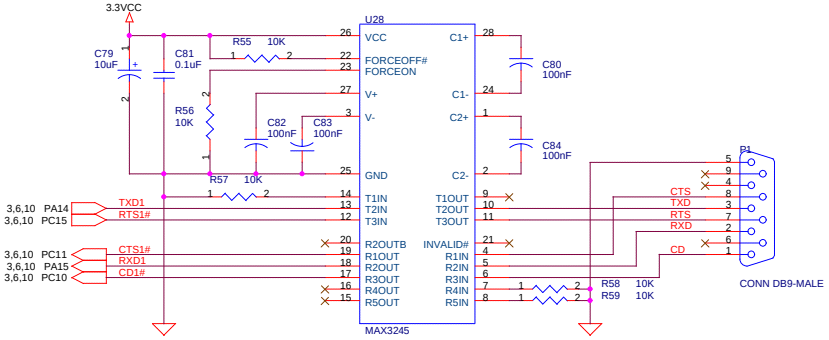

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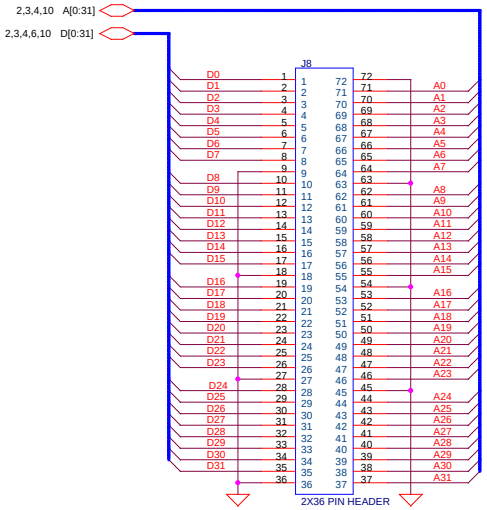
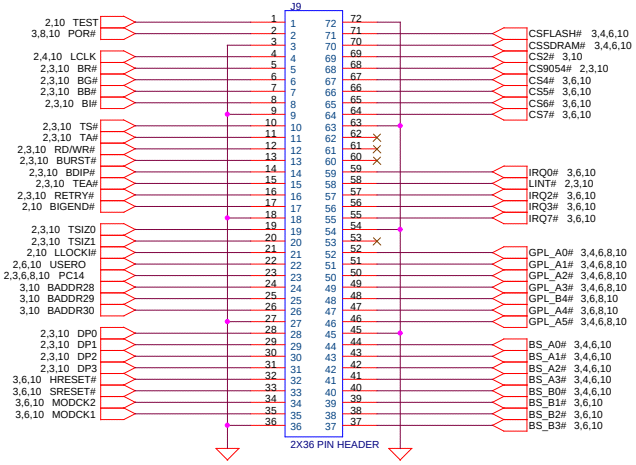
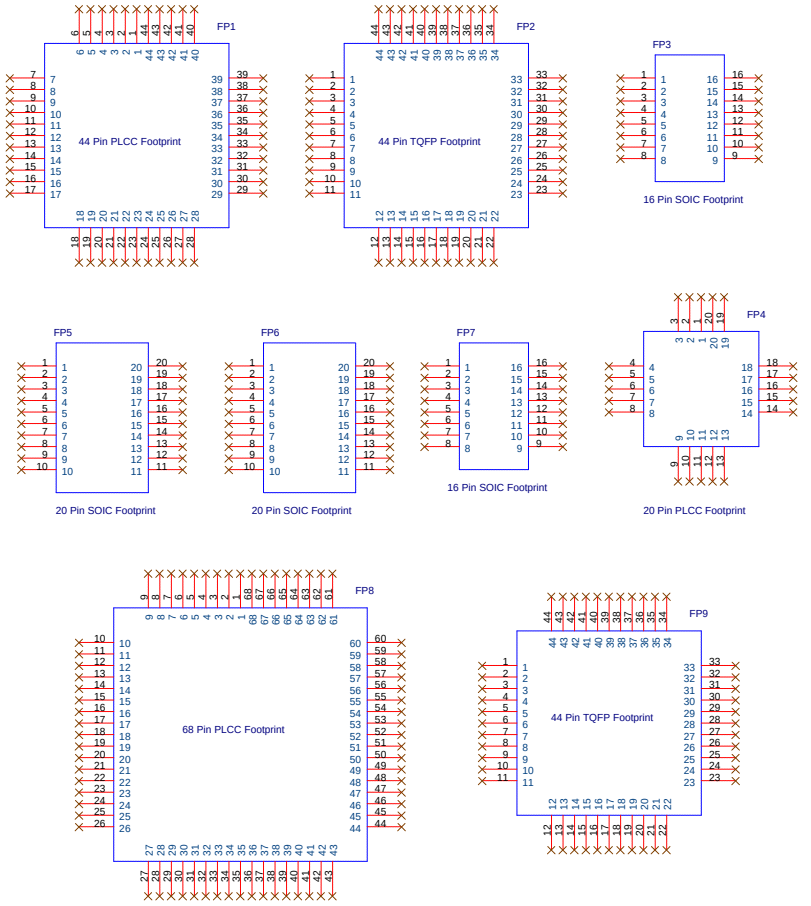




Prototyping Footprints

Note: Place the 3 PLCC devices co-incident on the board; that is, they share common pins and the 20 fits inside the 44 which fits inside the 68.



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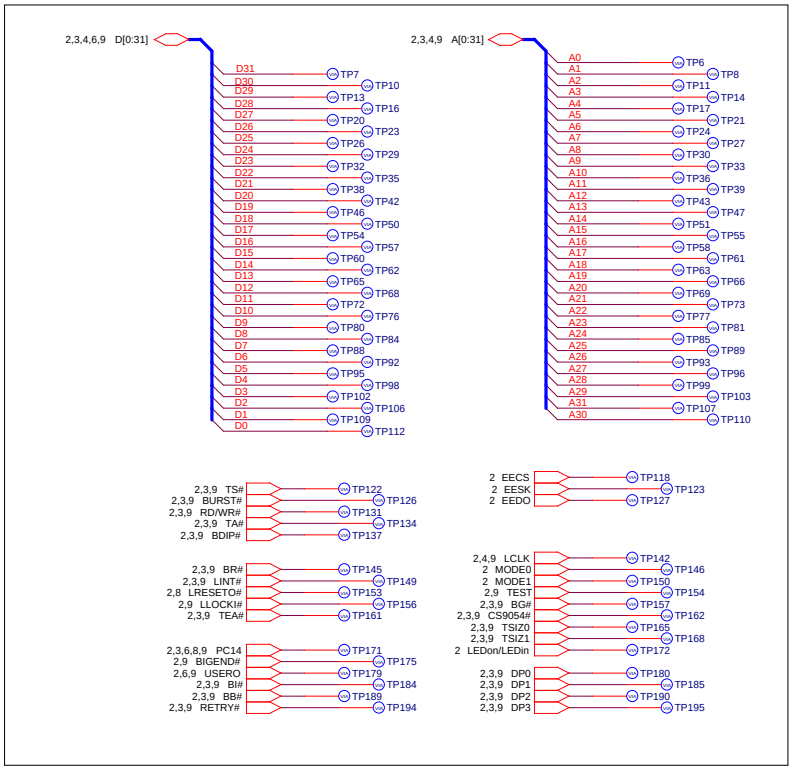

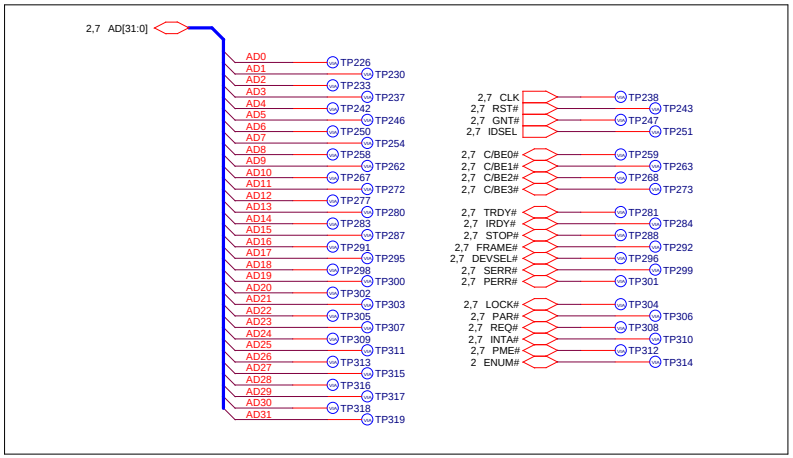

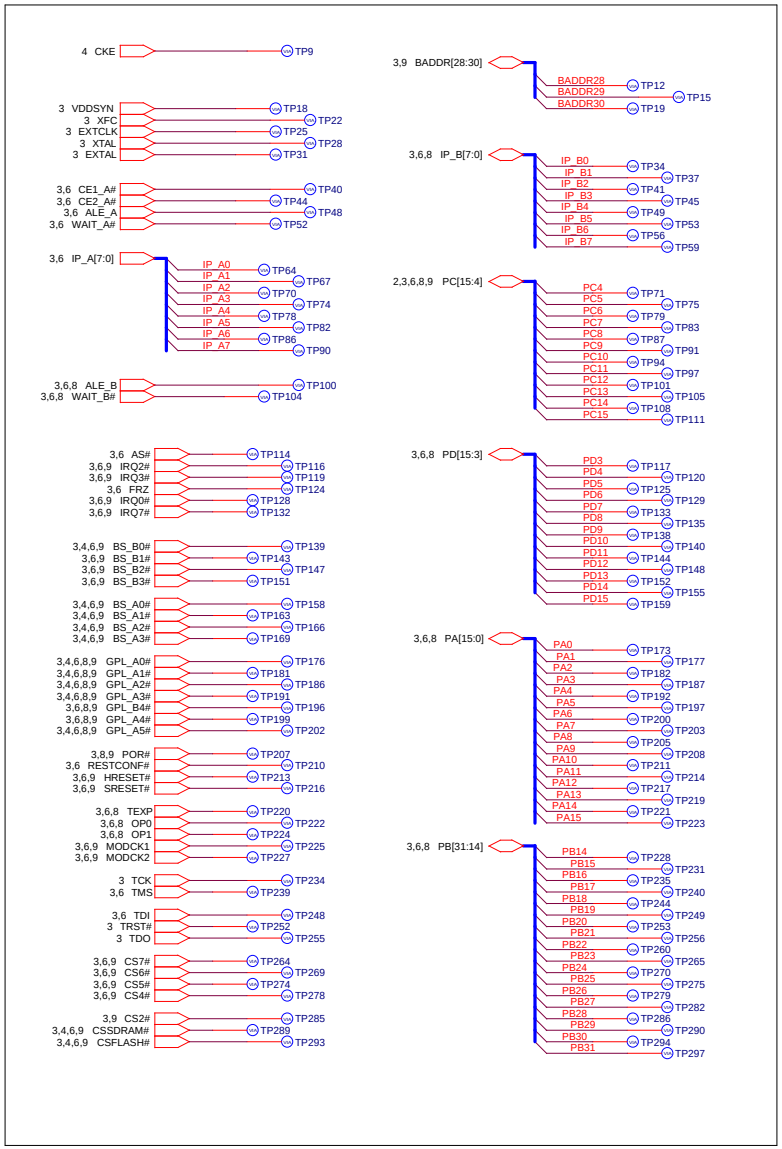

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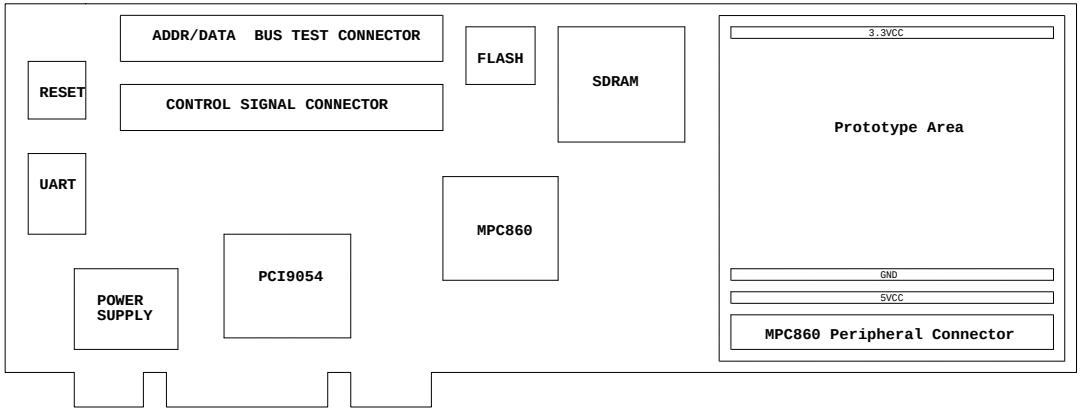
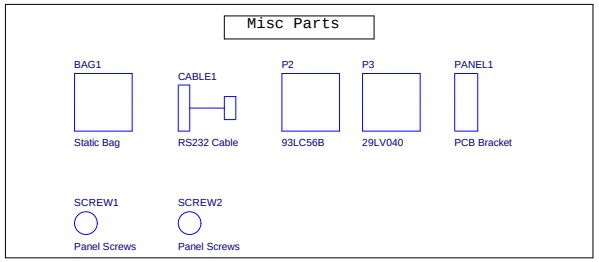


Universal PCI Connector (3.3V/5V)



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