PEX 8680
Schematic Design Checklist

August 10, 2010
Version 1.1

Purpose and Scope

The purpose of this document is to provide a checklist of recommendations to consider for successfully implementing the PEX 8680 device in your schematic and PCB design. It provides some basic guidelines to consider for your schematic design, PCB design and silicon choices. References to other PLX documents are also provided for more detailed information.
Note: *Table Numbering is consistent with the Databook.*

Serial EEPROM Requirements

The PEX 8680 is, as of the date of this document, shipping with revision AA silicon. If you have parts with this revision, a serial EEPROM is *not required* for this part. However, we strongly recommend implementing the serial EEPROM circuit in your design, even if not populated. This will allow for inclusion of EEPROM-based workarounds for any errata that may be documented in the future.

Schematic Guidelines

Please review the PEX 8680 Quick Start Design Guide for important information above how to design with the PEX 8680. Another good reference guide is the schematic included in the PEX 8680 Hardware Reference Manual. This design has been extensively tested by PLX so it can make a good template to customize for your design with the PEX 8680.

Schematic Connections – Transparent Port

APPLICATION: ADD-IN CARD ☐ EMBEDDED ☐ DAUGHTER CARD ☐ UNKNOWN ☐
CUSTOMER: **DATE:**

8680 SCHEMATIC CHECKLIST

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Abbreviations

The following abbreviations are used in the signal tables provided in this chapter.

Table 3-1. Ball Assignment Abbreviations

Abbreviation	Description
#	Active-Low signal
A	Analog Input signal
APWR	Power () balls for SerDes Analog circuits
CMLCLKn[1]	Differential low-voltage, high-speed, CML negative Clock inputs
CMLCLKp[a]	Differential low-voltage, high-speed, CML positive Clock inputs
CMLRn	Differential low-voltage, high-speed, CML negative Receiver inputs
CMLRp	Differential low-voltage, high-speed, CML positive Receiver inputs
CMLTn	Differential low-voltage, high-speed, CML negative Transmitter outputs
CMLTp	Differential low-voltage, high-speed, CML positive Transmitter outputs
CPWR	Power () balls for low-voltage Core circuits
GND	Common Ground () for all circuits
I	Input
I/O	Bidirectional (Input or Output)
I/OPWR	2.5V Power () balls for Input and Output interfaces
O	Output
OD	Open Drain output
PD	Weak internal pull-down resistor
PLLPWR	2.5V Power () balls for Phase-Locked Loop (PLL) circuits
PU	Weak internal pull-up resistor
SerDes	Serializer/De-Serializer differential low-voltage, high-speed, I/O signal pairs (negative and positive)
STRAP	Signals used for PEX 8680 configuration, operational mode setting, and ***Factory Test***; these signals generally are not toggled at runtime

[1] *For REFCLK input, CML source is recommended; however, LVDS source is supported.*

Internal Pull-Up/Pull-Down Resistors

The PEX 8680 contains I/O buffers that have weak internal pull-up or pull-down resistors, indicated in this chapter by PU or PD, respectively, in the signal ball tables (**Type** column). If a signal with this notation is used and no board trace is connected to the ball, the internal resistor is usually sufficient to keep the signal from toggling. However, if a signal with this notation is not used, but is connected to a board trace, the internal resistors might not be strong enough to hold the signal in the inactive state. In cases such as these, it is recommended that the signal be pulled High to or Low to (GND), as appropriate, through a 3KΩ to 10KΩ resistor.

Internal Resistor Values lists the internal pull-up and pull-down resistor values.

Table 3-2. Internal Resistor Values

Internal Resistor	Minimum	Typical	Maximum	Units
PU	74K	111K	177K	Ω
PD	61K	98K	178K	Ω

Signal Ball Descriptions

Note: *If there is more than one ball per signal name, the ball numbers are ordered, in sequence, to follow signal name sequencing [n to 0].*

The PEX 8680 signals are divided into the following groups:

- PCI Express Signals
- Parallel Hot Plug Signals for Ports D, C, B, and A
- Serial Hot Plug Signals
- Serial EEPROM Signals
- Strapping Signals
- JTAG Interface Signals
- I2C/SMBus Slave Interface Signals
- Device-Specific Signals
- External Resistor Signals
- No Connect Signals
- Power and Ground Signals

PCI Express Signals

PCI Express Signals defines the PCI Express SerDes and Control signals.

PCI Express Signals – 323 Balls

Signal Name	Type	Location	Pin Status	Description
PEX_PERn[15:0]	CMLRn	AL21, AL20, AL19, AL18, AL17, AL16, AL15, AL14, AL13, AL12, AL11, AL10, AL8, AL7, AL6, AL5	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 0 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PERn[31:16]	CMLRn	AL22, AL23, AL24, AL25, AL26, AL27, AL28, AL29, AJ31, AH31, AG31, AF31, AE31, AD31, AC31, AB31	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 1 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PERn[47:32]	CMLRn	D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 2 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PERn[79:64]	CMLRn	F31, G31, H31, J31, K31, L31, M31, N31, P31, R31, T31, U31, V31, W31, Y31, AA31	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 4 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PERn[95:80]	CMLRn	D13, D12, D11, D10, D9, D8, D7, D6, F4, G4, H4, J4, K4, L4, M4, N4	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 5 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PERp[15:0]	CMLRp	AK21, AK20, AK19, AK18, AK17, AK16, AK15, AK14, AK13, AK12, AK11, AK10, AK8, AK7, AK6, AK5	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 0 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PERp[31:16]	CMLRp	AK22, AK23, AK24, AK25, AK26, AK27, AK28, AK29, AJ30, AH30, AG30, AF30, AE30, AD30, AC30, AB30	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 1 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PERp[47:32]	CMLRp	E14, E15, E16, E17, E18, E19, E20, E21, E22, E23, E24, E25, E26, E27, E28, E29	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 2 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***

Signal Name	Type	Location	Pin Status	Description
PEX_PERp[79:64]	CMLRp	F30, G30, H30, J30, K30, L30, M30, N30, P30, R30, T30, U30, V30, W30, Y30, AA30	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 4 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PERp[95:80]	CMLRp	E13, E12, E11, E10, E9, E8, E7, E6, F5, G5, H5, J5, K5, L5, M5, N5	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 5 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PERST#	I PU	AC8	YES ☐ NO ☐ UNKNOWN ☐	**PCI Express Reset** Used only in Base mode, to cause a Fundamental Reset. (Refer to Section 5.1.1, "Base Mode (Mode1) Resets," for further details.) ***Note:VSx_PERST#*** *signals are the Reset inputs used in Virtual Switch mode.*
PEX_PETn[15:0]	CMLTn	AP21, AP20, AP19, AP18, AP17, AP16, AP15, AP14, AP13, AP12, AP11, AP10, AP8, AP7, AP6, AP5	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 0 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PETn[31:16]	CMLTn	AP22, AP23, AP24, AP25, AP26, AP27, AP28, AP29, AJ34, AH34, AG34, AF34, AE34, AD34, AC34, AB34	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 1 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PETn[47:32]	CMLTn	A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 2 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PETn[79:64]	CMLTn	F34, G34, H34, J34, K34, L34, M34, N34, P34, R34, T34, U34, V34, W34, Y34, AA34	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 4 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PETn[95:80]	CMLTn	A13, A12, A11, A10, A9, A8, A7, A6, F1, G1, H1, J1, K1, L1, M1, N1	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 5 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PETp[15:0]	CMLTp	AN21, AN20, AN19, AN18, AN17, AN16, AN15, AN14, AN13, AN12, AN11, AN10, AN8, AN7, AN6, AN5	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 0 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***

Signal Name	Type	Location	Pin Status	Description
PEX_PETp[31:16]	CMLTp	AN22, AN23, AN24, AN25, AN26, AN27, AN28, AN29, AJ33, AH33, AG33, AF33, AE33, AD33, AC33, AB33	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 1 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PETp[47:32]	CMLTp	B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 2 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PETp[79:64]	CMLTp	F33, G33, H33, J33, K33, L33, M33, N33, P33, R33, T33, U33, V33, W33, Y33, AA33	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 4 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
PEX_PETp[95:80]	CMLTp	B13, B12, B11, B10, B9, B8, B7, B6, F2, G2, H2, J2, K2, L2, M2, N2	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 5 (16 Balls)** ***Series 100nF AC coupling capacitor required on each transmit receive pair***
External REFCLK Clock Transmitter	N/A	External- CML	YES ☐ NO ☐ UNKNOWN ☐	Recommended for CML: **33Ohm series and 49Ohm shunt required on each differential Pair.** Maximum clock Frequency Tolerance allowed for REFCLK source is +/- 300PPM. Make sure your REFCLK oscillator supports this Also consult the clock buffer Manufacturers Data Sheet.
PEX_REFCLKn	CMLCLKn	AP9	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of 100-MHz PCI Express Reference Clock Input Signal Pair** Requires 100nF AC Coupling Capacitor in series with each differential signal.
PEX_REFCLKp	CMLCLKp	AN9	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of 100-MHz PCI Express Reference Clock Input Signal Pair** Requires 100nF AC Coupling Capacitor in series with each differential signal.

Hot Plug Signals

The PEX 8680 includes signals for both Parallel and Serial Hot Plug support. Parallel Hot Plug is supported on any of four Transparent downstream Ports, and/or Serial Hot Plug is supported on the maximum of 23 downstream Ports.

Parallel Hot Plug can be implemented on any Transparent downstream Port, as selected by the **Parallel Hot Plug Control** register (Port 0, offset 3A4h[7:0, 15:8, 23:16, and 31:24] for Parallel Hot Plug Controllers A, B, C and D, respectively).

Serial Hot Plug can be implemented on any Transparent downstream Port. If a downstream Transparent Port is capable of both Parallel Hot Plug and Serial Hot Plug, the Serial Hot Plug Controller is used, by default, unless the Port's *Serial Hot Plug Override Parallel Disable* bit is Set (offset F70h[19]=1).

Hot Plug signals are enabled, configured and accessed through the **Slot Capability** and **Slot Status and Control** registers (offsets 7Ch and 80h, respectively), in each Port. Also, the **Power Management Hot Plug User Configuration** register (offset F70h) in each Port provides additional Device-Specific configuration and control for both Parallel and Serial Hot Plug implementations.

Parallel Hot Plug Signals

The PEX 8680 includes 10 signal balls per Hot Plug-capable Port that supports the Parallel Hot Plug Controller (HP_), as defined in Parallel Hot Plug Signals fo. These signals are active only for Hot Plug-capable Transparent downstream Ports configured at startup.

For further details regarding Hot Plug, refer to Chapter 10, "Hot Plug Support."

Notes: *All Parallel Hot Plug signals are I/O; however, their logical operation is either input or output, as described for each signal.*

All Parallel Hot Plug signals are duplicated for each Hot Plug-capable Port, as A, B, C, and D signals, which map to any Transparent downstream Port, as selected by the ***Parallel Hot Plug Control*** *register (Port 0, offset 3A4h[7:0, 15:8, 23:16, and 31:24] for Parallel Hot Plug Controllers A, B, C and D, respectively)*

Parallel Hot Plug Signals[2] for Ports D, C, B, and A – 40 Balls

Signal Name	Type	Location	Pin Status	Description
HP_ATNLED_[D, C, B, A]#	I/O PU	N26, H27, W8, AM30	YES ☐ NO ☐ UNKNOWN ☐	**Hot Plug Attention LED Outputs (4 Balls)** Active-Low Slot Control Logic output that is used to drive the Attention Indicator. Output is asserted Low to turn On (illuminate) the LED. Enabled when the **Slot Capability** register *Attention Indicator Present* bit is Set (offset 7Ch[3]=1) and controlled by the **Slot Control** register *Attention Indicator Control* field (offset 80h[7:6]). When software writes to the *Attention Indicator Control* field, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capability** register *Attention Indicator Present* bit is Set (offset 7Ch[3]=1), and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is Set (offset 80h[5]=1), an interrupt (MSI, INT*x* Message, or output, all mutually exclusive, on a per-Port basis) can be generated to the Host. **If HP_ATNLED_*x*# are used, each requires an external current-limiting resistor.** No-connect ok if not used.

[2] *If Hot Plug outputs (including HP_PERST_x#) are used and HP_MRL_x# input is not used, pull HP_MRL_x# input Low so that Hot Plug outputs (including HP_PERST_x#) will properly sequence if the serial EEPROM is blank or missing. Default register values enable HP_MRL_x#, which must then be asserted to cause Hot Plug outputs to toggle (for example, to de-assert HP_PERST_x# and assert HP_PWRLED_x#).*

Signal Name	Type	Location	Pin Status	Description
HP_BUTTON_[D, C, B, A]#	I/O PU	M27, B32, AF9, AE23	YES ☐ NO ☐ UNKNOWN ☐	**Hot Plug Attention Button Inputs (4 Balls)** Active-Low Slot Control Logic input that is connected directly to the Attention Button, with input assertion status latched in the **Slot Status** register *Attention Button Pressed* bit (offset 80h[16]). Enabled when the **Slot Capability** register *Attention Button Present* bit is Set (offset 7Ch[0]=1). When the following conditions exist: • HP_BUTTON_*x*# is not masked (**Slot Control** register *Attention Button Pressed Enable* bit, offset 80h[0]=1), and • **Slot Capability** register *Hot Plug Capable* bit is Set (offset 7Ch[6]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is Set (offset 80h[5]=1), an interrupt (MSI, INT*x* Message, or output, all mutually exclusive, on a per-Port basis) can be generated, to notify the Host of intended board insertion or removal. ***Note:*** *HP_BUTTON_x# is internally de-bounced, but must remain stable for at least 10 ms.* No-connect ok if not used.
HP_CLKEN_[D, C, B, A]#	I/O PU	AD25, P26, AG8, AM4	YES ☐ NO ☐ UNKNOWN ☐	**Hot Plug Reference Clock Enable Outputs (4 Balls)** Active-Low Slot Control Logic output that, when enabled, controls the connection of the external REFCLK to the slot. Enabled when the **Slot Capability** register *Power Controller Present* bit is Set (offset 7Ch[1]=1), and controlled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]). The time delay from HP_PWREN_*x* output assertion to HP_CLKEN_*x*# output assertion is programmable (through serial EEPROM load) from 128 to 512 ms, in the *HPC* T_{pepv} field (offset F70h[4:3]). When this register is programmed to 00b (default), HP_PWR_GOOD_*x* input assertion controls the time delay from HP_PWREN_*x* output assertion to HP_CLKEN_*x*# output assertion. No-connect ok if not used.

Signal Name	Type	Location	Pin Status	Description
HP_MRL_[D, C, B, A]#	I/O PU	N27, H28, AA9, AG26	YES ☐ NO ☐ UNKNOWN ☐	**Hot Plug Manually Operated Retention Latch Sensor Inputs (4 Balls)** Active-Low Slot Control Logic input that is connected directly to an optional Manually operated Retention Latch (MRL) Sensor that is logic Low when the latch is closed. Enabled when the **Slot Capability** register *MRL Sensor Present* bit is Set (offset 7Ch[2]=1). When enabled, HP_MRL_*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power (HP_PWREN_*x* and HP_PWRLED_*x*#) and clock (HP_CLKEN_*x*#), and de-assert Reset (HP_PERST_*x*#) after reset, as illustrated in Figure 11-2, "Hot Plug Outputs When Power Controller Present and Power Controller Control Bits Are Cleared," or under software control. A change in the HP_MRL_*x*# signal state is latched in the **Slot Status** register *MRL Sensor Changed* bit (offset 80h[18]), and the state change can assert an interrupt to notify the Host of a change in the MRL Sensor state. When the following conditions exist: • HP_MRL_*x*# is not masked (**Slot Control** register *MRL Sensor Changed Enable* bit, offset 80h[2]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is Set (offset 80h[5]=1), an interrupt (MSI, INT*x* Message, or output, all mutually exclusive, on a per-Port basis) can be generated. If the associated Hot Plug-capable Transparent downstream Port connects to a PCI Express board slot that does not implement an MRL Sensor, HP_MRL_*x*# is typically connected to HP_PRSNT_*x*# and a pull-up resistor, with the common node connected to the PRSNT2# signal(s) at the slot. If the associated Hot Plug-capable Transparent downstream Port instead connects directly to a device (in which case Hot Plug is not used), pull HP_MRL_*x*# Low. When HP_MRL_*x*# is enabled and is sampled Low on a powered slot, the slot power is automatically shut Off. When HP_MRL_*x*# is enabled and the input is sampled High on a powered slot, REFCLK to the slot is automatically disconnected and the slot power is automatically turned Off, as illustrated in Figure 10-3, "Hot Plug Automatic Power-Down Sequence," ***Note:*** *HP_MRL_x# is internally de-bounced, but must remain stable for at least 10 ms. HP_MRL_x#, if enabled, is not de-bounced when sampled immediately after reset.* No-connect ok if not used.
HP_PERST_[D, C, B, A]#	I/O PU	AM33, C31, AG10, AM31	YES ☐ NO ☐ UNKNOWN ☐	**Hot Plug Reset Outputs (4 Balls)** Active-Low Slot Control Logic output that is used to reset the slot. The output is controlled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]). No-connect ok if not used.

Signal Name	Type	Location	Pin Status	Description
HP_PRSNT_[D, C, B, A]#	I/O PU	AC28, J26, AM2, AG24	YES ☐ NO ☐ UNKNOWN ☐	**Hot Plug PRSNT2# Inputs (4 Balls)** Active-Low Slot Control Logic input that connects to the slot's PRSNT2# signal, which on the add-in board connects to the slot's PRSNT1# signal, which is typically grounded on the motherboard. A change in the HP_PRSNT_*x*# Input signal state is latched in the **Slot Status** register *Presence Detect Changed* bit (offset 80h[19]), and the state change can assert an interrupt to notify the Host of board presence or absence. When the following conditions exist: • HP_PRSNT_*x*# is not masked (**Slot Control** register *Presence Detect Changed Enable* bit (offset 80h[3]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is Set (offset 80h[5]=1), an interrupt (MSI, INT*x* Message, or output, all mutually exclusive, on a per-Port basis) can be generated. ***Note:*** *HP_PRSNT_x# is internally de-bounced, but must remain stable for at least 10 ms.* No-connect ok if not used.
HP_PWREN_[D, C, B, A]	I/O PD	AB26, D31, AL2, AG23	YES ☐ NO ☐ UNKNOWN ☐	**Hot Plug Power Enable Outputs (4 Balls)** Active-High Slot Control Logic output that controls the slot power state. When this output is High, power is enabled to the slot. Enabled when the **Slot Capability** register *Power Controller Present* bit is Set (offset 7Ch[1]=1). When software turns the slot's Power Controller On or Off (**Slot Control** register *Power Controller Control* bit (offset 80h[10])), a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is Set (offset 80h[5]=1), an interrupt (MSI, INT*x* Message, or output, all mutually exclusive, on a per-Port basis) can be generated to the Host. When HP_MRL_*x*# is enabled (**Slot Capability** register *MRL Sensor Present* bit, offset 7Ch[2]=1), HP_MRL_*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power, by asserting HP_PWREN_*x* after reset, as illustrated in Figure 10-2, "Hot Plug Outputs When Power Controller Present and Power Controller Control Bits Are Cleared," or under software control. ***Note:*** *HP_PWREN_x polarity is inverted with respect to HP_PWRENx# functionality in PLX ExpressLane Gen 1 switches.* No-connect ok if not used.

Signal Name	Type	Location	Pin Status	Description
HP_PWRFLT_[D, C, B, A]#	I/O PU	AL34, B33, AA7, AP32	YES ☐ NO ☐ UNKNOWN ☐	**Hot Plug Power Fault Inputs (4 Balls)** Active-Low Slot Control Logic input that, when asserted Low, indicates that the slot's external Power Controller detected a power fault on one or more supply rails. Enabled when the **Slot Capability** register *Power Controller Present* bit is Set (offset 7Ch[1]=1), and input assertion status is latched in the **Slot Status** register *Power Fault Detected* bit (offset 80h[17]). When the following conditions exist: • HP_PWRFLT_*x*# is not masked (**Slot Control** register *Power Fault Detector Enable* bit, offset 80h[1]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is Set (offset 80h[5]=1), an interrupt (MSI, INT*x* Message, or output, all mutually exclusive, on a per-Port basis) can be generated, to notify the Host of a power fault. ***Note:*** *If HP_PWREN_x and HP_CLKEN_x# are not used, HP_PWRFLT_x# can be used as a general-purpose input with status reflected in the **Slot Status** register Power Fault Detected bit (offset 80h[17]), provided the **Slot Capability** register Power Controller Present bit is Set (offset 7Ch[1]=1).* No-connect ok if not used.
HP_PWR_GOOD_[D, C, B, A]	I/O PD	AH28, T25, AA10, AH7	YES ☐ NO ☐ UNKNOWN ☐	**Hot Plug Power Good Inputs (4 Balls)** Active-High (default) input that when enabled (default), causes the Slot Control Logic to delay HP_CLKEN_*x*# output assertion to turn On REFCLK to the slot, until HP_PWR_GOOD_*x*# input is asserted to indicate that the installed module's power supplies are active and stable. Signal polarity can be changed to Active-Low, by programming the serial EEPROM to Set the Port's *HP_PWR_GOOD_x Active Low Enable* bit (offset F70h[6]). Polarity must not be changed by I^2C, because that is too slow for initialization. HP_PWR_GOOD_*x* is disabled when the *HPC* T_{pepv} field (offset F70h[4:3]) is programmed to a value other than 00b, to cause HP_CLKEN_*x*# output assertion to follow HP_PWREN_*x*# assertion, by a fixed delay (128, 256, or 512 ms). No-connect ok if not used.

Signal Name	Type	Location	Pin Status	Description
HP_PWRLED_[D, C, B, A]#	I/O PU	AL31, P27, AK3, AN31	YES ☐ NO ☐ UNKNOWN ☐	**Hot Plug Power LED Outputs (4 Balls)** Active-Low Slot Control Logic output that is used to drive the Power Indicator. This output is asserted Low to turn On (illuminate) the LED. Enabled when the **Slot Capability** register *Power Indicator Present* bit is Set (offset 7Ch[4]=1), and controlled by the **Slot Control** register *Power Indicator Control* field (offset 80h[9:8]). When software writes to the *Power Indicator Control* field, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capability** register *Power Indicator Present* bit is Set (offset 7Ch[4]=1), and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4]=1), and • **Slot Control** register *Hot Plug Interrupt Enable* bit is Set (offset 80h[5]=1), an interrupt (MSI, INT*x* Message, or output, all mutually exclusive, on a per-Port basis) can be generated to the Host. **If HP_PWRLED_*x*# are used, they require an external current-limiting resistor.** No-connect ok if not used.

Serial Hot Plug Signals

Parallel Hot Plug Signals fo defines the three signal balls that support Serial Hot Plug. Additionally, the PEX 8680 supports external Serial Hot Plug signals on the I²C I/O Expander. (Refer to Section 10.9.2, "I/O Expander Parts Selection and Pin Definition.")

These signals are active only for Serial Hot Plug-capable Ports configured at startup. For further details regarding Hot Plug, refer to Chapter 10, "Hot Plug Support."

Transparent downstream Ports can implement Hot Plug by using external I²C I/O Expanders (one 16pin Maxim MAX7311, NXP PCA9555, or TI PCA9555 per slot (no serial EEPROM is required) –or– one 40-pin NXP PCA9698 per two slots. All Ports implementing Serial Hot Plug can concurrently use either type of I/O Expander (16-pin or 40-pin). The Serial Hot Plug Controller queries each I/O Expander for its Device ID. 40-Pin I/O Expanders implement Device ID, and 16-Pin I/O Expanders do not. If the device responds to the Device ID query from the PEX 8680, the Serial Hot Plug Controller assumes that the I/O Expander is a 40-pin device. The Device ID query can be disabled by setting the **Power Management Hot Plug User Configuration** register *40-Pin I/O Expander Disable* bit (Port 0, offset F70h[17]=1).

Serial Hot Plug Signals – 3 Balls

Signal Name	Type	Location	Pin Status	Description
I2C_SCL1	OD	AM32	YES ☐ NO ☐ UNKNOWN ☐	**I²C Serial Clock Output for Serial Hot Plug Support** I²C Clock source. Used with the external Serial Hot Plug I/O Expander, and must be bused to each I/O Expander's Clock (SCL) pin. In combination with , forms the PEX 8680 I²C Master interface. **I2C_SCL1 requires an external pull-up resistor.**
I2C_SDA1	OD	AF26	YES ☐ NO ☐ UNKNOWN ☐	**I²C Serial Data Output for Serial Hot Plug Support** Transmits and receives I²C data. Used with the external Serial Hot Plug I/O Expander, and must be bused to each I/O Expander's Data (SDA) pin. In combination with , forms the PEX 8680 I²C Master interface. **I2C_SDA1 requires an external pull-up resistor.**
SHPC_INT#	I/O PU	L11	YES ☐ NO ☐ UNKNOWN ☐	**Serial Hot Plug Controller Interrupt Input** Active-Low interrupt input from external I²C I/O Expanders. Used only by Serial Hot Plug-capable Transparent downstream Ports. **If used, SHPC_INT# requires an external pull-up resistor.** ***Notes:*** *By default, is internally de-bounced, but must remain stable for at least 10 ms. Internal de-bouncing can be disabled, by Setting the Serial Hot Plug INTx De-Bounce Disable bit (offset F70h[18]=1) in the Port.* *Although this is an I/O signal, its logical operation is input.* *If used, pull high to VDD25 through 3.3KΩ.*

Serial EEPROM Signals

The PEX 8680 includes four signals for interfacing to a serial EEPROM. For information regarding serial EEPROM use, refer to Chapter 6, "Serial EEPROM Controller."

Serial EEPROM Signals – 4 Balls

Signal Name	Type	Location	Pin Status	Description
EE_CS#	I/O PU	R28	YES ☐ NO ☐ UNKNOWN ☐	**Active-Low Serial EEPROM Chip Select Output** ***Note:****Although this is an I/O signal, its logical operation is output.* Can be left floating if not used.
EE_DI	O	N28	YES ☐ NO ☐ UNKNOWN ☐	**PEX 8680 Output to Serial EEPROM Data Input** Can be left floating if not used.
EE_DO	I/O PU	T26	YES ☐ NO ☐ UNKNOWN ☐	**PEX 8680 Input from Serial EEPROM Data Output** Should be pulled High .
EE_SK	I/O PU	T27	YES ☐ NO ☐ UNKNOWN ☐	**Serial EEPROM Clock Frequency Output** Programmable (by way of the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 268h[2:0])) to the following: • 1 MHz (default) • 1.98 MHz • 5 MHz • 9.62 MHz • 12.5 MHz • 15.6 MHz • 17.86 MHz Can be left floating if not used.

Strapping Signals

The PEX 8680 Strapping signals, defined in Strapping Signals, set the configuration of upstream Port and NT Port assignment, Port width, and various setup and test modes.

Internal pull-up and pull-down resistors set the default configuration; if the PEX 8680 configuration must be changed from the default, external pull-up and/or pull-down resistors can be connected. External resistors are not required unless:

- The Strapping signals must be inverted from the default logic state, –or–
- The Strapping signals are connected to circuit traces (the internal resistors are relatively weak, and may not be strong enough to hold circuit traces to the default input states)

After a Fundamental Reset, the **Link Capability**, **VS0 Upstream**, and **Port Configuration** registers capture ball status. Strapping ball Configuration data can be changed by writing new data to these registers from the Management Port or serial EEPROM. I^2C can change Strapping ball Configuration data; however, the input should be Low, to prevent linkup and Host enumeration. Then, when I^2C programming is complete, I^2C should lastly Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]=1), to enable linkup and allow subsequent Host enumeration.

Strapping Signals – 47 Balls

Signal Name	Type	Location	Pin Status	Description
STRAP_DEBUG_SEL[1:0]	I PD	AN2, AN3	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only* (2 Balls)** Pull Low. Optionally, this input can remain unconnected, because the internal pull-down resistor holds the input Low..
STRAP_FAST_BRINGUP#	I PU	AP31	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Must be High. This input can remain unconnected, because the internal pull-up resistor holds the input High.
STRAP_G1_COMPATIBLE#	I PU	AK1	YES ☐ NO ☐ UNKNOWN ☐	**Compatibility Enable for Non-Compliant Gen 1 Endpoints** When STRAP_G1_COMPATIBLE# is pulled High, the Data Rate Identifier symbol in the TS Ordered-Sets always advertises support for both the Gen 2 data rate and Autonomous Change. When STRAP_G1_COMPATIBLE# is pulled Low and the Link training sequence fails during the Configuration state, the next time the LTSSM exits the Detect state, TS Ordered-Sets advertise only the Gen 1 data rate, and no Autonomous Change support. The LTSSM then continues to toggle between Gen 1 and Gen 2 advertisement every time it exits Detect. ***Notes: This feature should be enabled only if a non-compliant device will not linkup if these Data Rate Identifier bits are Set.*** *Normally, this input should be pulled High to VDD25.* Optionally, this input can remain unconnected, because the internal pull-up resistor holds the input High.

Signal Name	Type	Location	Pin Status	Description
STRAP_I2C_CFG_EN#	I PU	AK4	YES ☐ NO ☐ UNKNOWN ☐	**I²C Bus Configuration Enable** L = Enables I²C Bus for device configuration. The Links do not start training until I²C Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]=1). ***Note:*** *I²C protocol (bitstream) must be used for this initialization and delayed linkup feature (not SMBus protocol).* H = Disables I²C Bus for device configuration. The Links start training after Fundamental Reset and serial EEPROM initialization. **Virtual Switch Mode Only** STRAP_I2C_CFG_EN# is used in tandem with STRAP_NT_ENABLE# and STRAP_NT_UPSTRM_PORTSEL0 in Virtual Switch mode. For details, refer to Table 3-8, which illustrates the relationship between the three signals.
STRAP_NT_ENABLE#	I/O PU	E4	YES ☐ NO ☐ UNKNOWN ☐	**Enable NT Mode** ***Note:*** *The PEX 8680 supports this NT mode signal in Base mode only.* Active-Low signal that enables and disables NT mode. The Strapping signal can be overridden by the serial EEPROM value for the **VS0 Upstream** register *VS0 NT Enable* bit (Port 0, offset 360h[13]). If the **VS0 Upstream** register is programmed by serial EEPROM, that must be the first entry in the serial EEPROM. I²C can enable or disable NT mode, by writing to the **VS0 Upstream** register. If I²C programs the **VS0 Upstream** register (to change the strapped configuration for the upstream Port, NT Port, and/or NT mode), I²C must program this register first. The input can be pulled Low, to delay linkup and Host enumeration until I²C initialization is complete. After I²C initialization is complete, I²C must then Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 3ACh[0]=1). Software can enable or disable NT mode, by writing to the **Debug Control** register, if the register's *Hardware/Software Configuration Mode Control* bit is already Set (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 350h[9]=1). L = Enables NT mode H = Disables NT mode (default)

Signal Name	Type	Location	Pin Status	Description
STRAP_NT_P2P_EN#	I PU	AL4	YES ☐ NO ☐ UNKNOWN ☐	**NT PCI-to-PCI Bridge Enable** ***Notes:*** *The PEX 8680 supports this NT mode signal in Base mode only.* *This input should be pulled Low, unless the NT PCI-to-PCI bridge between the internal Virtual PCI Bus and the NT Port Virtual Interface must be disabled for software compatibility to earlier NT mode switches.* This input maps to the **Debug Control** register *NT P2P Enable* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 350h[14]. This signal and its corresponding register bit must ***not*** be toggled at runtime. L = Enables NT PCI-to-PCI bridge H = Disables NT PCI-to-PCI bridge (default)

Signal Name	Type	Location	Pin Status	Description
STRAP_NT_UPSTRM_PORTSEL[4:0]	[4:1]: I PD [0]: I/O PD	E31, B5, E5, A5, A4	YES ☐ NO ☐ UNKNOWN ☐	**Select Upstream Non-Transparent Port (5 Balls)** ***Note:****The PEX 8680 supports this NT mode signal in Base mode only.* Select any Port to be the upstream NT Port. The Strapping signal can be overridden by the serial EEPROM value for the **VS0 Upstream** register *VS0 NT Port* field (Port 0, offset 360h[12:8]). If the **VS0 Upstream** register is programmed by serial EEPROM, that must be the first entry in the serial EEPROM. I^2C can change which Port is configured to be the NT Port, by writing to the **VS0 Upstream** register *VS0 NT Port* field. The input should be Low, to prevent linkup and Host enumeration. After I^2C reconfigures the PEX 8680, I^2C should lastly Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 3ACh[0]=1), to enable linkup and allow subsequent Host enumeration. Software can change which Port is configured to be the NT Port, by writing to the **Debug Control** register, if the register's *Hardware/Software Configuration Mode Control* bit is already Set (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 350h[9]=1). Refer to Section 14.8, "Port Programmability," for further details. LLLLL = Port 0 LHLHL = Port 10 LLLLH = Port 1 LHLHH = Port 11 LLLHL = Port 2 HLLLL = Port 16 LLLHH = Port 3 HLLLH = Port 17 LLHLL = Port 4 HLLHL = Port 18 LLHLH = Port 5 HLLHH = Port 19 LLHHL = Port 6 HLHLL = Port 20 LLHHH = Port 7 HLHLH = Port 21 LHLLL = Port 8 HLHHL = Port 22 LHLLH = Port 9 HLHHH = Port 23 ***Note:*** *If NT mode is not used (=H, and/or the serial EEPROM programs NT mode (**VS0 Upstream** register VS0 NT Enable bit (Port 0, offset 360h[13]=1), thereby overriding), these inputs can remain unconnected (N/C), in which case the **VS0 Upstream** register VS0 NT Port field value defaults to the logic level Set by the internal pull-down resistors, 0h.*

Signal Name	Type	Location	Pin Status	Description
STRAP_PLL_BYPASS#	I PU	AK34	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Must remain unconnected (N/C), or pulled High to .
STRAP_PROBE_MODE#	I PU	AN33	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Must remain unconnected (N/C), or pulled High to .
STRAP_RESERVED[1:0]	I PU	G12, H9	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only* (2 Balls)** These inputs must be strapped to 01b (LH). STRAP_RESERVED0 can remain unconnected (N/C), because the internal resistors Set the correct value.
STRAP_RESERVED[3:2]	I PD	H15, H14	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only* (2 Balls)** These inputs must be strapped to 00b (LL), and can remain unconnected (N/C), because the internal resistors Set the correct value.
STRAP_RESERVED[21, 20]	I PD	C2, B2	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only* (2 Balls)** These inputs should be unconnected (N/C), and are pulled Low by a weak internal pull-down resistor.
STRAP_RESERVED16	I	AG27	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Must be tied directly to Ground ().
STRAP_RESERVED17#	I PU	C34	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Must remain unconnected (N/C), or pulled High to .
STRAP_SERDES_MODE_EN#	I PU	AK33	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Must remain unconnected (N/C), or pulled High to .
STRAP_SMBUS_EN#	I PU	Y9	YES ☐ NO ☐ UNKNOWN ☐	**System Management Bus Enable** L = Enables SMBus Slave protocol on the and 2-wire bus H = Enables I^2C Slave protocol on the and 2-wire bus

Signal Name	Type	Location	Pin Status	Description
STRAP_STN0_PORTCFG[1:0]	[1]: I/O PD [0]: I PD	AL30, AN34	YES ☐ NO ☐ UNKNOWN ☐	**Strapping Signals to Select Port Configuration for Station 0 (Number of Enabled Ports (1, 2, 3, or 4), and Maximum Number of Lanes for Each Specific Port) (2 Balls)** **Register/Bits** – **Port Configuration** register *Port Configuration for Station 0* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 300h[1:0]) LL = x4, x4, x4, x4 LH = x16 HL = x8, x8 HH = x8, x4, x4
STRAP_STN1_PORTCFG[1:0]	I/O PD	E1, B3	YES ☐ NO ☐ UNKNOWN ☐	**Strapping Signals to Select Port Configuration for Station 1 (Number of Enabled Ports (1, 2, 3, or 4), and Maximum Number of Lanes for Each Specific Port) (2 Balls)** **Register/Bits** – **Port Configuration** register *Port Configuration for Station 1* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 300h[3:2]) LL = x4, x4, x4, x4 LH = x16 HL = x8, x8 HH = x8, x4, x4
STRAP_STN2_PORTCFG[1:0]	I PD	B30, D30	YES ☐ NO ☐ UNKNOWN ☐	**Strapping Signals to Select Port Configuration for Station 2 (Number of Enabled Ports (1, 2, 3, or 4), and Maximum Number of Lanes for Each Specific Port) (2 Balls)** **Register/Bits** – **Port Configuration** register *Port Configuration for Station 2* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 300h[5:4]) LL = x4, x4, x4, x4 LH = x16 HL = x8, x8 HH = x8, x4, x4
STRAP_STN4_PORTCFG[1:0]	I PD	AP30, A30	YES ☐ NO ☐ UNKNOWN ☐	**Strapping Signals to Select Port Configuration for Station 4 (Number of Enabled Ports (1, 2, 3, or 4), and Maximum Number of Lanes for Each Specific Port) (2 Balls)** **Register/Bits** – **Port Configuration** register *Port Configuration for Station 4* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 300h[9:8]) LL = x4, x4, x4, x4 LH = x16 HL = x8, x8 HH = x8, x4, x4

Signal Name	Type	Location	Pin Status	Description
STRAP_STN5_PORTCFG[1:0]	I PD	AN30, E2	YES ☐ NO ☐ UNKNOWN ☐	**Strapping Signals to Select Port Configuration for Station 5 (Number of Enabled Ports (1, 2, 3, or 4), and Maximum Number of Lanes for Each Specific Port) (2 Balls)** **Register/Bits** – **Port Configuration** register *Port Configuration for Station 5* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 300h[11:10]) LL = x4, x4, x4, x4 LH = x16 HL = x8, x8 HH = x8, x4, x4
STRAP_TESTMODE[4:0]	I PD	AK2, AL1, AP4, AN4, AM1	YES ☐ NO ☐ UNKNOWN ☐	**Test Mode Selects (5 Balls)** The setting defines and signal functionality following a Fundamental Reset. PEX_PORT_GOOD[and signal functionality can also be programmed by serial EEPROM, I^2C, or software. **LHLHH (01011b or 0Bh)** • default to the PORT_GOOD function • are inputs, with values reflected in the **GPIO 24_42 Input Data** register (offset 620h) **LHHLL (01100b or 0Ch)** • default to GPIO inputs, with values reflected in the **GPIO 0_23 Input Data** register (offset 61Ch) • default to the PERST# output function **LHHLH (01101b or 0Dh)** • default to the PORT_GOOD function • default to the PERST# output function **LHHHH (01111b or 0Fh)** • default to GPIO inputs, with values reflected in the **GPIO 0_23 Input Data** register (offset 61Ch) • are inputs, with values reflected in the **GPIO 24_42 Input Data** register (offset 620h) All other encodings are ***Factory Test Only***.

Signal Name	Type	Location	Pin Status	Description
STRAP_UPSTRM_PORTSEL[4:0]	I PD	AK30, A31, D34, E34, E33	YES ☐ NO ☐ UNKNOWN ☐	**Strapping Signals to Select Upstream Port (5 Balls)** Select any Port as the upstream Port. The **VS0 Upstream** register *VS0 Upstream Port* field (Port 0, offset 360h[4:0]) defines the upstream Port. If the **VS0 Upstream** register is programmed by serial EEPROM, that must be the first entry in the serial EEPROM. I^2C can enable or disable NT mode, by writing to the **VS0 Upstream** register. If I^2C programs the **VS0 Upstream** register (to change the strapped configuration for the upstream Port, NT Port, and/or NT mode), I^2C must program this register first. The input can be pulled Low, to delay linkup and Host enumeration until I^2C initialization is complete. After I^2C initialization is complete, I^2C must then Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 3ACh[0]=1). Software can change which Port is configured to be the upstream Port, by writing to the **Debug Control** register, if the register's *Hardware/Software Configuration Mode Control* bit is already Set (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 350h[9]=1). Refer to Section 14.8, "Port Programmability," for further details. LLLLL = Port 0 LHLHL = Port 10 LLLLH = Port 1 LHLHH = Port 11 LLLHL = Port 2 HLLLL = Port 16 LLLHH = Port 3 HLLLH = Port 17 LLHLL = Port 4 HLLHL = Port 18 LLHLH = Port 5 HLLHH = Port 19 LLHHL = Port 6 HLHLL = Port 20 LLHHH = Port 7 HLHLH = Port 21 LHLLL = Port 8 HLHHL = Port 22 LHLLH = Port 9 HLHHH = Port 23 All other encodings are ***reserved.***

Signal Name	Type	Location	Pin Status	Description
STRAP_VS_MODE[2:0]	[2]: I PD [1:0]: I/O PD	D5, C1, D1	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**Virtual Switch Enable (3 Balls)** Used together, to enable up to eight virtual switches, depending upon the ball states. The number of Virtual Switches enabled by these inputs is reflected in the **Virtual Switch Enable** register *VSx Enable* bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 358h[7:0]). **Base mode (Mode-1)** These inputs can remain unconnected (N/C), because the internal pull-down resistors Set the default value to LLL. LLL (000b) = Single switch (no virtual switches) **Virtual Switch mode (Mode-2)** LLH (001b) = Two virtual switches – VS0-1 LHL (010b) = Three virtual switches – VS0-2 LHH (011b) = Four virtual switches – VS0-3 HLL (100b) = Five virtual switches – VS0-4 HLH (101b) = Six virtual switches – VS0-5 All other encodings default to the highest value/quantity of virtual switches available**.**

JTAG Interface Signals

The PEX 8680 includes five signals for performing JTAG boundary scan, defined in JTAG Interface Signals. The JTAG interface is described in Section 17.6, "JTAG Interface." If JTAG is not used, these signals can remain unconnected (N/C), because the internal pull-down resistors provide termination for the inputs.

JTAG Interface Signals – 5 Balls

Signal Name	Type	Location	Pin Status	Description
JTAG_TCK	I PD	L10	YES ☐ NO ☐ UNKNOWN ☐	**JTAG Test Clock Input** JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 10 MHz. This signal is internally pulled down through a weak pull-down resistor. Can be left floating if not used.
JTAG_TDI	I PD	K9	YES ☐ NO ☐ UNKNOWN ☐	**JTAG Test Data Input** Serial input to the JTAG TAP Controller, for test instructions and data. This signal is internally pulled down through a weak pull-down resistor. Can be left floating if not used.
JTAG_TDO	O	H8	YES ☐ NO ☐ UNKNOWN ☐	**JTAG Test Data Output** Serial output from the JTAG TAP Controller test instructions and data. Can be left open (No Connect) if JTAG interface is not used.
JTAG_TMS	I PD	G11	YES ☐ NO ☐ UNKNOWN ☐	**JTAG Test Mode Select** When High, JTAG Test mode is enabled. Input decoded by the JTAG TAP Controller to control test operations. This signal is internally pulled down through a weak pull-down resistor. Can be left floating if not used.
JTAG_TRST#	I PD	D3	YES ☐ NO ☐ UNKNOWN ☐	**JTAG Test Reset** Active-Low input used to reset the Test Access Port. Tie to ground through a 1.5KΩ resistor, to hold the JTAG TAP Controller in the *Test-Logic-Reset* state, which enables standard logic operation. When JTAG functionality is not used, the input should be pulled or driven Low, to place the JTAG TAP Controller into the *Test-Logic-Reset* state, which disables the test logic and enables standard logic operation. Alternatively, if input is High, the JTAG TAP Controller can be placed into the *Test-Logic-Reset* state by initializing the JTAG TAP Controller's **Instruction** register to contain the *IDCODE* instruction, or by holding the input High for at least five rising edges of the input.

I²C/SMBus Slave Interface Signals

I defines the five signals that support the I²C/SMBus Slave interface. For further details, refer to Chapter 7, "I²C/SMBus Slave Interface Operation."

I²C/SMBus Slave Interface Signals – 5 Balls

Signal Name	Type	Location		Description
I2C_ADDR[2:0]	I/O PU	P7, B4, C4	YES ☐ NO ☐ UNKNOWN ☐	**I²C/SMBus Slave Address Bits 2 through 0 Inputs (3 Balls)** Used to Set the PEX 8680 Slave address on the I²C or SMBus Bus. If I²C or SMBus is used, should be strapped to a unique address, to avoid address conflict with any other I²C/SMBus devices (on the same I²C/SMBus Bus segment) that have the upper four bits of their 7bit I²C/SMBus Slave address also Set to 0011b. When SMBus is enabled (=L), and the **I²C/SMBus Configuration** register *SMBus Enable* bit is Set (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 2C8h[0]=1), only I2C_ADDR[1:0] are used for the Slave address, and I2C_ADDR2 is re-defined to function as the ARP (Address Resolution Protocol) Disable bit, which is mapped to the **I²C/SMBus Configuration** register *ARP Disable* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 2C8h[0]). When I2C_ADDR2=H, ARP is disabled. The internal pull-up resistors cause the inputs to default to 111b. If the I²C/SMBus Slave address must be changed to a different value, add pull-down resistors, to force the appropriate inputs to a logic Low state, and the Address bits that are to be logic High can remain unconnected. However, if the inputs that are logic High are connected to circuit traces, external pull-ups are recommended, because in such case, the internal pull-up resistors might not be strong enough to hold the input(s) High. ***Note:*** *Although this is an I/O signal, its logical operation is input.*
I2C_SCL0	OD	L8	YES ☐ NO ☐ UNKNOWN ☐	**I²C/SMBus Serial Clock Input** I²C/SMBus Clock source. I2C_SCL0 requires an external pull-up resistor.
I2C_SDA0	OD	N8	YES ☐ NO ☐ UNKNOWN ☐	**I²C/SMBus Serial Data I/O** Transmits and receives I²C/SMBus data during I²C/SMBus accesses to PEX 8680 registers. I2C_SDA0 requires an external pull-up resistor.

Device-Specific Signals

Device-Specific S defines the Device-Specific signals – signals that are unique to the PEX 8680.

Device-Specific Signals – 62 Balls

Signal Name	Type	Location	Pin Status	Description
FATAL_ERR#	O	B31	YES ☐ NO ☐ UNKNOWN ☐	**Fatal Error (6 Balls)** is used in Base mode, and in Virtual Switch mode for Virtual Switch 0. VS*x*_FATAL_ERR# are used only in Virtual Switch mode (one per each additional virtual switch – Virtual Switches 7 through 1, respectively). Asserted Low when a Fatal error is detected in the PEX 8680 and the following conditions exist (all the same conditions that are required to send a Fatal Error message to the Host): • Specific error is defined as *Fatal* in the **Uncorrectable Error Severity** register (offset FC0h), and • Reporting of the specific error condition is disabled, not masked by the corresponding bit of the **Uncorrectable Error Mask** register (offset FBCh), and • **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]) –or– **PCI Command** register *SERR# Enable* bit (offset 04h[8]) is Set The **Device Status** register *Fatal Error Detected* bit is Set (offset 70h[18]=1), and the specific error is flagged in the **Uncorrectable Error Status** register (offset FB8h). No pull up required.
VS5_FATAL_ERR# VS4_FATAL_ERR# VS3_FATAL_ERR# VS2_FATAL_ERR# VS1_FATAL_ERR#	O	C32, C33, AD24, AD26, AD27	YES ☐ NO ☐ UNKNOWN ☐	

Signal Name	Type	Location	Pin Status	Description
GPIO[15:12]	I/O PU	AF24, AB25, AA27, AA28	YES ☐ NO ☐ UNKNOWN ☐	**Programmable General-Purpose I/O (4 Balls)** GPIO[15:12] function as general-purpose inputs, interrupt inputs, or general-purpose outputs, as outlined below. **General-Purpose Inputs** For GPIO[15:12] signals that are configured as general-purpose inputs (by STRAP_TESTMODE[4:0] signal strapping sampled at reset, with values 01111b or 01100b), or by subsequent programming (by serial EEPROM, I2C, or software) of the appropriate **GPIO *x* Direction Control** register (Port 0, except in Base mode if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Endpoint, offset 604h) values, Input signal states are reflected in the **GPIO 0_23 Input Data** register (Port 0, except in Base mode if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Endpoint, offset 61Ch). Inputs can be internally de-bounced, by setting the corresponding **GPIO 0_23 Input De-Bounce** register bits (Port 0, except in Base mode if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Endpoint, offset 614h). Debouncing is disabled, by default; if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched. **Interrupt Inputs** For GPIO[15:12] signals that are configured as Interrupt inputs in the **GPIO *x* Direction Control** registers, Input signal states are reflected in the **GPIO 0_23 Interrupt Status** register (Port 0, except in Base mode if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Endpoint, offset 634h). Inputs can be internally de-bounced, by setting the corresponding **GPIO 0_23 Input De-Bounce** register bits (Port 0, except in Base mode if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Endpoint, offset 614h). Debouncing is disabled, by default; if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched. Interrupt polarity (Active-High or Active-Low) is individually programmable in the **GPIO 0_23 Interrupt Polarity** register (Port 0, except in Base mode if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Endpoint, offset 62Ch). Interrupt generation can be selectively masked in the **GPIO 0_23 Interrupt Mask** register (Port 0, except in Base mode if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Endpoint, offset 63Ch). **General-Purpose Outputs** For GPIO[15:12] signals that are configured as general-purpose outputs (in the GPIO *x* Direction Control registers, output signal states are controlled by the corresponding bit values in the GPIO 0_23 Output Data register (Port 0, except in Base mode if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Endpoint, offset 624h).

Signal Name	Type	Location	Pin Status	Description
GPIO[42:24]	I/O PU	E32, G28, C30, C3, C5, M7, L12, P9, AB8, AB9, AC9, AM3, AL3, AG11, AH8, AH23, AK32, P28, D33	YES ☐ NO ☐ UNKNOWN ☐	**General-Purpose I/O (19 Balls)** Default functionality is determined at Fundamental Reset; however, functionality can be switched by programming the **GPIO** registers using serial EEPROM, I^2C, or software. provide GPIO input functionality, by default, when the signal values sampled at Fundamental Reset (input de-assertion) are either 01011b or 01111b (0Bh or 0Fh, respectively). Alternatively, when the signals sampled at Fundamental Reset are either 01100b or 01101b (0Ch or 0Dh, respectively), function as PERST# Reset outputs, by default. If Serial Hot Plug is implemented (using external I^2C I/O Expanders), it is recommended that the signals be strapped as PERST# Reset outputs and routed to the slots, rather than using the PERST# outputs from the I/O Expanders.

<table>
<tr>
<td>PEX_INTA#</td>
<td>OD</td>
<td>E3</td>
<td>YES ☐
NO ☐
UNKNOWN ☐</td>
<td rowspan="2">Interrupt Output (6 Balls)

PEX_INTA# is used in Base mode, and in Virtual Switch mode for Virtual Switch 0.

VSx_INTA# outputs are used only in Virtual Switch mode (one per each additional virtual switch – Virtual Switches 7 through 1, respectively).

If not used, these balls can be left unconnected.

Interrupt output is enabled if:
• INTx Messages are enabled (PCI Command register Interrupt Disable bit, offset 04h[10]=0), and MSI is disabled (MSI Control register MSI Enable bit, offset 48h[16]=0)
• PEX_INTA# output is enabled (ECC Error Check Disable register Enable Ball for x Interrupt bits, offset 720h[9, 8, 7, 6, 5, and/or 4]=1)

The three interrupt mechanisms are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources:
• Conventional PCI INTx Message generation
• Native MSI transaction generation
• Device-Specific assertion

PEX_INTA# and/or VSx_PEX_INTA# assertion indicates that one or more of the following events and/or errors (if not masked) were detected:
• Hot Plug Events
• PCI Express Hot Plug events
• General-Purpose Input Interrupt events
• Device-Specific Error Conditions
• Device-Specific NT Link Port events
• NT Virtual Doorbell events
• NT Link Doorbell events
• Management Port Doorbell-Generated interrupts
• Management Link Status Events

Refer to data book Section 9.1.1, “Interrupt Sources or Events” for details.</td>
</tr>
<tr>
<td>VS5_PEX_INTA#
VS4_PEX_INTA#
VS3_PEX_INTA#
VS2_PEX_INTA#
VS1_PEX_INTA#</td>
<td>OD</td>
<td>H13,
J13,
AH24,
AE26,
AC25</td>
<td>YES ☐
NO ☐
UNKNOWN ☐</td>
</tr>
</table>

PEX_NT_RESET#	O	AN32	YES ☐ NO ☐ UNKNOWN ☐	**Active-Low Output Used to Propagate Reset in NT Mode** Pulse width is 1 µs.
PEX_PORT_GOOD[23 :16, 11:0]#	I/O PU	H11, K12, J9, J11, N10, N9, D2, AF22, AB24, AB28, AA26, AA25, M8, P8, N7, P10, W10, AA8, M10, M9	YES ☐ NO ☐ UNKNOWN ☐	**Active-Low PCI Express Port Linkup Status Indicator Outputs for Ports 23 through 16 and 11 through 0 –or– Programmable General-Purpose I/O (20 Balls)** PEX_PORT_GOODx# signals function as general-purpose inputs, interrupt inputs, general-purpose outputs, or as the PORT_GOOD function, as outlined below. **General-Purpose Inputs** For PEX_PORT_GOODx# signals that are configured as general-purpose inputs (by STRAP_TESTMODE[4:0] signal strapping sampled at reset with values 01111b or 01100b, or by subsequent programming (by serial EEPROM, I^2C, or software) of the appropriate **GPIO *x* Direction Control** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 600h, 604h, and 608h) values, Input signal states are reflected in the **GPIO 0_23 Input Data** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 61Ch). Inputs can be internally de-bounced, by setting the corresponding bits in the **GPIO 0_23 Input De-Bounce** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 614h); if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched. **Interrupt Inputs** For PEX_PORT_GOODx# signals that are configured as Interrupt inputs in the **GPIO *x* Direction Control** registers, Input signal states are reflected in the **GPIO 0_23 Interrupt Status** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 634h). Inputs can be internally de-bounced, by setting the corresponding bits in the **GPIO 0_23 Input De-Bounce** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 614h); if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched. Interrupt polarity (Active-High or Active-Low) is individually programmable in the **GPIO 0_23 Interrupt Polarity** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 62Ch). Interrupt generation can be selectively masked in the **GPIO 0_23 Interrupt Mask** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 63Ch). Continued…

PEX_PORT_GOOD[23:16, 11:0]#	I/O PU	H11, K12, J9, J11, N10, N9, D2, AF22, AB24, AB28, AA26, AA25, M8, P8, N7, P10, W10, AA8, M10, M9	YES ☐ NO ☐ UNKNOWN ☐	Continued… **General-Purpose Outputs** For PEX_PORT_GOODx# signals that are configured as general-purpose outputs (in the **GPIO *x* Direction Control** registers, output signal states are controlled by the corresponding bit values in the **GPIO 0_23 Output Data** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 624h). **PORT_GOOD Function** For PEX_PORT_GOODx# signals that correspond to enabled Ports and are configured for PORT_GOOD functionality (by STRAP_TESTMODE[4:0] signal strapping sampled at reset with values 01011b or 01101b, or by subsequent programming (by serial EEPROM, I^2C, or software) of the appropriate **GPIO *x* Direction Control** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 600h, 604h, and 608h) values. The Output signal states are not directly available from a single register (due to encoded, possibly blinking output); however, software can determine LANE_GOOD status (Physical Layer Link status for each Lane) from the **Station *x* Lane Status** registers (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 330h, 334h, and 338h). Software can also determine Maximum Link Width and Maximum Link Speed from the **Link Capability** register in each Port (offset 74h[9:4, 3:0], respectively, as well as Negotiated Link Width and Current Link Speed from the **Link Status** register in each Port (offset 78h[25:20, 19:16], respectively). The **Link Capability** and **Link Status** registers in the NT Port Virtual Interface follow the NT Port Link Interface configuration, and contain the same values as the corresponding NT Port Link Interface registers. If PORT_GOOD functionality is enabled, but some Ports are not enabled due to STRAP_STN*x*_PORTCFG*x* signal settings, the signals associated with non-enabled Ports function as GPIO signals. LED behavior when connected to signals: • **Off** – Link is down • **On** – Link is up, 5.0 GT/s, all Lanes are up • **Blinking, 0.5 seconds On, 0.5 seconds Off** – Link is up, 5.0 GT/s, reduced Lanes are up • **Blinking, 1.5 seconds On, 0.5 seconds Off** – Link is up, 2.5 GT/s, all Lanes are up • **Blinking, 0.5 seconds On, 1.5 seconds Off** – Link is up, 2.5 GT/s, reduced Lanes are up

VS5_PERST# VS4_PERST# VS3_PERST# VS2_PERST# VS1_PERST# VS0_PERST#	I/O PU	J12, H12, AC26, AL32, AM34, AL33	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**Virtual Switch Fundamental Reset (6 Balls)** Fundamental Reset signal for Virtual switches 5 through 0, respectively. In Virtual Switch mode, assert VSx_PERST# low to cause a Fundamental Reset (PERST#) (one per virtual switch). In Base Mode, VSx_PERST# inputs must be pulled or tied high. (Refer to Section 5.1.2, "Virtual Switch Mode (Mode2) Resets," for further details.) ***Note:*** *The PEX_PERST# signal, defined in PCI Express Signals, is the Reset input used in Base mode.*

External Resistor Signals

External Resistor Signals – 20 Balls

Signal Name	Type	Location	Pin Status	Description
REXT_A[11:8, 5:0]	A	F10, K6, J29, U29, F17, F25, AJ25, AF29, AJ18, AL9	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**External Resistor Balls (10 Balls)** One pair per SerDes block (paired with the "B" signal). **Must attach a 1.43KΩ 1% resistor between each REXT_A and REXT_B pair.** **Do not connect to any other signal, power, or ground.**
REXT_B[11:8, 5:0]	A	G10, K7, J28, U28, G17, G25, AH25, AF28, AH18, AK9	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**External Resistor Balls (10 Balls)** One pair per SerDes block (paired with the "A" signal). **Must attach a 1.43KΩ 1% resistor between each REXT_A and REXT_B pair.** **Do not connect to any other signal, power, or ground.**

No Connect Signals

Caution: ***Do not connect these balls to board electrical paths. These balls are internally connected to the device.***

No Connect Signals – 120 Balls

Signal Name	Type	Location	Pin Status	Description
N/C	***Reserved***	D4, D32, F9, F18, F26, G9, G13, G18, G26, H10, H17, H25, J6, J7, J27, K8, K11, K13, K28, K29, M26, P1, P2, P4, P5, R1, R2, R4, R5, T1, T2, T4, T5, U1, U2, U4, U5, U6, U7, U27, V1, V2, V4, V5, V6, V7, V8, V28, V29, W1, W2, W4, W5, W9, Y1, Y2, Y4, Y5, AA1, AA2, AA4, AA5, AB1, AB2, AB4, AB5, AC1, AC2, AC4, AC5, AD1, AD2, AD4, AD5, AE1, AE2, AE4, AE5, AE6, AE7, AE24, AE28, AE29, AF1, AF2, AF4, AF5, AF6, AF7, AF8, AF25, AF27, AG1, AG2, AG4, AG5, AG18, AG25, AH1, AH2, AH4, AH5, AH17, AH26, AJ1, AJ2, AJ4, AJ5, AJ9, AJ17, AJ26	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**No Connect (111 Balls)** Do not connect these balls to board electrical paths. **Note:** N/C balls now include balls AE24 and AF25, which are defined in the 0.87 version of the data book as THERMAL_DIODEn and THERMAL_DIODEp, respectively.
SPARE[8:0]	I/O PU	AG19, AG21, AG20, AG22, AC27, AB27, Y7, AB7, J10	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**Spare (9 Balls)** ***Reserved for future use*** Do not connect these balls to board electrical paths.

Power and Ground Signals

Power and Ground Signals – 527 Balls

Signal Name	Type	Location	Pin Status	Description
VDD10	CPWR	L13, L15, L17, L19, L21, L23, M12, M14, M16, M18, M20, M22, N13, N15, N17, N19, N21, N23, P12, P14, P16, P18, P20, P22, R13, R15, R17, R19, R21, R23, T12, T14, T16, T18, T20, T22, U13, U15, U17, U19, U21, U23, V12, V14, V16, V18, V20, V22, W13, W15, W17, W19, W21, W23, Y12, Y14, Y16, Y18, Y20, Y22, AA13, AA15, AA17, AA19, AA21, AA23, AB12, AB14, AB16, AB18, AB20, AB22, AC13, AC15, AC17, AC19, AC21, AC23, AD12, AD14, AD16, AD18, AD20, AD22	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**1.0V ±5% Power for Core Logic (84 Balls)**
VDD10A	APWR	G14, G15, G16, G19, G20, G21, G22, G23, G24, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, L7, L26, L28, M28, N11, N24, P11, P24, R7, R9, R24, R26, T7, T9, T11, T24, T28, U9, U11, U26, V9, V11, V24, V26, W7, W26, W28, Y11, Y24, Y26, Y28, AA11, AA24, AB11, AC7, AD7, AD9, AE9, AF11, AF12, AF13, AF14, AF15, AF16, AF17, AF18, AF19, AF20, AF21, AH9, AH10, AH11, AH12, AH13, AH14, AH15, AH16, AH19, AH20, AH21, AH22	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**1.0V ±5% Power for SerDes Analog Circuits (81 Balls)**
VDD25	I/OPWR	A2, A3, A32, A33, B1, B34, E30, G7, G8, G27, H7, H24, K10, K25, K26, L9, L24, M11, R27, Y8, AC24, AD11, AD23, AD28, AE10, AE11, AE25, AF10, AF23, AG7, AG9, AG28, AH27, AK31, AN1, AP2, AP3, AP33	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**2.5V ±10% Power for I/O Logic Functions (38 Balls)**
VDD25A	PLLPWR	K14, K17, K20, M24, R11, U24, W11, W24, AC11, AE15, AE18, AE21	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**2.5V ±10% Power for PLL Circuits (12 Balls)**

Signal Name	Type	Location	Pin Status	Description
VSS	GND	A1, A34, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, F3, F6, F7, F8, F11, F12, F13, F14, F15, F16, F19, F20, F21, F22, F23, F24, F27, F28, F29, F32, G3, G6, G29, G32, H3, H6, H16, H18, H19, H20, H21, H22, H23, H26, H29, H32, J3, J8, J25, J32, K3, K15, K16, K18, K19, K21, K22, K23, K24, K27, K32, L3, L6, L14, L16, L18, L20, L22, L25, L27, L29, L32, M3, M6, M13, M15, M17, M19, M21, M23, M25, M29, M32, N3, N6, N12, N14, N16, N18, N20, N22, N25, N29, N32, P3, P6, P13, P15, P17, P19, P21, P23, P25, P29, P32, R3, R6, R8, R10, R12, R14, R16, R18, R20, R22, R25, R29, R32, T3, T6, T8, T10, T13, T15, T17, T19, T21, T23, T29, T32, U3, U8, U10, U12, U14, U16, U18, U20, U22, U25, U32, V3, V10, V13, V15, V17, V19, V21, V23, V25, V27, V32, W3, W6, W12, W14, W16, W18, W20, W22, W25, W27, W29, W32, Y3, Y6, Y10, Y13, Y15, Y17, Y19, Y21, Y23, Y25, Y27, Y29, Y32, AA3, AA6, AA12, AA14, AA16, AA18, AA20, AA22, AA29, AA32, AB3, AB6, AB10, AB13, AB15, AB17, AB19, AB21, AB23, AB29, AB32, AC3, AC6, AC10, AC12, AC14, AC16, AC18, AC20, AC22, AC29, AC32, AD3, AD6, AD8, AD10, AD13, AD15, AD17, AD19, AD21, AD29, AD32, AE3, AE8, AE12, AE13, AE14, AE16, AE17, AE19, AE20, AE22, AE27, AE32, AF3, AF32, AG3, AG6, AG12, AG13, AG14, AG15, AG16, AG17, AG29, AG32, AH3, AH6, AH29, AH32, AJ3, AJ6, AJ7, AJ8, AJ10, AJ11, AJ12, AJ13, AJ14, AJ15, AJ16, AJ19, AJ20, AJ21, AJ22, AJ23, AJ24, AJ27, AJ28, AJ29, AJ32, AM5, AM6, AM7, AM8, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM16, AM17, AM18, AM19, AM20, AM21, AM22, AM23, AM24, AM25, AM26, AM27, AM28, AM29, AP1, AP34	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**Ground Connections (312 Balls)**

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Additional Schematic Guidelines

Power Sequencing

The PEX 8680 does not require its power supplies to be sequenced in a specific order.

Reset

The PEX 8680 latches the PEX_PERST# input reset assertion. Refer to the PEX 8680 RDK Hardware Reference Manual for suggested reference circuits for Power On Reset and Power Valid detection.

Mid-Bus Probe Pads

If your design contains an embedded PCIe link, for example, PCIe connection(s) between the PEX 8680's port(s) and endpoint(s) embedded on the same board. It is very useful to add probe pads to your PCB design for each embedded PCIe link connected to the PEX 8680. Probe pads can be very helpful when you need to debug a problem on a PCIe link with a PCIe analyzer. PCIe Analyzer Manufacturer's provide circuitry, called Mid-Bus Probes, to help you debug embedded links. If you do plan to implement Mid-Bus Probe footprints in your PCB design, be aware that it may induce jitter and/o reduce signal integrity on the PCIe lanes it is connected to. Each Manufacturer will usually provide a probe footprint to be implemented on the board for debugging purposes. For more information regarding this, please contact PLX Technical Applications.

Spread Spectrum Clocking (SSC)

The PEX 8680 supports a Spread Spectrum REFCLK source. The SSC clock *must* originate from the PCIe connector on a slot in the motherboard or through a common clock source that is being distributed to all add-in cards and/or PCIe devices in the system.
If your REFCLK source is non-SSC, then you may have separate REFCLK sources on different cards or devices as long as their frequency difference is within +/- 300ppm. (~30ps for a 100Mhz Clock source) Please refer to the PEX 8680 Quick Start Design Guide for more information.

General PCB Routing Guidelines

Note: The following guidelines were provided for PCIe 2.5 GT/s transmission lines. On the PCIe 5.0 GT/s signaling by increasing the pre-emphasis and increasing receiver sensitivity are supposed to counteract the bandwidth related losses associated with the frequency increase. However, as frequency goes up, other discontinuities become more of a factor not just the simple channel loss. We strongly recommend you simulate and verify your design at the operating frequency.

Since PCIe links operate are very high speeds, proper PCB routing of each RX and TX pair in each lane is critical for maintaining signal integrity on each PCIe link. The PCI-SIG provides numerous suggestions about how to correctly design PCB's containing PCIe links. Several important guidelines are listed below. Additional information is available from the PCI-SIG website.

1. Recommended Microstrip Trace Routing Guidelines:
   - Differential Impedance 4, 6 layer: 100 Ohms +/- 20% 8, 10 layer: 85 Ohms +/- 20%
   - Single ended Impedance 4, 6 layer: 60 Ohms +/- 15% 8, 10 layer: 55 Ohms +/- 15%
2. Recommended Stripline Trace Routing Guidelines:
   - Differential Impedance 6 layer: 100 Ohms +/- 15% 8, 10 layer: 85 Ohms +/- 15%
   - Single ended Impedance 6 layer: 60 Ohms +/- 15% 8, 10 layer: 55 Ohms +/- 15%
3. Recommended for all differential signal pairs: maintain >= 20 mil trace edge to plane edge gap
4. Recommended Length matching Intra-pair: max 5 mil delta, matching maintained segment to segment, match at point of discontinuity, but avoid "tight bends"
5. Gnd referenced signals is recommended. Use stitching caps with PWR referenced signal traces.
6. Use Gnd stitching vias by signal layer vias for layer changes
7. Do not route over plane splits or voids. Allow no more than 1/2 trace width routed over via antipad
8. Match left/right turn bends where possible. No 90-degree bends or "tight" bend structures.
9. The reference clock signal pair should maintain the same reference plane for the entire routed length and should not cross any plane splits (breaks in the reference plane)
10. Reference clock terminating components should be placed as close as possible to their respective device, ideally within 100 mils of the clock/receiver component pin
11. Match all segment lengths between differential pairs along the entire length of the pair.
12. Maintain constant line impedance along the routing path by keeping the same line width and line separation.
13. Avoid routing differential pairs adjacent to noisy signal lines or high speed switching devices such as clock chips.
14. Recommended reference clock differential pair spacing (clock to clock#) < = 11.25 mils.
15. Recommended reference clock trace spacing to other traces is >= 20 mils.
16. Recommended reference clock line width >= 5 mils.
17. When routing the 100Mhz differential clock, do not divide the two halves of the clock pair between layers.
18. Recommended reference clock trace impedance:

- Single ended: 50-60 Ohms +/- 15%
- Differential: 100 Ohms +/- 20%

19. Recommended PCI Express reference clock to PCI express reference clock length matching to within 25 mils
20. AC Coupling Capacitors: The same package size and value of capacitor should be used for each signal in a differential pair.
21. AC Coupling Capacitors: Locate capacitors for coupled traces in a differential pair at the same location along the differential traces. Place them as close to each other as possible.
22. AC Coupling Capacitors: The "breakout" into and out of the capacitor mounting pads should be symmetrical for both signal lines in a differential pair.
23. Test points and probing structures should not introduce stubs on the differential pairs.
24. Use Tantalum or Low ESR Lane AC Coupling Caps.