AVAGO TECHNOLOGIES | EXPRESS SWITCHING BY PLX

PEX 8604
Hardware Design Checklist

September 11, 2014
Revision 1.1

Revision History

- Rev 1.1: On page 5, Correction in Recommendation column of STRAP_PORTCFG[1:0] for x2x2 from HH to HL and HH changed to Reserved.

Introduction

This document is intended for systems design engineers incorporating the PEX 8604 PCI Express switch into a system hardware design. It provides a handy list of basic design checks covering schematic and printed-circuit board (PCB) layout designs. Including these checks as part of your design review can help insure that important details are not overlooked when your design is committed to hardware, thereby improving your chances for a successful bring-up. In preparation for your design review, we also recommend that you check our website, www.plxtech.com, and download the most current technical specifications, errata, and related documentation. This document supersedes and replaces previously released versions.

1 Schematic Design Checks

This section includes checks on basic elements of the circuit design, including schematic symbol, power supply, configuration straps, clocks, reset, configuration serial EEPROM, I2C, JTAG, GPIO, and other signals. All power and signal balls on the device are covered.

1.1 Schematic Symbol

For designers using ORCAD schematic capture tools, an ORCAD symbol library is available on the PLX website at www.plxtech.com. This library symbol is pre-checked by PLX engineers, and it is also used in the design of the PEX 8604 RDK.

For designers not using the PLX-supplied schematic symbol, we highly recommend double-checking your symbol's signal ball names and numbers for accuracy before using the symbol in your schematic design.

1.2 Power Supply

1.2.1 Regulated DC Supply Voltages

The PEX 8604 requires the following regulated DC voltages:

- ☐ VDD10: 1.0 Volts, +/- 5% - Powers digital core logic
- ☐ VDD25: 2.5 Volts, +/- 10% - Powers external I/O signals

These DC supplies can be sequenced on or off in any order. Refer to the data book for specific load current requirements.

1.2.2 Filtered Analog Supply Voltages

From the VDD10 and VDD25 supplies, the following analog supply voltages are derived:

- ☐ VDD10A: 1.0 Volts, filtered from VDD10, powers PCI Express SerDes signals
- ☐ VDD25A: 2.5 Volts, filtered from VDD25, powers internal clock PLL

1.2.3 Power, Ground Ball Connections

Signal Name	Ball #	Signal Type	Checked	Recommendations
VDD10	D5, D6, D9, D10, E4, E11, G4, G11, H4, H11, K4, K11, L5, L6, L9, L10	CPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**1.0 V Power for Core Logic (16 Balls)** PEX 8604 RDK Decoupling Scheme: 16 Caps 1000 pF 0201 caps at each power ball 4 Caps 0.1 uF near device 2 Caps 1uF near device
VDD10A	D7, D8, L7, L8	APWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**1.0 V Power for SerDes Analog Circuits (4 Balls)** Tie to VDD10. PEX8604 RDK Decoupling Scheme: 4 Caps 1000 pF 0201 caps at each power ball 4 Caps 0.1 uF near device 2 Caps 1uF near device
VDD25	D4, D11, L4, L11	I/OPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**2.5V Power for I/O Logic Functions (4 Balls)** PEX 8604 RDK Decoupling Scheme: 4 Caps 1000 pF 0201 caps at each power ball. 2 Caps 0.1µF near device 2 Caps 1 µF near device
VDD25A	C8, G3, G12, M7	PLLPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**2.5V Power for PLL Circuits (4 Balls)** Tie to VDD25. PEX 8604 RDK Decoupling Scheme: 4 Caps 1000 pF 0201 caps at each power ball. 2 Caps 0.1µF near device 2 Caps 1 µF near device
VSS, VSS_THERMAL	C5, C6, C9-11, E5-10, F5-10, G5-10, H3, H5-10, J5-10, K5-10, M5, M6, M9-11	GND	***YES*** ☐ ***NO*** ☐ **UNKNOWN** ☐	**Ground Connections (46 Balls)**

1.3 Clocks

1.3.1 Clock Source and Line Termination

REFCLK Source	Signal Type	Checked	Requirements
External REFCLK Clock Transmitter	External-CML	**YES**☐ **NO**☐ **UNKNOWN** ☐	Frequency Tolerance: ± 300 ppm, max. 33 Ω series (in-line) and 49 Ω shunt (to GND) required on each differential signal, near the clock source.

1.3.2 Clock Input Balls

Signal Name	Ball #	Signal Type	Checked	Recommendations
PEX_REFCLKn , PEX_REFCLKp	P8, N8	CML Input	YES☐ NO☐ UNKNOWN ☐	**100 MHz PCI Express Reference Clock input pair.** When Dual Clocking is enabled, these are the Spread-Spectrum Clocking (SSC) domain signals. Requires 100nF AC coupling capacitor in series with each differential signal.
PEX_REFCLKCFCn, PEX_REFCLKCFCp	A7, B7	CML Input	YES ☐ NO ☐ UNKNOWN☐	**100 MHz PCI Express Constant-Frequency Clock Input Signal pair.** When Dual Clocking is enabled, these are the Constant-Frequency Clocking (CFC) domain signals. Requires 100nF AC coupling capacitor in series with each differential signal. When Dual Clocking is not used, these signals can be left floating.

1.4 Reset

Signal Name	Ball #	Signal Type	Checked	Recommendations
PEX_PERST#	H13	I	YES ☐ NO ☐ UNKNOWN ☐	**PCI Express Reset** Used to initiate a fundamental reset. This reset is propagated to all downstream ports, except those configured as NT.
PEX_NT_RESET#	L13	O	YES ☐ NO ☐ UNKNOWN ☐	**NT Port Reset** Active-Low Output Used to Propagate Reset across an NT Port

1.5 Configuration Straps

Signal Name	Ball #	Signal Type	Checked	Recommendations
STRAP_DEBUG_SEL0#	J11	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Pull high to VDD25 for normal operation.
STRAP_FAST_BRINGUP#	C3	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Pull high to VDD25 for normal operation.
STRAP_NT_ENABLE#	H12	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	**Enable NT Mode** Tie to Ground (VSS) to enable NT mode, otherwise, pull high to VDD25
STRAP_NT_UPSTRM_PORTSEL[3:0]	M3, K3, J2, J3	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	**Non-Transparent Upstream Port Select Straps (4 Balls)** Binary value selects port number. See data book for additional details. L = Tie to Ground; H = Pull or tie to VDD25: LLLL=Port 0 LLLH=Port1 LHLL=Port4 LHLH=Port5 All other encodings are reserved.
STRAP_UPSTRM_PORTSEL[3:0]	G2, H2, F1, F3	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	**Upstream Port Select Straps (4 Balls)** Binary value selects port number. See data book for additional details. L = Tie to Ground; H = Pull or tie to VDD25: LLLL=Port 0 LLLH=Port1 LHLL=Port4 LHLH=Port5 All other encodings are reserved
STRAP_PLL_BYPASS#	M12	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Pull high to VDD25 for normal operation.
STRAP_PROBE_MODE#	K13	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Pull high to VDD25 for normal operation.
STRAP_SERDES_MODE_EN#	C4	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Pull high to VDD25 for normal operation.

Signal Name	Ball #	Signal Type	Checked	Recommendations
STRAP_PORTCFG[1:0]	B2, A1	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	**Port Configuration Straps (2 balls)** Binary value selects port number. See data book for additional details. L = Tie to Ground; H = Pull or tie to VDD25: LL = x1, x1, x1, x1 LH = x2, x1, x1 HL = x2, x2 HH = *Reserved*
STRAP_RESERVED17#	F4	ISTRAP	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Pull high to VDD25 for normal operation.
STRAP_SSC_ISO_ENABLE#	M4	ISTRAP	YES ☐ NO ☐ UNKNOWN ☐	**Enable Spread-Spectrum Clocking** Tie to Ground (VSS) to enable spread-spectrum clock isolation, otherwise, pull high to VDD25
STRAP_TESTMODE[3:0]	N13, M14, N14, P13	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Pull high to VDD25 for normal operation.
STRAP_RESERVED16	D13	I STRAP	YES ☐ NO ☐ UNKNOWN ☐	***Reserved*** Connect this ball to Ground (VSS).
STRAP_SPARE0#	K2	***Reserved***	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Do not connect this ball to board electrical paths.
STRAP_SPARE1#	L2	***Reserved***	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Pull high to VDD25 for normal operation.
STRAP_UPCFG_TIMER_EN#	C1	ISTRAP	YES ☐ NO ☐ UNKNOWN ☐	**Enable Up-Config Timer** Tie to ground to enable up-config timer.
STRAP_SMBUS_EN#	L1	ISTRAP	YES ☐ NO ☐ UNKNOWN ☐	**Enable SMBus** Tie to ground to enable SMBus.
STRAP_NT_P2P_EN#	G1	ISTRAP	YES ☐ NO ☐ UNKNOWN ☐	**Enable Legacy Mode NT** Tie to ground to enable Legacy mode NT. Pull high to VDD25 to enable Vista compliant NT mode

1.6 PCI Express Interface

Signal Name	Ball #	Signal Type	Checked	Recommendations
PEX_LANE_GOOD[5, 4, 1, 0]#	B14, B1, M13, P14	I/O	YES ☐ NO ☐ UNKNOWN ☐	**Active-Low PCI Express Lane Linkup Status Indicator Outputs for lanes 5, 4, 1 and 0 (4 Balls)** These signals can directly drive common-anode LED modules (external current-limiting resistors are required).
PEX_PERn[5, 4, 1, 0]	B10, B12, N5, N3	CMLRn	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Receiver Differential Signal Pairs for lanes 5, 4, 1 and 0 (4 Balls)**
PEX_PERp[5, 4, 1, 0]	A10, A12, P5, P3	CMLRp	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Receiver Differential Signal Pairs for lanes 5, 4, 1 and 0 (4 Balls)**
PEX_PETn[5, 4, 1, 0]	B9, B11, N6, N4	CMLTn	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of PCI Express Transmitter Differential Signal for lanes 5, 4, 1 and 0 (4 Balls)** 100 nF AC coupling caps required on all PCI Express transmit pairs.
PEX_PETp[5, 4, 1, 0]	A9, A11, P6, P4	CMLTp	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of PCI Express Transmitter Differential Signal Pairs for lanes 5, 4, 1 and 0 (4 Balls)** 100 nF AC coupling caps required on all PCI Express transmit pairs.

1.7 Serial EEPROM

As of this writing, a serial configuration EEPROM is ***not required*** for the PEX 8604. Use of a serial configuration EEPROM in systems designs is optional. However, we highly recommend including the serial EEPROM circuit as a stuffing option, to allow inclusion of EEPROM-based performance enhancements and/or errata workarounds that may become available in the future.

1.7.1 Serial EEPROM Type

Use Atmel part number AT25256A or equivalent for programming the PEX 8604. Be sure to specify the '-1.8' version of the part, which can support operation at VCC voltage of 2.5Volts. Power the device from the VDD25 supply, bypassed with 0.1 uF.

1.7.2 Serial EEPROM Interface

Signal Name	Ball #	Signal Type	Checked	Recommendations
EE_CS#	J13	O	YES ☐ NO ☐ UNKNOWN ☐	**Serial EEPROM Chip Select Output.** Connect to EEPROM CS# input. Can be left floating if not used.
EE_DI	K14	O	YES ☐ NO ☐ UNKNOWN ☐	**Serial EEPROM Data Input (Write Data)** Connect to EEPROM serial data input, SI. Can be left floating if not used.
EE_DO	H14	I/PU	YES ☐ NO ☐ UNKNOWN ☐	**Serial EEPROM Data Output (Read Data)** Connect to EEPROM serial data output, SO. Weakly pulled up. Should be externally pulled high to VDD25

EE_SK	J14	O	YES ☐ NO ☐ UNKNOWN ☐	**Serial EEPROM Clock Output** Connect to EEPROM clock input, SCK. Can be left floating if not used.

1.7.3 Additional EEPROM Signals

- ☐ **WP#:** Tie to EEPROM VCC if not used, else jumper to GND to enable write-protect.
- ☐ **HOLD#:** Tie to EEPROM VCC

1.8 JTAG Interface

Signal Name	Ball #	Signal Type	Checked	Recommendations
JTAG_TCK	E13	I/PU	YES ☐ NO ☐ UNKNOWN ☐	**JTAG Test Clock Input** Frequency can be from 0 to 10 MHz. This signal is internally pulled up to VDD2.5 through a weak pull-up resistor. If this ball is connected to external board circuits, an external pull-up is also recommended.
JTAG_TDI	D12	I/PU	YES ☐ NO ☐ UNKNOWN ☐	**JTAG Test Data Input** This signal is internally pulled up to VDD2.5 through a weak pull-up resistor. If this ball is connected to external board circuits, an external pull-up is also recommended.
JTAG_TDO	E12	O	YES ☐ NO ☐ UNKNOWN ☐	**JTAG Test Data Output** Serial output from the JTAG TAP Controller test instructions and data. Can be left open (no connect) if JTAG interface is not used.
JTAG_TMS	D14	I/PU	YES ☐ NO ☐ UNKNOWN ☐	**JTAG Test Mode Select** This signal is internally pulled up to VDD2.5 through a weak pull-up resistor. If this ball is connected to external board circuits, an external pull-up is also recommended.
JTAG_TRST#	C13	I/PU	YES ☐ NO ☐ UNKNOWN ☐	**JTAG Test Reset** Pull to GROUND (VSS) through 1.5K ohms for normal operation

1.9 I²C Slave Interface Signals

Signal Name	Ball #	Signal Type	Checked	Recommendations
I2C_ADDR[2:0]	G14, F11, G13	I/PU	YES ☐ NO ☐ UNKNOWN ☐	**I²C Slave Address Bits 2 through 0 (3 Balls)** Used to configure the device address on the I²C Bus. If I²C or PEX_INTA# output is used, I2C_ADDR[2:0] should be strapped to a unique address, to avoid address conflict with any other I²C devices (on the same I²C Bus segment) that have the upper four bits of their 7-bit I²C Slave address also Set to 1011b. Must be pulled High to VDD25 or Low to VSS (GND) through external resistors.
I2C_SCL0	F14	I, OD	YES ☐ NO ☐ UNKNOWN ☐	**I²C Serial Clock** I²C Clock source. Requires an external pull-up resistor, the value of which depends on the I2C bus architecture. It must be strong enough to overcome I2C bus capacitance to meet timing, but weak enough that the OD drivers can sink the current. The PEX 8604 RDK uses a 2.26 KΩ Pull-up.

I2C_SDA0	F12	I/O, OD	YES ☐ NO ☐ UNKNOWN ☐	**I²C Serial Data** Transfers and receives I²C data. Requires an external pull-up resistor, the value of which depends on the I2C bus architecture. It must be strong enough to overcome I2C bus capacitance to meet timing, but weak enough that the OD drivers can sink the current. The PEX 8604 RDK uses a 2.26 KΩ Pull-up.

1.10 Serial Hot-Plug Controller Signals

Signal Name	Ball #	Signal Type	Checked	Recommendations
I2C_SCL1	F13	I, OD	YES ☐ NO ☐ UNKNOWN ☐	**I²C Serial Clock** I²C Clock source. Requires an external pull-up resistor, the value of which depends on the I2C bus architecture. It must be strong enough to overcome I2C bus capacitance to meet timing, but weak enough that the OD drivers can sink the current. The PEX 8604 RDK uses a 10 KΩ Pull-up.
I2C_SDA1	E14	I/O OD	YES ☐ NO ☐ UNKNOWN ☐	**I²C Serial Data** Transfers and receives I²C data. Requires an external pull-up resistor, the value of which depends on the I2C bus architecture. It must be strong enough to overcome I2C bus capacitance to meet timing, but weak enough that the OD drivers can sink the current. The PEX 8604 RDK uses a 10 KΩ Pull-up.
SHPC_INT#	C14	I	YES ☐ NO ☐ UNKNOWN ☐	**Serial Hot Plug Controller Interrupt** Active-Low signal used only by Hot Plug-capable Transparent downstream Ports. Pull high to VDD25 through 3.3K ohms.

1.11 Miscellaneous Signals

Signal Name	Ball #	Signal Type	Checked	Recommendations
GPIO[30, 29], GPIO[16:0]	A2, D3, K12, N2, M2, L3, P1, P2, M1, K1, H1, J1, J4, F2, E1, E2, E3, D1, D2	I/O	YES ☐ NO ☐ UNKNOWN ☐	**General-Purpose I/O (19 balls)**
THERMAL_DIODEn	C12	***Reserved***	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Do not connect this ball to board electrical paths.
THERMAL_DIODEp	A13	***Reserved***	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Do not connect this ball to board electrical paths.
REXT_A[1:0]	B8, P7		YES ☐ NO ☐ UNKNOWN ☐	Tie each REXT_A***n*** to REXT_B***n*** through a 1.43K ohms, 1% Resistor.
REXT_B[1:0]	A8, N7		YES ☐ NO ☐ UNKNOWN ☐	Tie each REXT_B***n*** to REXT_A***n*** through a 1.43K ohms, 1% Resistor.
PEX_INTA#	J12	OD	YES ☐ NO ☐ UNKNOWN ☐	**Interrupt Output** Assertion (Low) indicates that one or more events

Signal Name	Ball #	Signal Type	Checked	Recommendations
				and/or errors were detected. See data book for details. Pull high to VDD25 through 3.3K ohms.
FATAL_ERR#	B13	O	YES ☐ NO ☐ UNKNOWN ☐	**Fatal Error** Asserted Low when a Fatal error is detected in the PEX 8604. See data book for details. No pull up required.
NC	A3, A4, A5, A6, A14, B3, B4, B5, B6, C2, C7, L12, L14, M8, N1, N9, N10, N11, N12, P9, P10, P11, P12	No Connect	YES ☐ NO ☐ UNKNOWN ☐	**No Connect (23 Balls)** Do not connect these balls to board electrical paths.

1.12 Additional Schematic Design Considerations

1.12.1 PERST#

The PEX 8604 requires the PERST# signal to be asserted for at least 100ms after the board's power is stable to allow the chip to initialize correctly. Insure that Power On Reset and Power Valid detection circuitry implemented in your design meets this requirement. Refer to the PEX 8604 RDK Hardware Reference Manual for an example schematic.

1.12.2 Mid-Bus Probe Points

If your design contains embedded PCI Express links, it can sometimes be useful to add probe pads to your PCB design to allow instrumentation access to PCI Express links on the board. If you are planning to include mid-bus probe footprints in your PCB design, be aware that they may induce jitter and/or reduce signal integrity on the PCI Express lanes it is connected to. Refer to your instrumentation vendor's specifications for specific layout design considerations.

1.12.3 Spread Spectrum Clocking (SSC)

The PEX 8604 supports a Spread Spectrum REFCLK source. The SSC clock *must* originate from the PCI Express connector on a slot in the motherboard or through a common clock source that is being distributed to all add-in cards and/or PCI Express devices in the system.

If your REFCLK source is non-SSC, then you may have separate REFCLK sources on different cards or devices as long as their frequency difference is within ± 300ppm. (~30ps for a 100MHz Clock source) Refer to the PEX 8604 data book for more information.

2 PCB Layout Design Checks

Note: The following guidelines were provided for PCI Express 2.5 GT/s (Gen 1) transmission lines. On the Gen 2 PCI Express 5.0 GT/s signaling by increasing the pre-emphasis and increasing receiver sensitivity are supposed to counteract the bandwidth related losses associated with the frequency increase. However, as frequency goes up, other discontinuities become more of a factor not just the simple channel loss. We strongly recommend you simulate and verify your design at the operating frequency. HSPICE models are available on the PLX website.

Since PCI Express links operate at very high speeds, proper PCB routing of each RX and TX pair in each lane is critical for maintaining signal integrity on each PCI Express link. The PCI-SIG provides numerous suggestions about how to correctly design PCB's containing PCI Express links. Several important guidelines for proper layout of PCI Express SerDes signals are listed below. Additional information is available from the PCI-SIG website, www.pci-sig.com.

1. Recommended Microstrip Trace Impedance:
   - Differential Impedance: 85 Ω ± 20%
   - Single ended Impedance: 55 Ω ± 15%
2. Recommended Stripline Trace Impedance:

- Differential Impedance: 85 Ω ± 15%
- Single ended Impedance: 55 Ω ± 15%

3. Maintain ≥ 20 mil trace edge to plane edge gap
4. Match signal trace lengths to within 5 mils. Equalize using a snaked trace near the receive end if needed, but avoid "tight bends"
5. Route signals over continuous, un-broken planes.
6. Use GND-GND stitching vias near signal vias when routing between PCB layers
7. Do not route over plane splits or voids. Allow no more than 1/2 trace width routed over via antipad
8. Match left/right turn bends where possible. No 90-degree bends or "tight" bend structures.
9. The reference clock signal pair should maintain the same reference plane for the entire routed length and should not cross any plane splits (breaks in the reference plane)
10. Reference clock terminating components should be placed as close as possible to their respective driving sources, ideally within 100 mils of the clock/receiver component pin/ball.
11. Match all segment lengths between differential pairs along the entire length of the pair.
12. Maintain constant line impedance along the routing path by keeping the same line width and line separation.
13. Avoid routing differential pairs adjacent to noisy signal lines or high speed switching devices such as clock chips.
14. Recommended reference clock differential pair spacing (clock to clock#) ≤ 11.25 mils.
15. Recommended reference clock trace spacing to other traces is ≥ 20 mils.
16. Recommended reference clock line width ≥ 5 mils.
17. When routing the 100MHz differential clock, do not divide the two halves of the clock pair between layers.
18. Recommended reference clock differential impedance: 85 Ω ± 15%
19. Recommended PCI Express reference clock to PCI express reference clock length matching to within 25 mils
20. AC Coupling Capacitors: The same package size and value of capacitor should be used for each signal in a differential pair. Refer to the *PCI Express Base Specification* for permitted values.
21. AC Coupling Capacitors: Locate capacitors for coupled traces in a differential pair at the same location along the differential traces. Place them as close to each other as possible.
22. AC Coupling Capacitors: The "breakout" into and out of the capacitor mounting pads should be symmetrical for both signal lines in a differential pair. In addition, the area under the cap footprint should be voided of metal.
23. Test points and probing structures should not introduce stubs on the differential pairs.
24. Use Low ESR, ceramic caps for lane AC-coupling.

