PEX 8548
Schematic Design Checklist

June 20, 2007
Version 1.1

Purpose and Scope

The purpose of this document is to provide a checklist of recommendations to consider for successfully implementing the PEX 8548 device in your schematic and PCB design. It provides some basic guidelines to consider for your schematic design, PCB design and silicon choices. References to other PLX documents are also provided for more detailed information.

1 ORCAD Symbol

The ORCAD symbols for the PEX 8548 are shown Figure 1, 2 and 3 below. It is highly recommended you use these ORCAD symbols in your schematic designs rather than creating your own symbol. These ORCAD symbol files are available on the PLX website at www.plxtech.com.

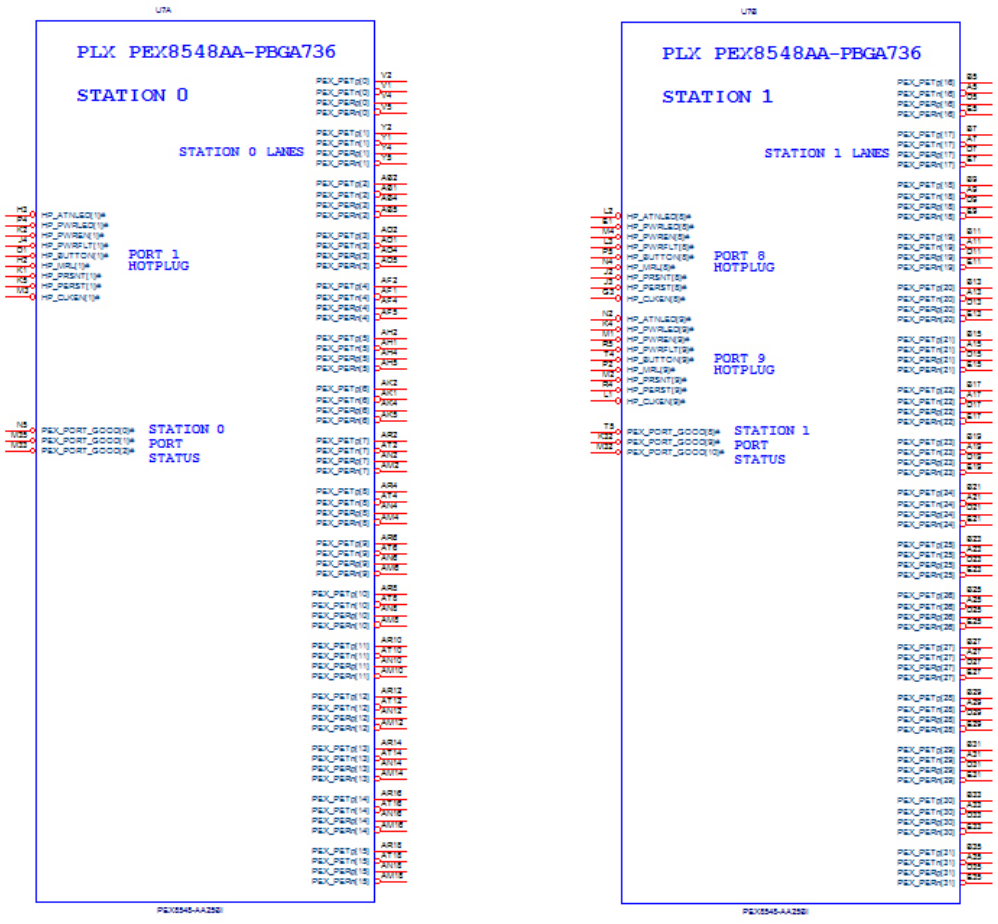

Figure 1. PEX 8548 ORCAD Symbol

PLX Technology, Inc, 870 Maude Avenue, Sunnyvale, CA 94085, Phone 408-774-9060, Fax 408-774-2169

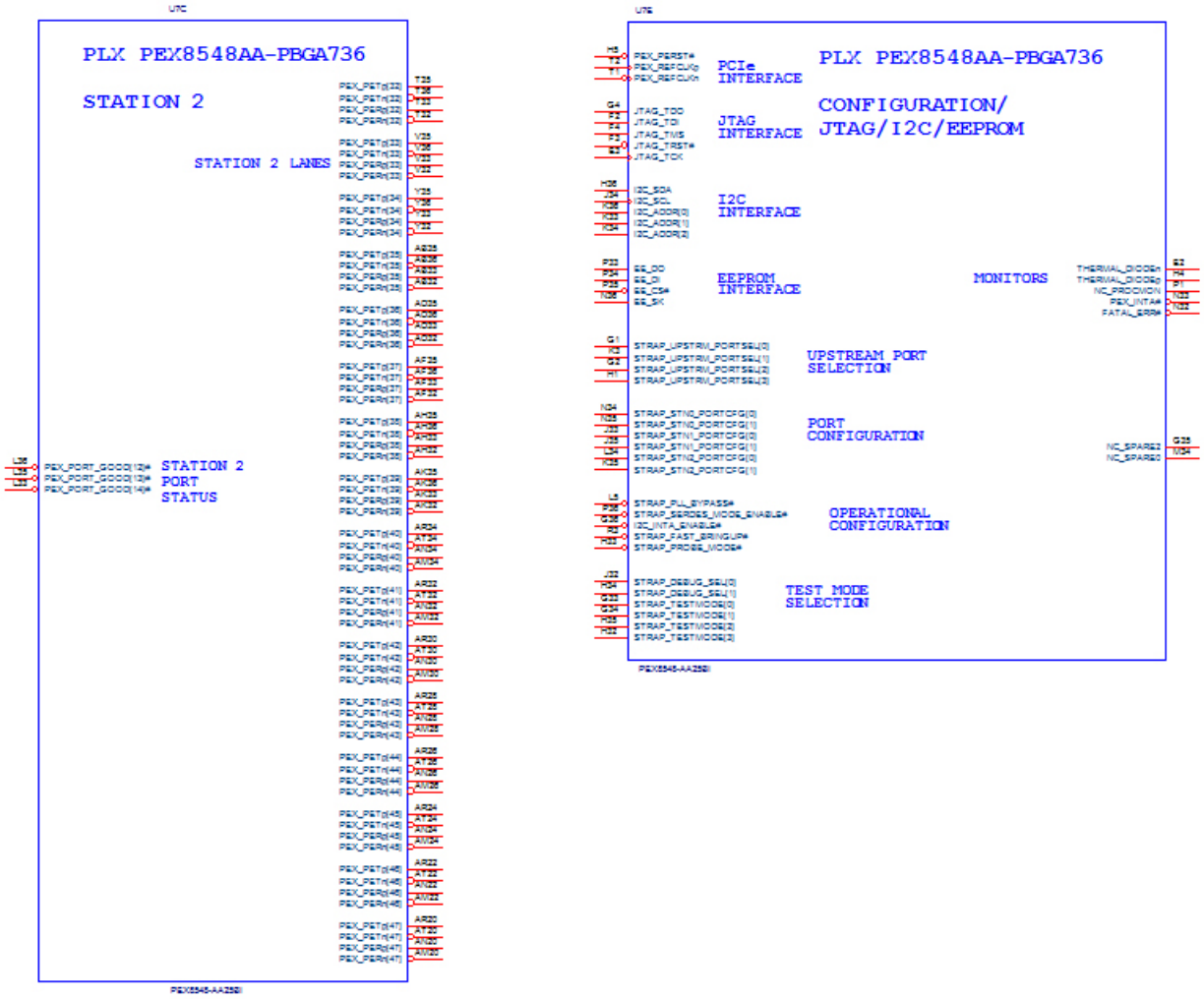

Figure 2. PEX 8548 ORCAD Symbol

Figure 3. PEX 8548 ORCAD Symbol

2 Silicon Requirements

The PEX 8548 is, as of the date of this document, shipping with revision AA silicon. If you have parts with this revision, a serial EEPROM is *not required* for this part. If you need and/or you have an EEPROM image, please contact the PLX Applications Group at apps-engineering@plxtech.com.

The known Errata, if any, associated with revision AA silicon may be fixed with an EEPROM. Please review the PEX 8548 Errata list for a list of known Errata.

This can be obtained from the PLX website at the following URL:
http://www.plxtech.com/products/pci_express/PEX 8548/default.asp.

An NDA is required to access the Errata Document. Please follow the instructions on the website for details.

3 Schematic Guidelines

Please review the PEX 8548 Quick Start Design Guide for important information above how to design with the PEX 8548. Another good reference guide is the schematic included in the PEX 8548 Hardware Reference Manual. This design has been extensively tested by PLX so it can make a good template to customize for your design with the PEX 8548.

3.1 Schematic Connections – Transparent Port

APPLICATION: **ADD-IN CARD** ☐ **EMBEDDED** ☐ **DAUGHTER CARD** ☐ **UNKNOWN** ☐

CUSTOMER: **DATE:**

8548 SCHEMATIC CHECKLIST

3.1.1 CLOCK INTERFACE:

Table 1. Transparent Port Clock Interface Connections

CLOCK SOURCES/ PIN NAMES	PIN #	TYPE	TERMINATION	RECOMMENDATIONS
PCI-EXPRESS				
External REFCLK Clock Transmitter	N/A	External-CML	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Recommended: 33Ohm series and 49Ohm shunt required on each differential Pair. **Maximum clock Frequency Tolerance allowed for REFCLK source is +/- 300PPM. Make sure your REFCLK oscillator supports this**
	N/A	External-LVPECL	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Please verify for your system. 100Ohm shunt required on each differential pair.
	N/A	External-LVDS	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Please verify for your system. 2KOhm coupling resistor required across differential signal pairs close to PEX 8548 Clock inputs
PEX_REFCLKn Input	T1	I	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Requires 100nF AC Coupling Capacitor in series with each differential signal.

CLOCK SOURCES/ PIN NAMES	PIN #	TYPE	TERMINATION	RECOMMENDATIONS
PEX_REFCLKp Input	T2	I	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Requires 100nF AC Coupling Capacitor in series with each differential signal.

3.1.2 RESET

Table 2. Transparent Port Chip Reset Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
PEX_PERST#	H5	I	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCI Express Reset. Propagates to Downstream ports.

3.1.3 SERIAL EEPROM

Table 3. Transparent Port Serial EEPROM Connections

EPROM TYPE	PIN#	STATUS	SUPPLY	RECOMMENDATIONS
AT25256A	N/A	**NOT PRESENT** ☐ **PRESENT** ☐	**+3.3V** ☐ **Other** ☐	Existing +3.3V supply must be used. Default recommended EEPROM.
PIN NAME	**PIN#**	**TYPE**	**PIN STATUS**	**RECOMMENDATIONS**
EE_CS#	P35	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Serial EEPROM Chip select Output. Weakly pulled up. Can be left floating if not used or stronger pull-ups (5K-10KOhms) used. ***This signal is an output. Verify that signal is being used accordingly on the schematic***.
EE_DI	P34	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Serial EEPROM Data Input. Weakly pulled up. Can be left floating if not used or stronger pull-ups (5K-10KOhms used) ***This signal is an output. Verify that signal is being used accordingly on the schematic***
EE_DO	P33	I	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Serial EEPROM Data Output. Weakly pulled up. Can be left floating if not used or stronger pull-ups (5K-10KOhms used). ***This signal is an input. Verify that signal is being used accordingly on the schematic***.

EPROM TYPE	PIN#	STATUS	SUPPLY	RECOMMENDATIONS
EE_SK	N36	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Serial EEPROM Clock Output Programmable [by way of the Serial EEPROM Clock Frequency Register EepFreq[2:0] field (offset 268h[2:0])] to the following: • 1 MHz • 1.98 MHz • 5 MHz • 9.62 MHz • 12.5 MHz • 15.6 MHz • 17.86 MHz Serial EEPROM Clock output. Weakly pulled up. Can be left floating if not used or stronger pull-ups (5K-10KOhms) used. ***This signal is an input. Verify that signal is being used accordingly on the schematic***.

3.1.4 PORT STRAPPING BALLS

Table 4. Port Strapping Ball Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
STRAP_FACTORY_TEST1#	R3	STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Must be tied High (VDD33). 5K-10Kohm pulled preferred
STRAP_FACTORY_TEST2#	P36	STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Must be tied High (VDD33). 5K-10Kohm pulled preferred
STRAP_FACTORY_TEST3#	H33	STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Must be tied High (VDD33). 5K-10Kohm pulled preferred
STRAP_FACTORY_TEST[5:4]#	H34, J32	STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Must be tied High (VDD33). 5K-10Kohm pulled preferred
STRAP_FACTORY_TEST6#	L5	STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Must be tied High (VDD33). 5K-10Kohm pulled preferred

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
STRAP_STN0_PORTCFG[1:0]	N35, N34	STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Strapping Signals to Select Number of Lanes in Port Configuration for Station 0, Ports[0,1,2] (2 Balls). EEPROM, if present will override settings. However, if no EEPROM present, these signals must be pulled-up/down to VDD33/VSS accordingly to select appropriate mode on the PEX 8548. Register/Bits – Port Configuration (Port 0, offset 224h) **LL, HH = x8,x4,x4** **LH = x16** **HL = x8,x8** Signals must not be strapped to "**Reserved**" settings. ***Verify Strapping of these pins matches the desired operating mode of the switch*.**
STRAP_STN1_PORTCFG[1:0]	J35, J33	STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Strapping Signals to Select Number of Lanes in Port Configuration for Station 1, Ports[8,9,10] (2 Balls). EEPROM, if present will override settings. However, if no EEPROM present, these signals must be pulled-up/down to VDD33/VSS accordingly to select appropriate mode on the PEX 8548. Register/Bits – Port Configuration (Port 8, offset 224h) **LL, HH = x8,x4,x4** **LH = x16** **HL = x8,x8** Signals must not be strapped to "**Reserved**" settings. ***Verify Strapping of these pins matches the desired operating mode of the switch*.**

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
STRAP_STN2_PORTCFG[1:0]	K35, L34	STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Strapping Signals to Select Number of Lanes in Port Configuration for Station 2, Ports[12,13, 14] (2 Balls). EEPROM, if present will override settings. However, if no EEPROM present, these signals must be pulled-up/down to VDD33/VSS accordingly to select appropriate mode on the PEX 8548. Register/Bits – Port Configuration (Port 12, offset 224h) **LL, HH = x8,x4,x4** **LH = x16** **HL = x8,x8** Signals must not be strapped to "**Reserved**" settings. ***Verify Strapping of these pins matches the desired operating mode of the switch.***
STRAP_TESTMODE[3:0]	H32, H35, G34, G33	STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Test Mode Selects (4 Balls) These signals are reserved for Factory Test Signals Must be pulled High. Register – Physical Layer Test HHHH = Default (Test Modes are disabled) (VDD33) 5K-10Kohm pulled preferred

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
STRAP_UPSTRM_PORT_SEL[3:0]	H1, G2, K3, G1	STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Strapping Signal for Upstream. EEPROM will overwrite Strap Setting. However, if no EEPROM present, these signals must be pulled-up/down to VDD33/VSS according to select appropriate mode on the PEX 8548 Appropriate setting are: Register/Bits – Upstream Port ID LLLL = Port 0 LLLH = Port 1 LLHL = Port 2 **LLHH to LHHH = Reserved.** HLLL = Port 8 HLLH = Port 9 HLHL = Port 10 **HLHH = Reserved** HHLL = Port 12 HHLH = Port 13 HHHL = Port 14 **HHHH = Reserved** Signals must not be strapped to "**Reserved**" settings. ***Verify Strapping of these pins matches the desired operating mode of the switch*.**

3.1.5 POWER SUPPLY

Table 5. Power Supply Connections

POWER SEQUENCING	STATUS	RECOMMENDATIONS
VDD10/S, VTT, VDD33/A	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Schematic should include power sequencing circuitry to assure that: (1) VDD10/S power up first and power down last. (2) All power rails should power within 50ms of each other

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
THERMAL_DIODEn	E2	Reserved	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Must be Tied High.
THERMAL_DIODEp	H4	Reserved	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	No Connect. Don't connect this to electrical Path.

VDD10	P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, P23, P24, R13, R24, T13, T24, U13, U24, V13, V24, W13, W24, Y13, Y24, AA13, AA24, AB13, AB24, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AC24	CPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**1.0V Power for Core Logic (40 Balls)** The PEX8548 Reference Design uses a “3 value per decade” decoupling scheme. The discrete decoupling capacitors are meant to cover frequencies from 1Mhz to 200MHz without creating frequency holes. The design also relies on the plane capacitance and special footprint for the decoupling capacitors. Please refer to the Reference Design HRM. 1. Fifteen 0.001uF 2. Ten 0.0022uF 3. Seven 0.0047uF 4. Five 0.001uF 5. Four 0.022uF 6. Three 0.04uF 7. Two 0.1uF 8. One 0.22uF An alternative approach is to use the “one Value per decade” following are the recommended values for the decoupling capacitors. 1. Eight 0.001uF 2. Sixteen 0.01uF 3. Sixteen 0.1uF 4. Six 1uF 5. Six 10uF

VDD10A	E8, E16, E24, E32, U5, W32, AA5, AG32, AJ5, AM7, AM15, AM23, AM31	APWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	ANALOG PWR: 320Mhz Low Pass Filter should be used to improve noise tolerance. 100nF and 10uF Decoupling Caps can be shared with VDD10 supply. However, decoupling caps are required right at the supply pins. Filter should reject VCC noise between 600Khz to 320Mhz. **Verify that VDD10A is at 1.0V +/- 5%**.
VDD10S	B2, B3, B4, B6, B8, B10, B12, B14, B16, B18, B20, B22, B24, B26, B28, B30, B32, B34, B36, C3, C4, C8, C12, C16, C20, C24, C28, C32, C36, E12, E20, E28, E34, R34, R35, U2, U3, U35, W2, W34, W35, AA2, AA3, AA35, AC2, AC34, AC35, AE2, AE3, AE5, AE35, AG2, AG34, AG35, AJ2, AJ3, AJ35, AL2, AL32, AL34, AL35, AM11, AM19, AM27, AM33, AP3, AP7, AP11, AP15, AP19, AP23, AP27, AP31, AP35, AR1, AR3, AR5, AR7, AR9, AR11, AR13, AR15, AR17, AR19, AR21, AR23, AR25, AR27, AR29, AR31, AR33, AR35	SerDesPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	DIGITAL PWR: Decoupling Caps can be shared with VDD10 supply. However, decoupling caps are required right at the supply pins **Verify that VDD10A is at 1.0V +/- 5%.**

VDD33	C1, D2, G5, G32, J5, L32, M5, P32	I/OPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	I/O LOGIC PWR: One per decade scheme. >Ten 0.001uF Ceramic Decoupling Caps placed close to Balls as possible. >Four 0.01uF Decoupling Caps placed as close to Balls as possible >One 0.1uF Decoupling Caps placed as close to Balls as possible **Verify that VDD33 is at 3.3V +/- 10%.**
VDD33A	L4	PLLPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PLL PWR: Additional .1uF capacitors should be placed near to this pin depending on the extent of supply noise. **Verify that VDD33A is at 3.3V +/- 10%.**

VSS	A2, A3, A4, A6, A8, A10, A12, A14, A16, A18, A20, A22, A24, A26, A28, A30, A32, A34, B1, C2, C5, C6, C7, C9, C10, C11, C13, C14, C15, C17, C18, C19, C21, C22, C23, C25, C26, C27, C29, C30, C31, C33, C34, C35, D3, D4, D6, D8, D10, D12, D14, D16, D18, D20, D22, D24, D26, D28, D30, D32, D34, D36, E4, E36, F1, F5, F33, F34, F35, F36, J1, J36, M36, N1, N3, P3, R1, R32, R33, R36, T3, T34, U1, U4, U33, U34, U36, V3, V34, W1, W3, W4, W33, W36, Y3, Y34, AA1, AA4, AA33, AA34, AA36, AB3, AB34, AC1, AC3, AC4, AC33, AC36, AD3, AD34, AE1, AE4, AE33, AE34, AE36, AF3, AF34, AG1, AG3, AG4, AG33, AG36, AH3, AH34, AJ1, AJ4, AJ33, AJ34, AJ36, AK3, AK34, AL1, AL3, AL4, AL33, AL36, AM1, AM3, AM35, AM36, AN1, AN3, AN5, AN7, AN9, AN11, AN13, AN15, AN17, AN19, AN21, AN23, AN25, AN27, AN29, AN31, AN33, AN35, AN36, AP1, AP2, AP4, AP5, AP6, AP8, AP9, AP10, AP12, AP13, AP14, AP16, AP17, AP18, AP20, AP21, AP22, AP24, AP25, AP26, AP28, AP29, AP30, AP32, AP33, AP34, AP36, AR36, AT3, AT5, AT7, AT9, AT11, AT13, AT15, AT17, AT19, AT21, AT23, AT25, AT27, AT29, AT31, AT33, AT35	GND	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Ground and Thermal Ball-Ground Connections.

VSS_Thermal	R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, T14, T15, T16, T17, T18, T19, T20, T21, T22, T23, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, V14, V15, V16, V17, V18, V19, V20, V21, V22, V23, W14, W15, W16, W17, W18, W19, W20, W21, W22, W23, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, Y22, Y23, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA22, AA23, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23	Thermal-GND	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Thermal ground connection are not connect to the Die, but should be grounded to reduce power dissipation.
VSSA_PLL	R2	PLL_GND	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PLL Ground Connection.
VTT_ PEX[7:0]	AM17, AM13, AM9, AM5, AL5, AG5, AC5, W5	Supply	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	SERDES Termination Supply. One per decade scheme. >Ten 0.001uF Ceramic Decoupling Caps placed close to Balls as possible. >Four 0.01uF Decoupling Caps placed as close to Balls as possible >One 0.1uF Decoupling Caps placed as close to Balls as possible **This supply should be implemented separated from other supplies preferably point-to-point to the input.** **Verify that VTT is between 1.0V to 1.8V.**

VTT_ PEX[15:8]	F32, E30, E26, E22, E18, E14, E10, E6	Supply	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	SERDES Termination Supply. Connect to VTT_PEX[7:0]. **Verify that VTT is between 1.0V to 1.8V.**
VTT_ PEX[23:16]	AM21, AM25, AM29, AJ32, AE32, AC32, AA32, U32	Supply	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	SERDES Termination Supply. Connect to VTT_PEX[7:0]. **Verify that VTT is between 1.0V to 1.8V.**

3.1.6 JTAG PINS

Table 6. JTAG Ball Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
JTAG_TCK	E3	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	JTAG Test Clock Input. JTAG Test Access Port (TAP) Controller clock source. JTAG_TCK frequency can be from 0 to 10 MHz. Should be pulled up to VDD33 if unused.
JTAG_TDI	F2	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	JTAG Test Data Input Serial input to the TAP Controller for test instructions and data. Should be pulled up to VDD33 if unused
JTAG_TDO	G4	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	JTAG Test Data Output Serial output to the TAP Controller for test instructions and data
JTAG_TMS	F4	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	JTAG Test Mode Select Input Input decoded by the TAP Controller to control test operations. Should be pulled up to VDD33 with a 3K to 10KOhm resistor if unused
JTAG_TRST#	F3	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	JTAG Test Reset. Active Low input Active-Low input, to place the Test Access Port(TAP) Controller into Test-Logic-Reset state, which enables normal logic operation. Tie to VSS through a 1.5KOhm resistor when Test Access Port is not being used.

3.1.7 I2C PINS

Table 7. JTAG Ball Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
I2C_ADDR[2:0]	K34,K33,K36	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	I2C Slave Address Bits 2 through 0. Used to set the PEX 8548 address on the I2C Bus. Must be pulled up to VDD33 through external resistors.

I2C_INTA_ENABLE#	G36	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Enables I2C and PEX_INTA#. Controls whether the I2C_SCL , I2C_SDA , and PEX_INTA# Open Drain buffers are internally terminated. If either I2 C or PEX_INTA# is used, pull I2C_INTA_ENABLE# Low to disable internal termination of the I2C_SCL, I2C_SDA, and PEX_INTA# Open Drain buffers, and provide external pull-up resistors on all three signals. If neither I2 C nor PEX_INTA# is used, I2C_INTA_ENABLE# can be pulled High or remain unconnected with its internal pull-up resistor, to enable internal termination of the I2C_SCL, I2C_SDA, and PEX_INTA# Open Drain buffers, in which case I2C_SCL, I2C_SDA, and PEX_INTA# can all remain unconnected.
I2C_SCL	J34	I OD	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	I2C Serial Clock Line I2C Clock Source Use a 2.26 K Ohm Pull-up.
I2C_SDA	H36	I/O OD	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	I2C Serial Data Output Transfer and receives I2C data.

3.1.8 FATAL ERROR/ PEX_INTA# SIGNAL

Table 8. Fatal Error and PEX_INTA#

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
PEX_INTA#	N33	OD	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**Interrupt Message** Interrupt output enabled when INTA# messages are enabled (**Command** register Interrupt Disable bit, offset 04h[10]=0) and Message Signaled Interrupts (MSI) are disabled (**MSI Control** register MSI Enable bit, offset 48h[16]=0). **No Pull up Required.**
FATAL_ERR#	N32	I/O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**Fatal Error** **No Pull up Required.**

3.1.9 NO CONNECT BALLS

Table 9. No Connect Balls

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
NC_FACTORY_TEST14	L33	RESERVED	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**No Connect. For Factory Test Only** **Do not connect this pin to any electrical path on the board.**
NC_PROCMON	P1	RESERVED	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**No Connect.** **Do not connect this pin to any electrical path on the board.**
NC_SPARE[2,0]	G35, M34	RESERVED	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**No Connect. (2 Balls)** **Do not connect this pin to any electrical path on the board.**

3.1.10 HOT PLUG CONTROLLER INTERFACE

Table 10. Hot Plug Port Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
HP_ATNLED[9:8,1]#	N2, L2, H3	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Hot Plug Attention LED for Ports 9,8 and 1 (3 Balls). Active Low Output. Don't Care if Hot-Plug is unused
HP_BUTTON[9:8,1]#	T4, P5, D1	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Hot Plug Attention Button for Ports 9,8 and 1 (3 Balls). If Hot-Plug is unused leave unconnected or pulled up to VDD33. Otherwise, driven active low Recommended Resistance 3K to 10K Ohms.
HP_CLKEN[9:8,1]#	L1, G3, M3	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Reference clock enable outputs for Ports 9,8 and 1 (3 Balls). Don't care if Hot-Plug is unused
HP_MRL[9:8,1]#	P2, N4, H2	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Hot-Plug Manually-operated retention latch If Hot-Plug is unused, leave unconnected or pull up to VDD33 Otherwise, driven active low
HP_PERST[9:8,1]#	R4, J3, K5	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Active low reset output for Downstream Ports 9,8 and 1 (3 Balls). Don't Care if Hot Plug is unused Recommended Resistance 3K to 10K Ohms.

HP_PRSNT[9:8,1]#	M2, J2, K1	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Combination of Hot Plug PRSNT1# and PRSNT2# Input for Ports 9,8 and 1 (3 Balls). If Hot-Plug is unused, leave unconnected or pull up to VDD33. Otherwise, driven active low Recommended Resistance 3K to 10K Ohms.
HP_PWREN[9:8,1]#	M1, M4, K2	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Active Low Hot Plug Power Enable Output for Station 0 Ports. Don't Care if Hot Plug is unused
HP_PWRFLT[9:8,1]#	R5, L3, J4	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Hot Plug Power Fault Input for Ports 9,8 and 1 (3 Balls). If Hot-Plug is unused, leave unconnected or pull up to VDD33. Otherwise, driven active low Recommended Resistance 3K to 10K Ohms.
HP_PWRLED[9:8,1]#	K4, E1, P4	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Hot Plug Power LED Output for Ports 9,8 and 1 (3 Balls). Don't Care if Hot-Plug is unused.

3.1.11 PCI EXPRESS BUS INTERFACE

Table 11. PCI Express Interface Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
PEX_PORT_GOOD[14:12,10:8,2:0]#	L33, L35, L36, M32, K32, T5, M33, M35, N5	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	These outputs can directly drive common-anode LED modules. External current-limiting resistors are required. **Highly recommended that customer implement these signal on schematic and PCB to verify Link Training status.**
PEX_PERn[15:0]	AM18, M16, AM14, AM12, AM10, AM8, AM6, AM4, AM2, AK5, AH5, AF5, AD5, AB5, Y5, V5	CMLRn	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Receive Signals for Station 0

PEX_PERn[31:16]	E35, E33, E31, E29, E27, E25, E23, E21, E19, E17, E15, E13, E11, E9, E7, E5	CMLRn	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Receive Signals for Station 1
PEX_PERn[47:32]	AM20, AM22, AM24, AM26, AM28, AM30, AM32, AM34, AK32, AH32, AF32, AD32, AB32, Y32, V32, T32	CMLRn	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Receive Signals for Station 2
PEX_PERp[15:0]	AN18, AN16, AN14, AN12, AN10, AN8, AN6, AN4, AN2, AK4, AH4, AF4, AD4, AB4, Y4, V4	CMLRp	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe positive polarity differential Lane Receive Signals for Station 0
PEX_PERp[31:16]	D35, D33, D31, D29, D27, D25, D23, D21, D19, D17, D15, D13, D11, D9, D7, D5	CMLRp	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe positive polarity differential Lane Receive Signals for Station 1
PEX_PERp[47:32]	AN20, AN22, AN24, AN26, AN28, AN30, AN32, AN34, AK33, AH33, AF33, AD33, AB33, Y33, V33, T33	CMLRp	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe positive polarity differential Lane Receive Signals for Station 2

PEX_PETn[15:0]	AT18, AT16, AT14, AT12, AT10, AT8, AT6, AT4, AT2, AK1, AH1, AF1, AD1, AB1, Y1, V1	CMLTn	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Transmit Signals for Station 0 ***Series 100nF AC coupling capacitor required on each transmit pair***.
PEX_PETn[31:16]	A35, A33, A31, A29, A27, A25, A23, A21, A19, A17, A15, A13, A11, A9, A7, A5	CMLTn	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Transmit Signals for Station 0 ***Series 100nF AC coupling capacitor required on each transmit pair***.
PEX_PETn[47:32]	AT20, AT22, AT24, AT26, AT28, AT30, AT32, AT34, AK36, AH36, AF36, AD36, AB36, Y36, V36, T36	CMLTn	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Transmit Signals for Station 0 ***Series 100nF AC coupling capacitor required on each transmit pair***.
PEX_PETp[15:0]	AR18, AR16, AR14, AR12, AR10, AR8, AR6, AR4, AR2, AK2, AH2, AF2, AD2, AB2, Y2, V2	CMLTp	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Transmit Signals for Station 0 ***Series 100nF AC coupling capacitor required on each transmit pair***
PEX_PETp[31:16]	B35, B33, B31, B29, B27, B25, B23, B21, B19, B17, B15, B13, B11, B9, B7, B5	CMLTp	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Transmit Signals for Station 0 ***Series 100nF AC coupling capacitor required on each transmit pair***
PEX_PETp[47:32]	AR20, AR22, AR24, AR26, AR28, AR30, AR32, AR34, AK35, AH35, AF35, AD35, AB35, Y35, V35, T35	CMLTp	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Transmit Signals for Station 0 ***Series 100nF AC coupling capacitor required on each transmit pair***

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3.2 Additional Schematic Guidelines

3.2.1 Power Sequencing

The PEX 8548 requires its power supplies to be sequenced in a specific order. In particular, VDD10, VDD10A and VDD10S should be powered up first and powered down last followed by the 3.3V I/O supply, and VTT (SerDes Transmitter power). Please make sure to implement power sequencing circuitry on your board to meet the sequencing requirements of the device. Additional information about power sequencing can be found in the PEX 8548 Quick Start Design Guide. Additionally, you can refer to the PEX 8548 RDK Hardware Reference Manual for a suggested reference circuit that control power sequencing.

3.2.2 Reset

The PEX 8548 requires the PERST# signal to be asserted for at least 100ms after the board's power is stable to allow the chip to initialize correctly. Please make sure to implement Power On Reset and Power Valid detection circuitry on your board to meet these requirement. Please refer to the PEX 8548 RDK Hardware Reference Manual for suggested reference circuits.

3.2.3 Mid-Bus Probe Pads

If your design contains an embedded PCIe link, for example, PCIe connection(s) between the PEX 8548's port(s) and endpoint(s) embedded on the same board. It is very useful to add probe pads to your PCB design for each embedded PCIe link connected to the PEX 8548. Probe pads can be very helpful when you need to debug a problem on a PCIe link with a PCIe analyzer. PCIe Analyzer Manufacturer's provide circuitry, called Mid-Bus Probes, to help you debug embedded links. If you do plan to implement Mid-Bus Probe footprints in your PCB design, be aware that it may induce jitter and/o reduce signal integrity on the PCIe lanes it is connected to.

Each Manufacturer will usually provide a probe footprint to be implemented on the board for debugging purposes. For more information regarding this, please contact PLX Technical Applications.

3.2.4 Port Good Logic

The PEX 8548 contains 1 PEX_PORT_GOOD output for each port on the device. There outputs are active low so they can drive LEDs on your board. These signal are a very useful visual indication to determine whether a specific SerDes lane is up and active (In the L0, normal operating) mode on any port on the PEX 8548. This is helpful to determine whether link up problems are occurring on the board. It is highly recommended that your use these outputs to drive LEDs on your board for all ports that are connected to the PEX 8548.

3.2.5 Spread Spectrum Clocking (SSC)

The PEX 8548 supports a Spread Spectrum REFCLK source. The SSC clock *must* originate from the PCIe connector on a slot in the motherboard or through a common clock source that is being distributed to all add-in cards and/or PCIe devices in the system.

If your REFCLK source is non-SSC, then you may have separate REFCLK sources on different cards or devices as long as their frequency difference is within +/- 300ppm. (~30ps for a 100Mhz Clock source) Please refer to the PEX 8548 Quick Start Design Guide for more information.

4 PEX 8548 Power Consumption Notes

The power consumption of the PEX 8548 is divided in to four sources. There are separate power consumption values for the Core (VDD10/A) SerDes Digital Supply (VDD10S), SerDes Analog Supply (VTT) and 3.3V IO (VDD33A) The total power consumption of the device is the sum of the power draw from all of these four sources. The amount of power the device actually consumes depends on the amount of traffic passed through it. More power consumption will occur when heavier PCIe traffic is flowing through the switch. Please refer to "Electrical Specifications" section of PEX 8548 Databook for more details.

Based on these power consumption numbers you can calculate the maximum current draw for each of the power sources above and generate an estimated AC current draw for the entire device. Divide the Power consumption data based on your traffic type by the supply voltage for each source to obtain the worst case current draw for that source. Sum up each current value to get an estimate of the total current draw for the device.

5 General PCB Routing Guidelines

Since PCIe links operate are very high speeds, proper PCB routing of each RX and TX pair in each lane is critical for maintaining signal integrity on each PCIe link. The PCI-SIG provides numerous suggestions about how to correctly design PCB's containing PCIe links. Several important guidelines are listed below. Additional information is available from the PCI-SIG website.

1. Recommended Microstrip Trace Routing Guidelines:
   - Differential Impedance 4, 6 layer: 100 Ohms +/- 20% 8, 10 layer: 85 Ohms +/- 20%
   - Single ended Impedance 4, 6 layer: 60 Ohms +/- 15% 8, 10 layer: 55 Ohms +/- 15%
2. Recommended Stripline Trace Routing Guidelines:
   - Differential Impedance 6 layer: 100 Ohms +/- 15% 8, 10 layer: 85 Ohms +/- 15%
   - Single ended Impedance 6 layer: 60 Ohms +/- 15% 8, 10 layer: 55 Ohms +/- 15%
3. Recommended for all differential signal pairs: maintain >= 20 mil trace edge to plane edge gap
4. Recommended Length matching Intra-pair: max 5 mil delta, matching maintained segment to segment, match at point of discontinuity, but avoid "tight bends"
5. Gnd referenced signals is recommended. Use stitching caps with PWR referenced signal traces.
6. Use Gnd stitching vias by signal layer vias for layer changes
7. Do not route over plane splits or voids. Allow no more than 1/2 trace width routed over via antipad
8. Match left/right turn bends where possible. No 90-degree bends or "tight" bend structures.
9. The reference clock signal pair should maintain the same reference plane for the entire routed length and should not cross any plane splits (breaks in the reference plane)
10. Reference clock terminating components should be placed as close as possible to their respective device, ideally within 100 mils of the clock/receiver component pin
11. Match all segment lengths between differential pairs along the entire length of the pair.
12. Maintain constant line impedance along the routing path by keeping the same line width and line separation.
13. Avoid routing differential pairs adjacent to noisy signal lines or high speed switching devices such as clock chips.
14. Recommended reference clock differential pair spacing (clock to clock#) < = 11.25 mils.
15. Recommended reference clock trace spacing to other traces is >= 20 mils.
16. Recommended reference clock line width >= 5 mils.
17. When routing the 100Mhz differential clock, do not divide the two halves of the clock pair between layers.
18. Recommended reference clock trace impedance:
    - Single ended: 50-60 Ohms +/- 15%
    - Differential: 100 Ohms +/- 20%
19. Recommended PCI Express reference clock to PCI express reference clock length matching to within 25 mils
20. AC Coupling Capacitors: The same package size and value of capacitor should be used for each signal in a differential pair.
21. AC Coupling Capacitors: Locate capacitors for coupled traces in a differential pair at the same location along the differential traces. Place them as close to each other as possible.
22. AC Coupling Capacitors: The "breakout" into and out of the capacitor mounting pads should be symmetrical for both signal lines in a differential pair.
23. Test points and probing structures should not introduce stubs on the differential pairs.
24. Use Tantalum or Low ESR Lane AC Coupling Caps.

6 Reference Documents

- PEX 8548 Databook. URL:
- PEX 8548 Quick Start Design Guide. URL:
- PEX 8548 Errata[1] URL:
- [1]An NDA is required to access this document. Please check the website for details
- PEX 8548 EEPROM Application Note – TBD
- PCI Express Add-in Card Compliance Checklist, Revision 1.0. PCI-SIG. http://www.pcisig.com/developers/compliance_program/compliance_checklist (Membership to PCI-SIG is required to access this document.)
- PEX 8548 Hardware Reference Manual URL: