PEX 8548-AA RDK
Hardware Reference Manual

Version 1.2

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Preface

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About This Manual

This Hardware Reference Manual describes the PLX PEX 8548 Rapid Development Kit (RDK) Board (PEX 8548RDK), from a hardware perspective. It contains a description of all major functional circuit blocks on the PEX 8548RDK, and serves as a reference for creating software for this product. This manual also includes a complete Bill of Materials and Schematics.

Revision History

Date	Version	Comments
November 13, 2006	1.0	Initial release. Supports Board Revision 100.
May 8, 2007	1.1	Added item c to "Frequently Asked Questions" section. Changed RDK references/part number to "PEX 8548-AA RDK". Updated Data Book revision listed in Section 8. Applied miscellaneous enhancements throughout the manual.
July 3, 2007	1.2	Corrected CEM Specification revision reference on page 3. Removed "AA" from most part number references. Applied miscellaneous enhancements throughout the manual. Updated Data Book revision listed in Section 8. Added *I²C Specification* information.

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1 General Information

The PLX PEX 8548RDK is a Rapid Development Kit based on PLX Technology's ExpressLane™ PEX 8548, a 9-port, 48-lane, 3-station PCI Express switch. The PEX 8548RDK provides a complete hardware and software development platform to facilitate getting designs up and running quickly, lowering risk and reducing time-to-market. The PEX 8548RDK routes Station 0 to a x16 male board edge connector (P1), allowing the PEX 8548RDK to be directly plugged into a motherboard's x16 PCI Express connector, or plugged into x8, x4, or x1 PCI Express connectors by using board edge adapters. This connector is the path by which power, REFCLK, and PERST# are brought onto the PEX 8548RDK. Station 1 and Station 2 are routed to female x16 PCI Express slot connectors J1 and J2, respectively. Figure 1 provides a component-side view of the PEX 8548RDK.

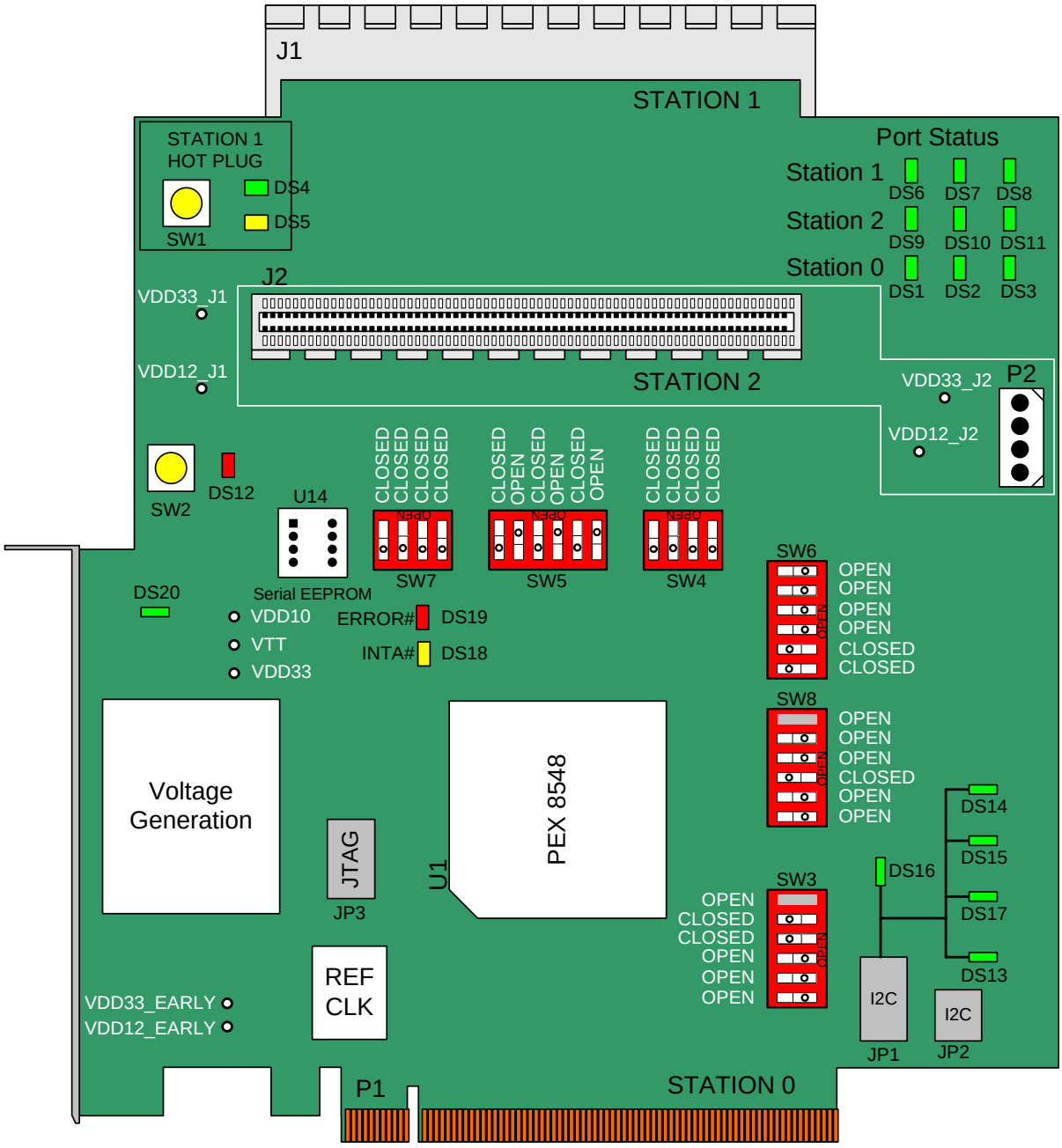


Figure 1. PEX 8548RDK – Component Side View

1.1 PEX 8548 Switch Features

- 9-port (maximum), 48-lane, 3-station PCI Express switch
- Standard 736-ball PBGA-H3 package (37.5 x 37.5 mm)
- 240 Gbps maximum bandwidth [2.5 Gbps/lane x 48 lanes x 2 (full duplex)]
- Non-blocking internal crossbar architecture supports TLP bandwidth capacity of each x16 link
- 1,024-byte Maximum Packet Size
- Performance tuning
- Assign x1, x2, or x4, x8, or x16 lanes per port; combination of x8 ports provides x16
- Allows any port to be designated as the upstream port (Port 0 is recommended)
- Configuration with Strapping balls, serial EEPROM, or I^2C
- Lane and Polarity reversal
- Quality of Service (QoS) with one Virtual Channel (VC) and eight Traffic Classes (TC)
- Round-Robin and Weighted Round-Robin Port Arbitration
- INTA# (PEX_INTA#) and FATAL ERROR (FATAL_ERR#) (Conventional PCI SERR# equivalent) ball support
- Compliant to the following specifications:
  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI Bus Power Management Interface Specification, Revision 1.2*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2*
  - *PCI Express Base Specification, Revision 1.1*
  - *PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a*
  - *The I2C-Bus Specification, Version 2.1*

1.2 PEX 8548RDK Features

- PLX PEX 8548 PCI Express switch in a 736-ball PBGA-H3 package
- Form factor based on the *PCI Express Card Electromechanical (CEM) Specification, Revisions 1.0a and 1.1*
- Two downstream PCI Express slot connectors, each configured as x16
  - Breakout Boards available for further fan-out (x8x8 and x8x4x4 boards available)
- DIP switches for hardware configuration of PEX 8548 switch
- On-board PCI Express REFCLK Fan-Out buffer
- One Hot Plug-controllable slot
- Socketable Serial EEPROM (+3.3V devices supported)
- I^2C interface to read and write registers
- On-board Power Sequencer
- Manual pushbutton PERST# capability
- Port Status indicator LEDs for visual inspection of link status
- Auxiliary hard disk drive header, for supporting additional power requirements for add-in boards

2 System Architecture

The PEX 8548RDK is a PLX Rapid Development Kit intended primarily for use in silicon evaluation and design reference. The form factor is based on the *PCI Express Card Electromechanical (CEM) Specification, Revisions 1.0a and 1.1*. The PEX 8548RDK is designed to work by plugging into a PCI Express-compliant motherboard. Figure 2 illustrates the PEX 8548RDK functional block diagram.

The 16 lanes of Station 0 (which consists of Ports 0, 1, and 2) are routed to a male x16 PCI Express board edge connector (P1). This connector delivers +3.3 VDC and +12 VDC, the Reference Clock, and PERST# to the PEX 8548RDK.

The 16 lanes of Station 1 (which consists of Ports 8, 9, and 10) are routed to a female x16 PCI Express straddle-mount slot connector (J1). The PEX 8548RDK provides +3.3 VDC and +12 VDC, the Reference Clock, and PERST# to this connector. On-board circuitry allows Port 8 to operate as a Hot Plug port; however, this means that Port 8 cannot be configured as the upstream port.

The 16 lanes of Station 2 (which consists of Ports 12, 13, and 14) are routed to a female x16 PCI Express through-hole slot connector (J2). The PEX 8548RDK provides the Reference Clock and PERST#, and a hard disk drive header (P2) provides +3.3 VDC and +12 VDC, to this connector.

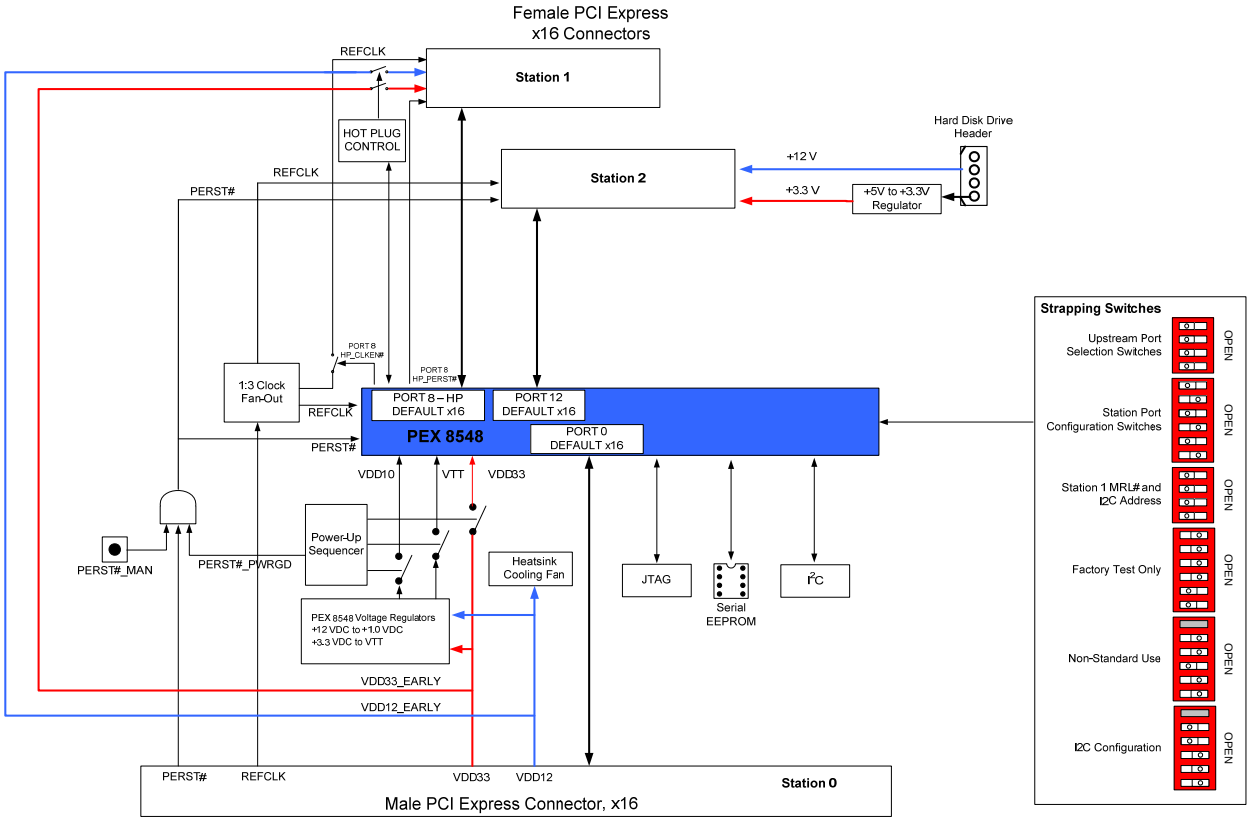


Figure 2. PEX 8548RDK Functional Block Diagram

3 Hardware Architecture

There are several subsystems on the PEX 8548RDK. Among them are a power system that powers the PEX 8548 switch, circuitry for supporting Hot Plug on Station 1 (Port 8), a Reference Clock Fan-Out buffer circuit, and LED indicators and controls. The following sections describe each PEX 8548RDK subsystem.

3.1 PEX 8548 PCI Express Switch

The PEX 8548 is a 9-port, 48-lane, 3-station (up to three ports per station, maximum of nine PCI Express ports), non-blocking PCI Express switch. The switch operates in Transparent mode. Each lane consists of Transmit and Receive signal pairs, which transfer data at a rate of 2.5 Gbps in both directions. The maximum achievable bandwidth is 240 Gbps [2.5 Gbps * 48 lanes * 2 (full duplex)]. The port configuration is flexible and can be changed using a serial EEPROM, the I^2C interface, or Strapping balls. The PEX 8548RDK is designed to allow Station 0 to be routed to a x16 male PCI Express board edge connector, and each of the other two stations (Stations 1 and 2) to be routed to a x16 female PCI Express slot connector. Breakout add-in boards can be plugged into the Station 1 and/or Station 2 connectors, to break these stations out to x8x8 or x8x4x4 port configurations.

3.2 PCI Express Upstream Port PCI Express Connection

The upstream port (within Station 0) is a x16 link that connects the PEX 8548 switch to the male x16 PCI Express board edge connector (P1). The PEX 8548RDK can plug into narrower PCI Express slots (x8, x4, or x1) by using a small adapter board, *such as* those offered by Catalyst. In these situations, the PEX 8548 switch negotiates down to the narrower link width.

3.3 PCI Express Downstream Port Connections

The PEX 8548RDK, in conjunction with breakout add-in boards, provides connectivity to support up to six downstream ports – three from Station 1 and three from Station 2. For each station, PCB traces provide a x16 link to one PCI Express slot connector, for a hardwired default configuration of x16 for Station 1 and x16 for Station 2. (Refer to Figure 3.) If the link width connected between the PEX 8548 switch and an add-in board's PCI Express device is not x16, the link auto-negotiates to a common link width.

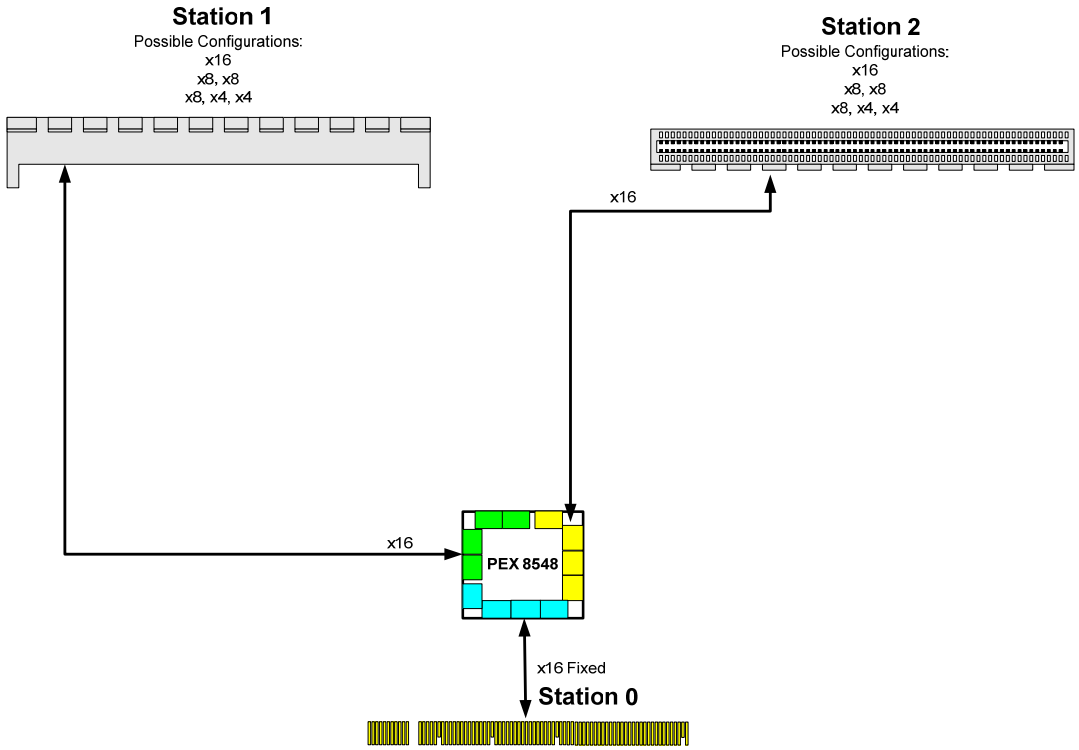


Figure 3. PCI Express Board Interconnect

Hardwire connections that support x8x4x4 and x8x8 downstream configurations can be provided by breakout add-in boards, as illustrated in Figure 4.

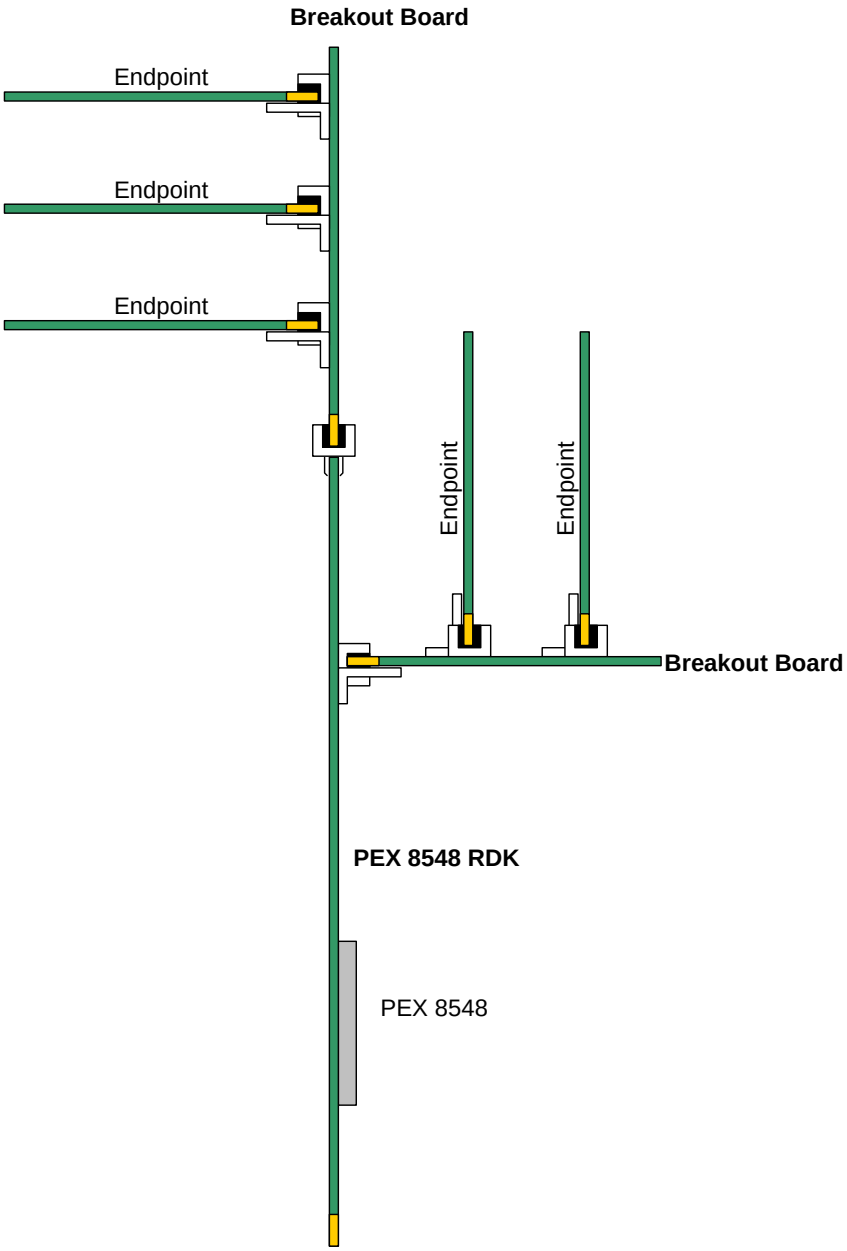


Figure 4. x8x4x4 and x8x8 Downstream Configurations

3.3.1 Downstream Port Breakout Add-In Boards

Breakout add-in boards allow breaking out of the x16 station link into smaller port configurations. There are two breakout board configurations – x16 to x8x8 and x16 to x8x4x4. An on-board Clock Fan-Out buffer circuit provides REFCLK to the slot connectors, from the REFCLK signal provided through the male PCI Express board's edge connector. (Refer to Figure 5.)

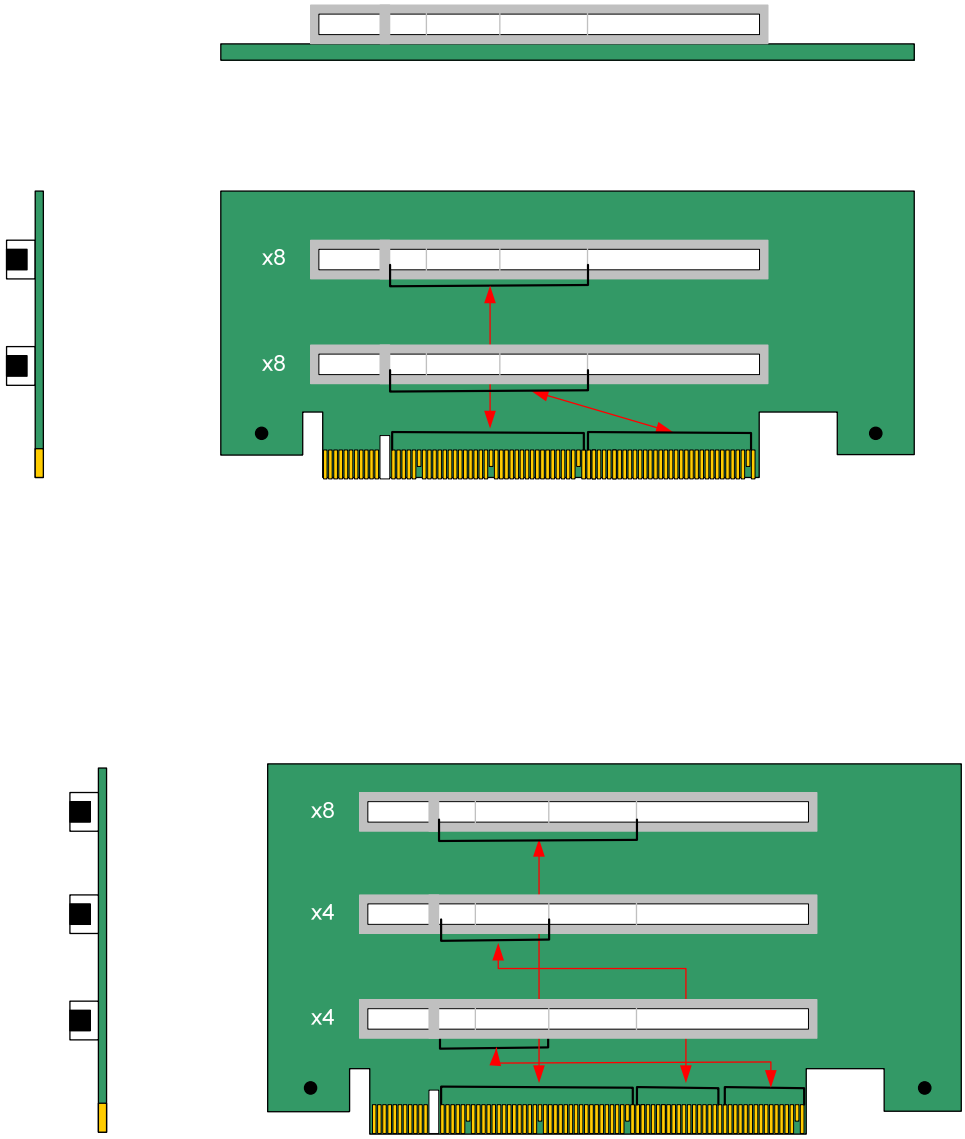


Figure 5. Breakout Add-In Boards

3.4 PCI Express Hot Plug Circuitry

Three of the PEX 8548 switch's ports (Ports 1, 8, and 9) have a PCI Express Hot Plug Controller. The PEX 8548RDK uses only Port 8's Hot Plug Controller, in conjunction with an Intersil ISL6161 Hot Plug Controller, to provide Hot Plug capability to the Station 1 PCI Express slot. The Port 1 and Port 9 Hot Plug Controllers are ***not used***.

Note: *Because Port 8 is hardware-configured to support Hot Plug, Port 8 cannot be used as the upstream port.*

3.5 Reference Clock Circuitry

The PEX 8548RDK uses the 100-MHz differential Reference Clock (REFCLK), provided at the male add-in board's edge connector. This clock drives a 1:3 Clock Fan-Out buffer circuit, to drive the two downstream connectors, as well as the PEX 8548 switch. REFCLK to the Station 1 Hot Plug connector is enabled by the PEX 8548 switch's Port 8 Hot Plug Controller. (The Reference Clock data path is included in Figure 2.)

3.6 PERST# Circuitry

The PEX 8548RDK generates PERST# to the PEX 8548 switch and Station 2 port connector, by wire-ORing PERST# from the male board edge connector with a reset controller chip (U11) driven by +3.3 VDC to the PEX 8548 switch and a manual Reset driven by the MAN_PERST# pushbutton (SW2). (Refer to Figure 6.) PERST# to the Station 1 Hot Plug connector is driven by the PEX 8548 switch's Port 8 Hot Plug Controller.

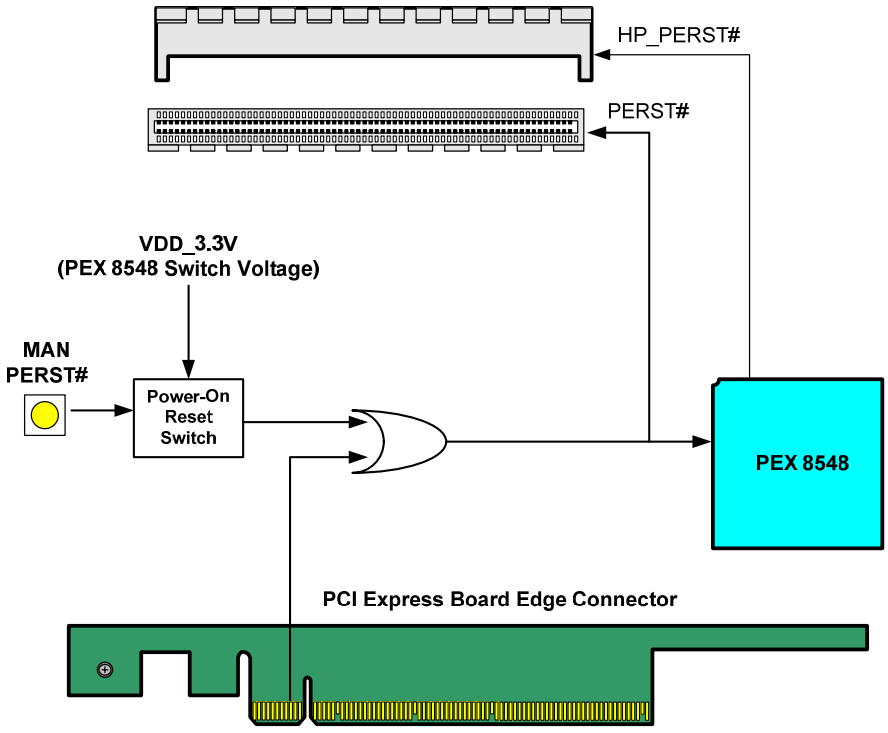


Figure 6. PCI Express Reset Circuitry

3.7 Port Status Indicator LEDs

The PEX 8548 switch incorporates a nine-signal interface dedicated to providing port status for each of the nine possible ports. Two port status states are indicated:

- **Port is up and operating** – PEX_PORT_GOOD# Status signal is asserted, PORT_GOOD status LED is turned On
- **Port is not used** – PEX_PORT_GOOD# Status signal is de-asserted, PORT_GOOD status LED is turned Off

The PEX 8548RDK uses these signals to drive nine discrete green PORT_GOOD status LEDs (located on the upper-right corner of the PEX 8548RDK; refer to Figure 1 and Figure 7). When an LED is driven, that port is active. (Refer to Section 4.1.2, "LED Indicators," for further details.)

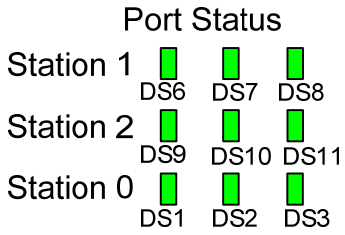


Figure 7. PEX 8548RDK Port Status (PORT_GOOD) Indicators

3.8 Strapping Switches – SW7, SW5, SW4, SW6, SW8, and SW3

The PEX 8548 switch has several Strapping balls that provide the capability to perform various types of hardware initialization, without the use of software. Most Strapping balls are brought out to DIP switches (SW7, SW5, SW4, SW6, SW8, and SW3). Other Strapping balls that are not used in typical situations are strapped, using pull-up or pull-down resistors. Figure 8 illustrates the default switch settings. (Refer to Section 4.1.3, "Controls," for further details.)

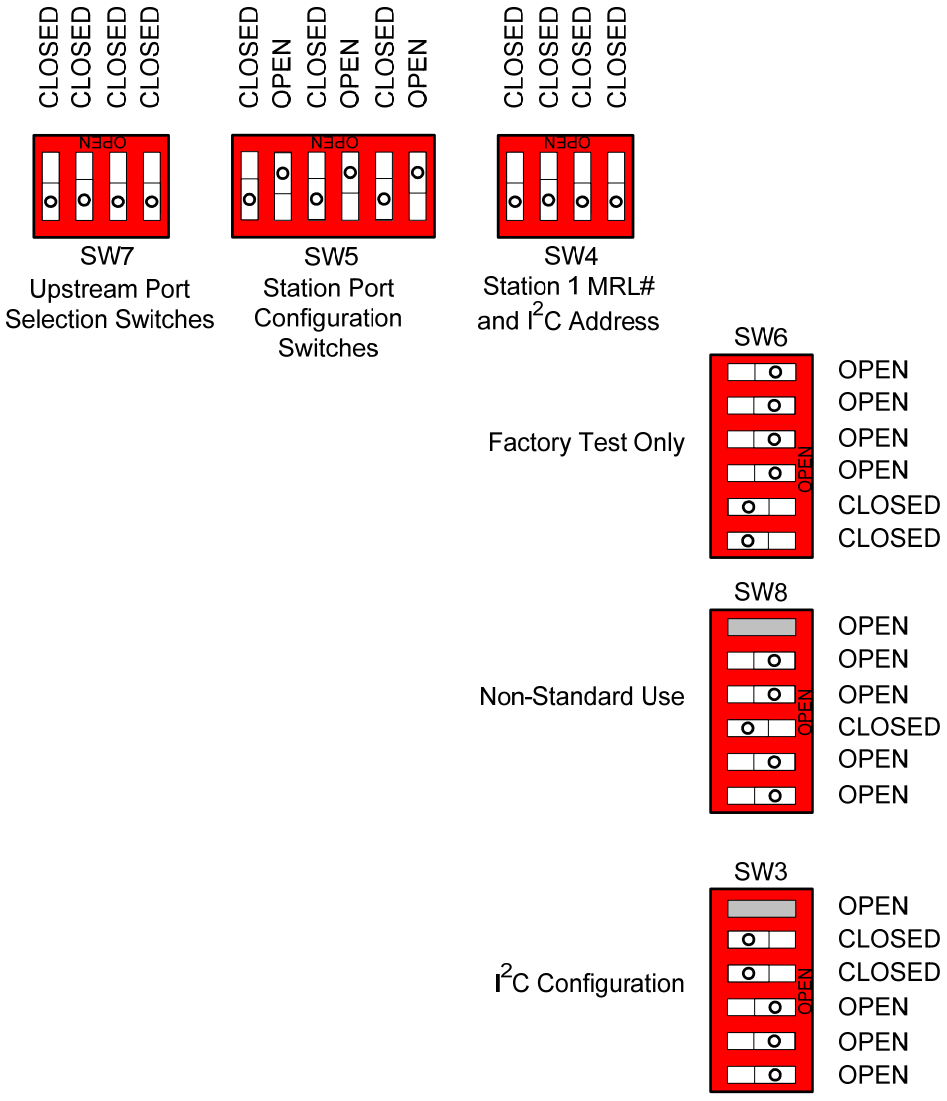


Figure 8. Strapping Switches – SW7, SW5, SW4, SW6, SW8, and SW3

Note: *The grayed-out switch location in SW8 and SW3 is* ***not used****.*

3.9 Power Circuitry

The PEX 8548RDK is used as an add-in board. All power to the on-board components is provided directly from the male board edge connector +12 VDC and +3.3 VDC power pins. The +12 VDC power is converted to +1.0 VDC, for use by the PEX 8548 switch. Most on-board devices, *such as* Clock buffers, serial EEPROM, Port 8 Hot Plug circuitry, and numerous I/O buffers on the PEX 8548 switch, use the +3.3 VDC power rail. All power rails reference a common ground. Figure 9 illustrates the PEX 8548RDK power distribution circuitry.

Voltages to the PEX 8548 switch are sequenced such that VDD_1.0V powers up before VDD_3.3V and VDD_VTT, and powers down after VDD_3.3V and VDD_VTT. (Refer to Figure 10.)

Power field-effect transistors (FETs) are used to gate board power to the Station 1 Hot Plug connector. The Station 2 slot connector receives +12 VDC and +3.3 VDC from a straight, hard disk drive header that can support up to 10A per pin.

Power decoupling uses a three-per-decade decoupling scheme, starting at 12.5 MHz, to avoid resonance peaks in the power distribution system.

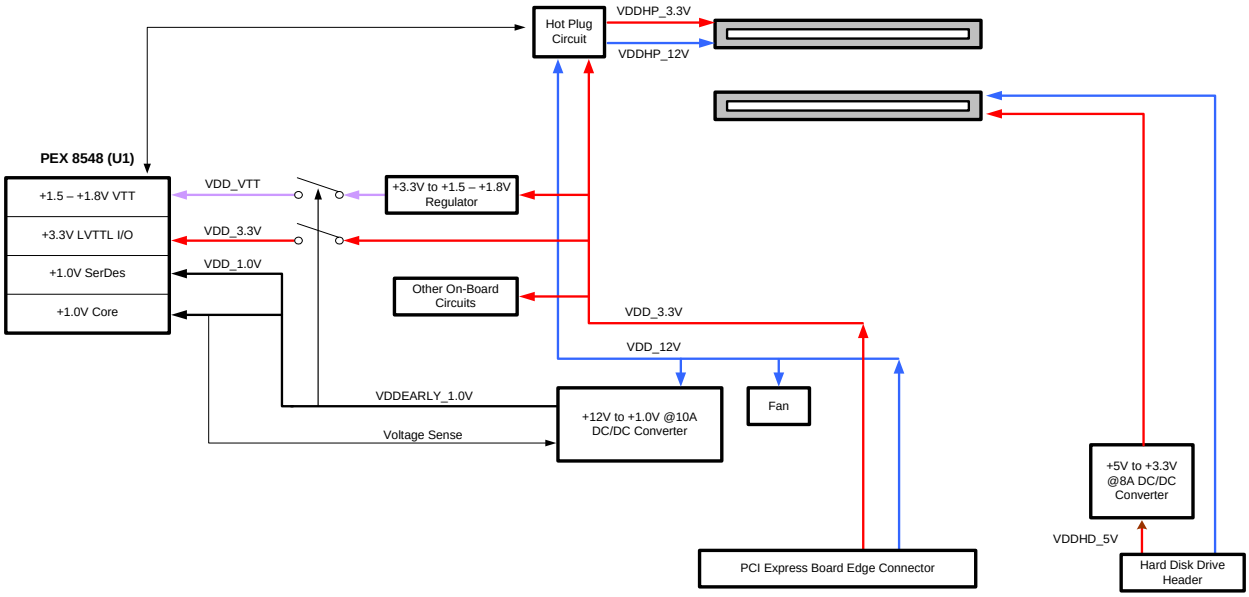


Figure 9. PEX 8548RDK Power Distribution Circuitry

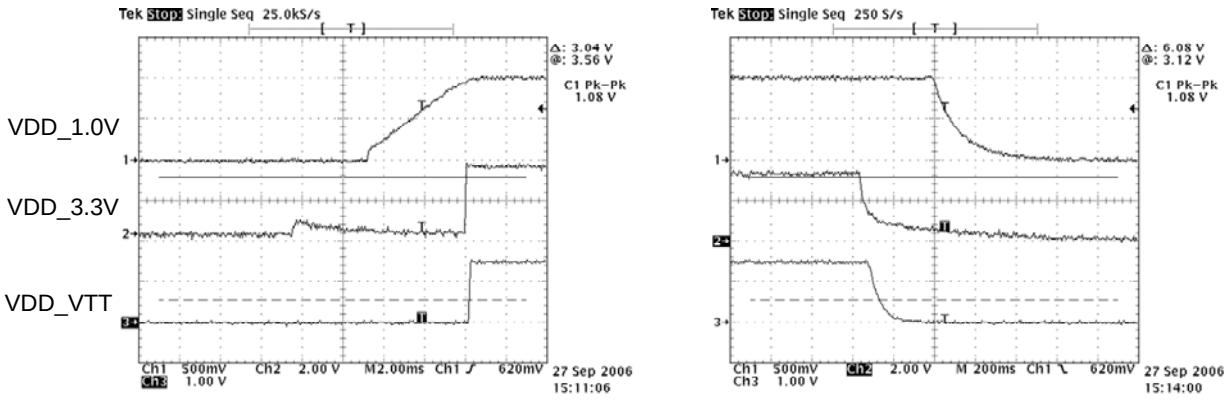


Figure 10. Power-Up and Power-Down Sequencing

3.10 Serial EEPROM Interface

The PEX 8548RDK provides a socketable serial EEPROM (Atmel AT25128A-10PI-2.7) (U14). The serial EEPROM contents are used to initialize the PEX 8548 switch after power-on reset.

3.11 JTAG Interface

The PEX 8548RDK includes a dedicated 2x5 JTAG header (JP3) to the PEX 8548 switch. (Refer to Figure 11.) Additionally, the PEX 8548 switch's JTAG interface can be connected to the PCI Express board edge connector JTAG pins, through 0-Ohm resistors.

There is no "standard" JTAG header pin arrangement; therefore, JTAG header type and pin assignments are arbitrary. The header and pin assignment chosen for the PEX 8548RDK is compatible with the Corelis JTAG single TAP cable (AS00790050-A0).

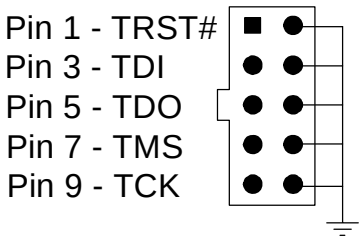


Figure 11. JTAG Header (Top View)

3.12 I²C Interface

The PEX 8548 switch provides a two-wire, I²C-compatible Slave mode interface with 3-bit addressing. Through this out-of-band channel, users can read, write, and configure the PEX 8548 switch's internal registers, and monitor Error Counters and port status. The PEX 8548RDK provides two headers that enable chaining together of multiple boards – a 2x5-pin header (JP1) and a 2x2-pin header (JP2).

There is no "standard" I²C header pin arrangement; therefore, I²C header type and pin assignments are arbitrary. The header and pin assignment chosen for the 2x5 pin header is compatible with the Aardvark I²C/SPI cable. (Refer to Figure 12.) I²C address selection is determined by the SW4 switch settings.

The I²C headers (JP1 and JP2) can be connected to five different objects:

- PEX 8548 switch's I²C interface
- SMBus interface on the three PCI Express connectors (P1, J1, and J2)
- Pull-up resistor network

The connection to the I²C headers is through analog switches that are controlled by DIP switch SW3. Five LEDs (DS13 through DS17) indicate (turn On) when an associated object is connected to the I²C headers. (Refer to Figure 13.)

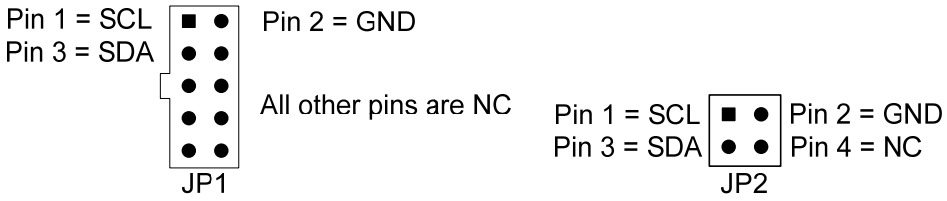


Figure 12. I²C Header (Top View)

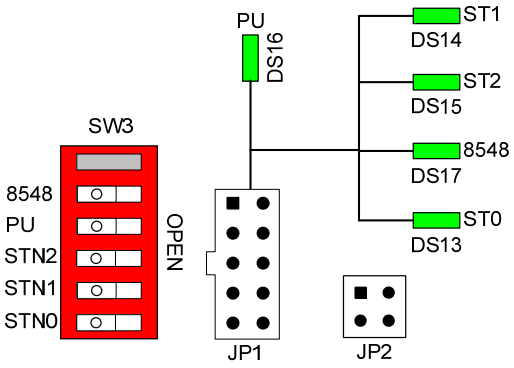


Figure 13. I²C Configuration Control

4 Mechanical Architecture

Figure 14 illustrates the PEX 8548RDK board and component placement.

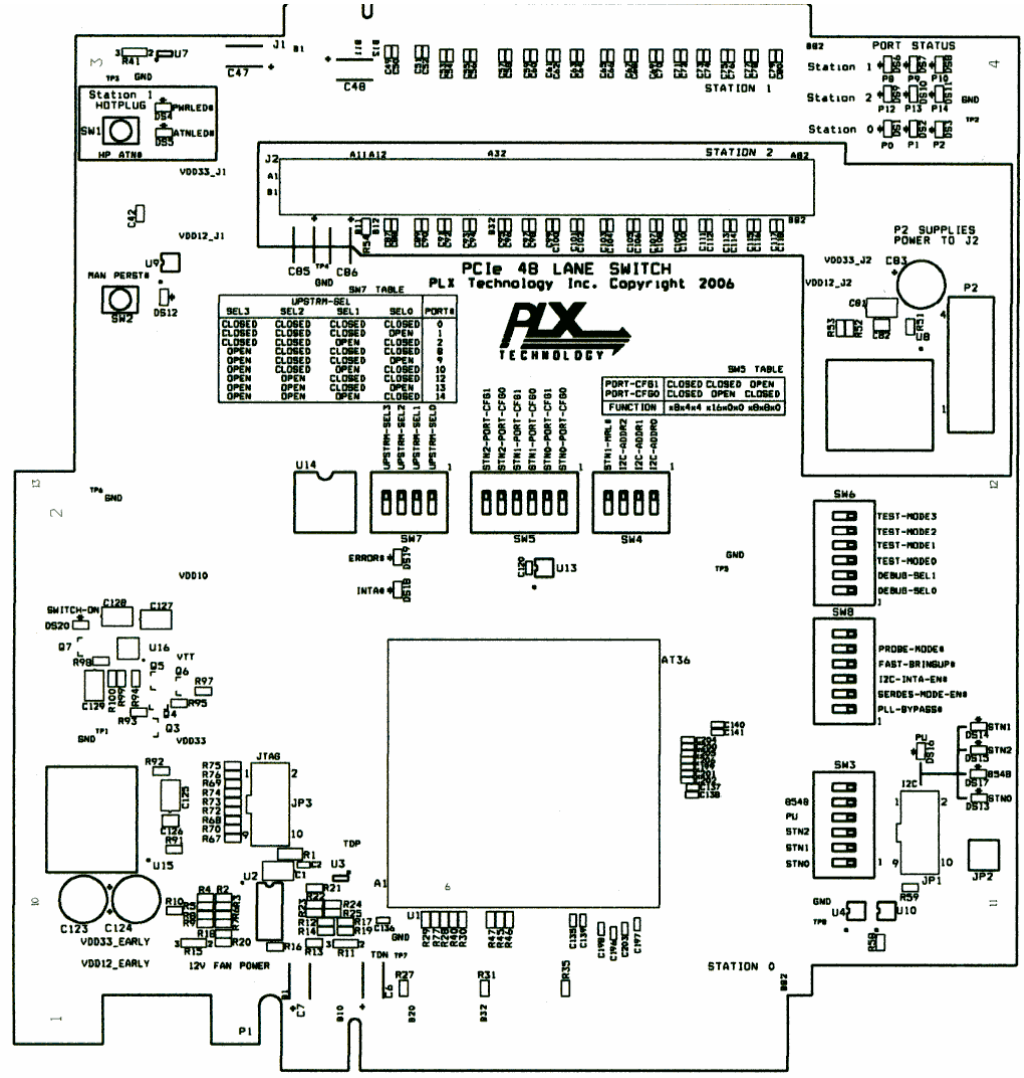


Figure 14. PEX 8548RDK Mechanical Outline

4.1 Monitoring Point, LED Indicator, and Control Summary

This section summarizes the PEX 8548RDK interfaces that are used for monitoring, indicating, and controlling PEX 8548 switch performance.

4.1.1 Monitoring Points

Table 1 lists the functions of all monitoring points available for use on the PEX 8548RDK.

Table 1. PEX 8548RDK Monitoring Points

Silkscreen Label	Function
ERROR#	Test point via at this location can be used to monitor FATAL_ERR# from the PEX 8548 switch.
GND	Eight ground posts, scattered around the PEX 8548RDK, that provide probe reference points.
INTA#	Test point via at this location can be used to monitor PEX_INTA# from the PEX 8548 switch.
VDD10	Test point via at this location can be used to monitor +1.0 VDC to the PEX 8548 switch.
VDD12_EARLY	Test point via at this location can be used to monitor the +12 VDC brought onto the PEX 8548RDK from the male PCI Express board edge connector.
VDD12_J1	Test point via at this location can be used to monitor +12 VDC to Hot Plug slot J1.
VDD12_J2	Test point via at this location can be used to monitor +12 VDC to slot J2.
VDD33	Test point via at this location can be used to monitor +3.3 VDC to the PEX 8548 switch.
VDD33_EARLY	Test point via at this location can be used to monitor +3.3 VDC brought onto the PEX 8548RDK from the male PCI Express board edge connector.
VDD33_J1	Test point via at this location can be used to monitor +3.3 VDC to Hot Plug slot J1.
VDD33_J2	Test point via at this location can be used to monitor +3.3 VDC to slot J2.
VTT	Test point via at this location can be used to monitor VTT voltage to the PEX 8548 switch.

4.1.2 LED Indicators

Table 2 lists the functions of all LED indicators available for use on the PEX 8548RDK.

Table 2. PEX 8548RDK LED Indicators

Location	Silkscreen Label(s)	Color	Function
DS1, DS2, DS3 (Station 0, Ports 0, 1, 2)	DS1, DS2, DS3, Station 0	Green	PORT_GOOD Status Indicator (refer to Figure 7): ▪ **LED is turned On** – Port is active ▪ **LED is turned Off** – Port is inactive
DS6, DS7, DS8 (Station 1, Ports 8, 9, 10)	DS6, DS7, DS8, Station 1		
DS9, DS10, DS11 (Station 2, Ports 12, 13, 14)	DS9, DS10, DS11, Station 2		
DS4	DS4, PWRLED#	Green	HP_PWRLED8# signal Hot Plug indicator for slot J1: ▪ **LED is turned On** – Slot J1 is powered on ▪ **LED is turned On and blinking** – Slot J1 is in the process of being powered On or Off ▪ **LED is turned Off** – Slot J1 is powered Off
DS5	DS5, ATNLED#	Amber	HP_ATNLED8# signal Hot Plug indicator for slot J1: ▪ **LED is turned On** – Slot J1 has an operational problem ▪ **LED is turned On and blinking** – A Hot Plug event for Slot J1 is occurring ▪ **LED is turned Off** – Slot J1 is in standard operation
DS12	DS12, MAN PERST#	Red	When turned On, indicates that PERST# to the PEX 8548 switch is asserted. Momentarily blinks when the PEX 8548RDK first powers up.
DS13 DS14 DS15 DS16 DS17	DS13, STN0 DS14, STN1 DS15, STN2 DS16, PU DS17, 8548	Green	When turned On, the object associated with the LED is connected to the I^2C headers.
DS18	DS18	Amber	When turned On, indicates that PEX_INTA# from the PEX 8548 switch is asserted. Momentarily blinks when the PEX 8548RDK first powers up.
DS19	DS19	Red	When turned On, indicates that FATAL_ERR# from the PEX 8548 switch is asserted. Momentarily blinks when the PEX 8548RDK first powers up.
DS20	DS20, SWITCH-ON	Green	When turned On, indicates that voltages to the PEX 8548 switch are turned On.

4.1.3 Controls

Table 3 lists the functions of all controls available for use on the PEX 8548RDK.

Refer also to Section 3.8, "Strapping Switches – SW7, SW5, SW4, SW6, SW8, and SW3."

Table 3. PEX 8548RDK Controls

Location	Silkscreen Label(s)	Function
SW1	SW1, HP ATN#	Hot Plug Attention Button for slot J1. Momentary SPST pushbutton control.
SW2	SW2, MAN PERST#	Manual assertion of PERST# to the PEX 8548 switch and slot J2. Momentary SPST pushbutton control.
SW3	SW3	DIP switch control of the I^2C interconnect. Switch status is indicated by LEDs DS13 through DS17. (Refer to Table 2.)
SW4	SW4	DIP switch control of the PEX 8548 switch's Strapping balls for the I^2C Slave address and Hot Plug Station 1 (Port 8) HP_MRL8# assertion.
SW5	SW5	DIP switch control of the PEX 8548 switch's Strapping balls for port configuration. A silkscreen table on the component side of the PEX 8548RDK lists the configurations determined by these switches.
SW6	SW6	***Factory Test Only.*** Do not adjust these switches.
SW7	SW7	DIP switch control of the PEX 8548 switch's Strapping balls for upstream port selection. A silkscreen table on the component side of the PEX 8548RDK lists the configurations determined by these switches.
SW8	SW8	Do not adjust these switches, except in the event of an unusual operation. SW8 provides DIP switch control for the following PEX 8548 switch signals: ▪ STRAP_PROBE_MODE# ▪ STRAP_FAST_BRINGUP# ▪ I2C_INTA_ENABLE# ▪ STRAP_SERDES_MODE_ENABLE# ▪ STRAP_PLL_BYPASS#

4.2 Board Layout Information

4.2.1 Trace Routing Design Rules

PCI Express differential pair impedance is 100 Ohms ±5%. The two traces of a differential pair are matched within 5 mil for those pairs that route to the board edge gold fingers, and length-matched within 10 mil for those pairs that route to the slot connectors. Differential pairs that form a common link are matched pair-to-pair within 7.62 cm (3 inches).

Differential pairs routed from the PEX 8548 switch to the board edge gold fingers do not exceed 10.16 cm (4 inches) in length. Differential pairs routed from the PEX 8548 switch to the slot connectors do not exceed 25.4 cm (10 inches) in length.

4.2.2 Power Decoupling

Power decoupling is provided by two means – discrete decoupling capacitors and plane capacitance provided by the PCB layer stackup. The discrete decoupling capacitor footprints are designed such that the inductance between the pad and plane is reduced by careful via placement. (Refer to Figure 15.) Plane capacitance filters noise above approximately 100 MHz.

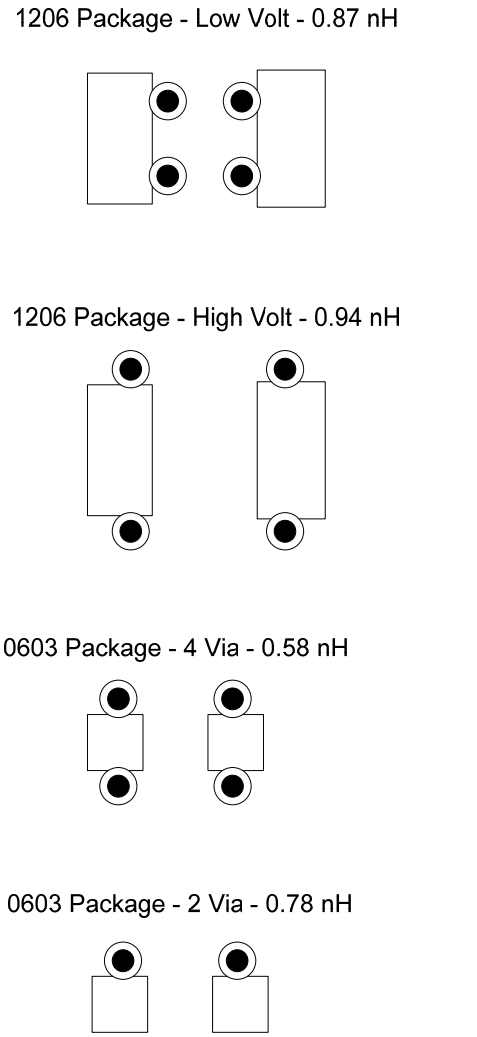


Figure 15. Decoupling Capacitor Footprints

4.2.3 PCB Layer Stackup

The PEX 8548RDK is a 10-layer, 63-mil thick PCB, as illustrated in Figure 16. This stackup includes:

- Four routing layers
- Four ground planes
- Two power planes

The target signal impedance for all routing layers is 57 Ohms ±5% single-ended impedance and 100 Ohms ±5% differential.

This PCB stackup was chosen for the following reasons:

- Power/ground plane arrangement provides capacitance to filter noise above 100 MHz from the supply voltages
- Differential pair routing layers and plane layers arrangement provides shielding for the PCI Express signals

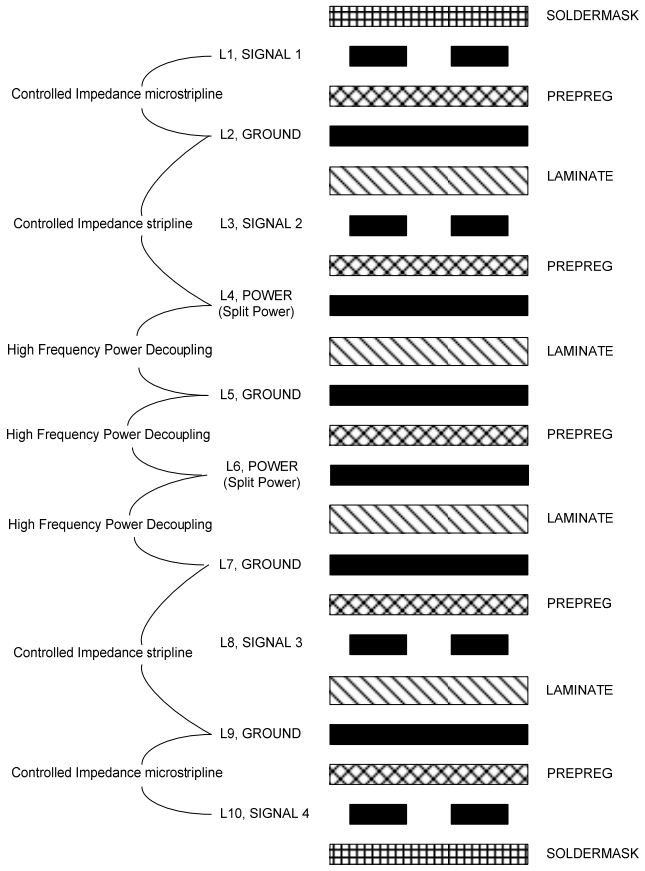


Figure 16. PEX 8548RDK 10-Layer PCB Stackup

5 Frequently Asked Questions

a. When I try to use Port 8 as the upstream port, power and REFCLK to the Station 1 connector (J1) do not turn On.

The board circuitry that turns On power and REFCLK to the Station 1 connector (J1) is controlled by the PEX 8548 switch's Port 8 Hot Plug interface. When this port is used as the upstream port, this interface is turned Off; therefore, power and REFCLK to J1 are turned Off as well.

Note: *The Hot Plug interface signals are driven Off, not floated; therefore, trying to force these signals High or Low might damage the PEX 8548 switch.*

b. The Station 2 connector (J2) does not seem to be receiving power.

Ensure that a power connector is plugged into P2 and that both voltages are being delivered.

c. The PEX 8548RDK does not include a heat sink. Is one required?

The **PEX 8548RDK** is designed to be a hardware and software development platform to facilitate getting designs up and running quickly. As such, it is designed to be used in laboratory environments. If ambient temperatures are expected to be above 40 °C, consult the *PEX 8548AA Data Book* to determine cooling requirements.

6 Bill of Materials

This section replicates the PEX 8548RDK Bill of Materials.

PLX Part # 91-0062-100-A									
Product Name: PEX 8548-AA RDK									
Item #	**Qty**	**Mfgr**	**Mfgr Part #**	**Desc**	**Package Type**	**Component Designator(s)**	**Distributor**	**Dist Part #**	**Part**
SURFACE MOUNT COMPONENTS									
1	3	Panasonic	ECJ-3YB1C106M	CAP 10UF 16V CERAMIC X5R 1206 LOVOLT FOOTPRINT	SMT, 1206, LoVolt	C1, C81, C125	Digi-Key	PCC2227CT-ND	10uF
2	110	Kemet	C0402C104K8PACTU	CAP .10UF 10V CERAMIC X5R 0402	SMT, 0402	C2, C3, C4, C5, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C43, C45, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C84, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C122, C144, C159, C204, C205	Digi-Key	399-3027-1-ND	0.1uF
3	6	AVX	TAJC226K020R	CAP TANTALUM 22UF 20V 10% SMD	EIA size C	C6, C7, C47, C48, C85, C86	Digi-Key	478-1711-1-ND	22uF
4	3	Kemet	C0603C104K3RACTU	CAP .1UF 25V CERAMIC X7R 0603	SMT, 0603	C40, C42, C46	Digi-Key	399-1281-1-ND	0.1uF
5	2	Kemet	C0603C103K5RACTU	CAP 10000PF 50V CERAMIC X7R 0603	SMT, 0603	C41, C44	Digi-Key	399-1091-1-ND	0.01uF
6	2	Kemet	C0603C105K8PACTU	CAP CERAMIC 1.0UF 10V X5R 0603, 2 VIA	SMT, 0603, 2via	C82, C126	Digi-Key	399-3118-1-ND	1uF
7	1	Panasonic	ECJ-1VB1H473K	CAP .047UF 50V CERAMIC X7R 0603	SMT, 0603	C121	Digi-Key	PCC2286CT-ND	0.047uF

Item #	Qty	Mfgr	Mfgr Part #	Desc	Package Type	Component Designator(s)	Distributor	Dist Part #	Part
8	1	Kemet	C1206C156K9PACTU	CAP 15UF 6.3V CER X5R SMD 1206 LOVOLT FOOTPRINT	SMT, 1206, LoVolt	C127	Digi-Key	399-3227-1-ND	15uF
9	2	Kemet	C1206C226K9PACTU	CAP 22UF 6.3V CER X5R SMD 1206 LOVOLT FOOTPRINT	SMT, 1206, LoVolt	C128, C129	Digi-Key	399-3229-1-ND	22uF
10	35	Panasonic	ECJ-0EB1E102K	CAP 1000PF 25V CERAMIC 0402 SMD	SMT, 0402	C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C145, C146, C147, C148, C149, C150, C151, C152, C153, C154, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169, C170, C171, C172, C173, C174	Digi-Key	PCC102BQCT-ND	0.001uF
11	13	Panasonic	ECJ-0EB1C103K	CAP 10000PF 16V CERAMIC 0402 SMD	SMT, 0402	C140, C141, C142, C143, C155, C156, C157, C158, C192, C193, C194, C195, C196	Digi-Key	PCC103BQCT-ND	0.01uF
12	10	Panasonic	ECJ-0EB1E222K	CAP 2200PF 25V CERAMIC 0402 SMD	SMT, 0402	C175, C176, C177, C178, C179, C180, C181, C182, C183, C184	Digi-Key	PCC222BQCT-ND	0.0022uF
13	7	Panasonic	ECJ-0EB1E472K	CAP 4700PF 25V CERAMIC 0402 SMD	SMT, 0402	C185, C186, C187, C188, C189, C190, C191	Digi-Key	PCC472BQCT-ND	0.0047uF
14	4	Panasonic	ECJ-0EB1C223K	CAP 22000PF 16V CERAMIC X7R 0402	SMT, 0402	C197, C198, C199, C200	Digi-Key	PCC2138CT-ND	0.022uF
15	3	Panasonic	ECJ-0EB1A473K	CAP 47000PF 10V CERAMIC X5R 0402	SMT, 0402	C201, C202, C203	Digi-Key	PCC2142CT-ND	0.047uF
16	1	Panasonic	ECJ-0EB0J224K	CAP .22UF 6.3V CERAMIC X5R 0402	SMT, 0402	C206	Digi-Key	PCC2269CT-ND	0.22uF
17	16	Panasonic	LNJ308G8LRA	LED GREEN SS TYPE LOW CUR SMD	SMT, 0603	DS1, DS2, DS3, DS4, DS6, DS7, DS8, DS9, DS10, DS11, DS13, DS14, DS15, DS16, DS17, DS20	Digi-Key	P521CT-ND	Green
18	2	Panasonic	LNJ408K8ZRA	LED AMBER SS TYPE LOW CUR SMD	SMT, 0603	DS5, DS18	Digi-Key	P522CT-ND	Amber
19	2	Panasonic	LNJ208R8ARA	LED RED HI BRT SS TYPE LO CUR SM	SMT, 0603	DS12, DS19	Digi-Key	P524CT-ND	Red
20	1	Molex	87767-0123	PCI Express x16 straddle-mount connector	SMT, 164-pin	J1			PCI_EXP_X16_STRADDLE_MNT_CONN

Item #	Qty	Mfgr	Mfgr Part #	Desc	Package Type	Component Designator(s)	Distributor	Dist Part #	Part
21	2	International Rectifier	IRF7470	MOSFET, N-CHAN, 10A, Rds=13 mohm	SO8	Q1, Q2			IRF7470
22	1	Fairchild	FDN371N	MOSFET, N-CHAN, 2.5A, Rds=60 mohm	SuperSOT-3	Q3			FDN371N
23	4	ON Semiconductor	MMBT3904LT1	NPN, GPSS, MMBT3904, SOT23	SOT23-3	Q4, Q5, Q6, Q7			MMBT3904LT1
24	2	CTS Resistor Products	742-083-512-J	RESNET, MF, 5.1 KOHM NIL 5%, ISOLATED	742-CTS-RN-8	RN1, RN2	Digi-Key	742C083512JCT-ND	5.1K
25	2	Yageo	9C08052A0R00JLHFT	RES 0.0 OHM 1/8W 5% 0805 SMD	SMT, 0805	R1, R90	Digi-Key	311-0.0ACT-ND	0
26	9	Panasonic	ERJ-3EKF33R2V	RES 33.2 OHM 1/16W 1% 0603 SMD	SMT, 0603	R2, R3, R6, R7, R12, R14, R22, R23, R77	Digi-Key	P33.2HCT-ND	33.2
27	8	Panasonic	ERJ-3EKF49R9V	RES 49.9 OHM 1/16W 1% 0603 SMD	SMT, 0603	R4, R5, R8, R9, R17, R19, R24, R25	Digi-Key	P49.9HCT-ND	49.9
28	20	Panasonic	ERJ-3GEYJ512V	RES 5.1K OHM 1/10W 5% 0603 SMD	SMT, 0603	R10, R13, R16, R18, R20, R28, R29, R30, R38, R40, R44, R45, R46, R47, R51, R61, R62, R91, R94, R95	Digi-Key	P5.1KGCT-ND	5.1K
29	2	Yageo	9C06031A0R00JLHFT	RES, Shunt Select Footprint, 0603	SMT, 0603-2	R11, R15	Digi-Key	311-0.0GCT-ND	0 Shunt
30	1	Panasonic	ERJ-3EKF4750V	RES 475 OHM 1/16W 1% 0603 SMD	SMT, 0603	R21	Digi-Key	P475HCT-ND	475
31	9	Yageo	9C06031A0R00JLHFT	RES 0.0 OHM 1/10W 5% 0603 SMD	SMT, 0603	R26, R27, R31, R35, R54, R81, R82, R83, R84	Digi-Key	311-0.0GCT-ND	0
32	20	Panasonic	ERJ-3GEYJ391V	RES 390 OHM 1/10W 5% 0603 SMD	SMT, 0603	R32, R33, R34, R42, R43, R48, R49, R50, R55, R56, R57, R60, R63, R64, R65, R66, R71, R78, R79, R96	Digi-Key	P390GCT-ND	390
33	2	Panasonic	ERJ-3GEYJ200V	RES 20 OHM 1/10W 5% 0603 SMD	SMT, 0603	R36, R39	Digi-Key	P20GCT-ND	20
34	1	Panasonic	ERJ-3EKF1002V	RES 10.0K OHM 1/16W 1% 0603 SMD	SMT, 0603	R37	Digi-Key	P10.0KHCT-ND	10.0K
35	22	Panasonic	ERJ-3GEYJ512V	RES, Shunt Select Footprint, 0603	SMT, 0603-2	R41, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121	Digi-Key	P5.1KGCT-ND	5.1K

Item #	Qty	Mfgr	Mfgr Part #	Desc	Package Type	Component Designator(s)	Distributor	Dist Part #	Part
36	2	Panasonic	ERJ-3EKF2261V	RES 2.26K OHM 1/10W 1% 0603 SMD	SMT, 0603	R58, R59	Digi-Key	P2.26KHCT-ND	2.26K
37	4	Panasonic	ERJ-3GEYJ102V	RES 1.0K OHM 1/10W 5% 0603 SMD	SMT, 0603	R67, R68, R69, R97	Digi-Key	P1.0KGCT-ND	1K
38	1	Panasonic	ERJ-3GEYJ152V	RES 1.5K OHM 1/10W 5% 0603 SMD	SMT, 0603	R76	Digi-Key	P1.5KGCT-ND	1.5K
39	2	Panasonic	ERJ-3GEYJ103V	RES 10K OHM 1/10W 5% 0603 SMD	SMT, 0603	R80, R93	Digi-Key	P10KGCT-ND	10K
40	1	Panasonic	ERJ-3GEYJ333V	RES 33K OHM 1/10W 5% 0603 SMD	SMT, 0603	R92	Digi-Key	P33KGCT-ND	33K
41	1	Panasonic	ERJ-3GEYJ273V	RES 27K OHM 1/10W 5% 0603 SMD	SMT, 0603	R98	Digi-Key	P27KGCT-ND	27K
42	1	Panasonic	ERJ-3EKF2001V	RES 2.00K OHM 1/10W 1% 0603 SMD	SMT, 0603	R99	Digi-Key	P2.00KHCT-ND	2.00K
43	1	Panasonic	ERJ-3EKF1001V	RES 1.00K OHM 1/10W 1% 0603 SMD	SMT, 0603	R100	Digi-Key	P1.00KHCT-ND	1.00K
44	2	Omron	B3S-1002	SWITCH TACT 6MM SMD MOM 230GF		SW1, SW2	Digi-Key	SW416-ND	B3S-1002
45	1	PLX Technology	PEX8548-AA25BI	IC, 48-lane, 3-station, 9-port, PCI Express switch	PBGA736	U1			PEX8548-AA25BI
46	1	ICS	ICS9DB104yFLFT	IC, 1:4 100MHz Differential Clock Fanout	SSOP28	U2			ICS9DB104
47	1	Fairchild	NC7SZ04P5X	IC, NOT GATE	SC70-5	U3			NC7SZ04P5X
48	5	Maxim	MAX4722EUA	IC, Analog Switch, Dual, SPST, 4.5 ohm, NC	uMAX8	U4, U6, U9, U10, U13			MAX4722EUA
49	1	Intersil	ISL6161CB	IC, Hot Swap Controller, Dual, PCIEx	SOIC14	U5	Arrow		ISL6161
50	1	Fairchild	NC7SZ126P5X	IC, BUFFER, 24mA drive	SC70-5	U7			NC7SZ126P5X

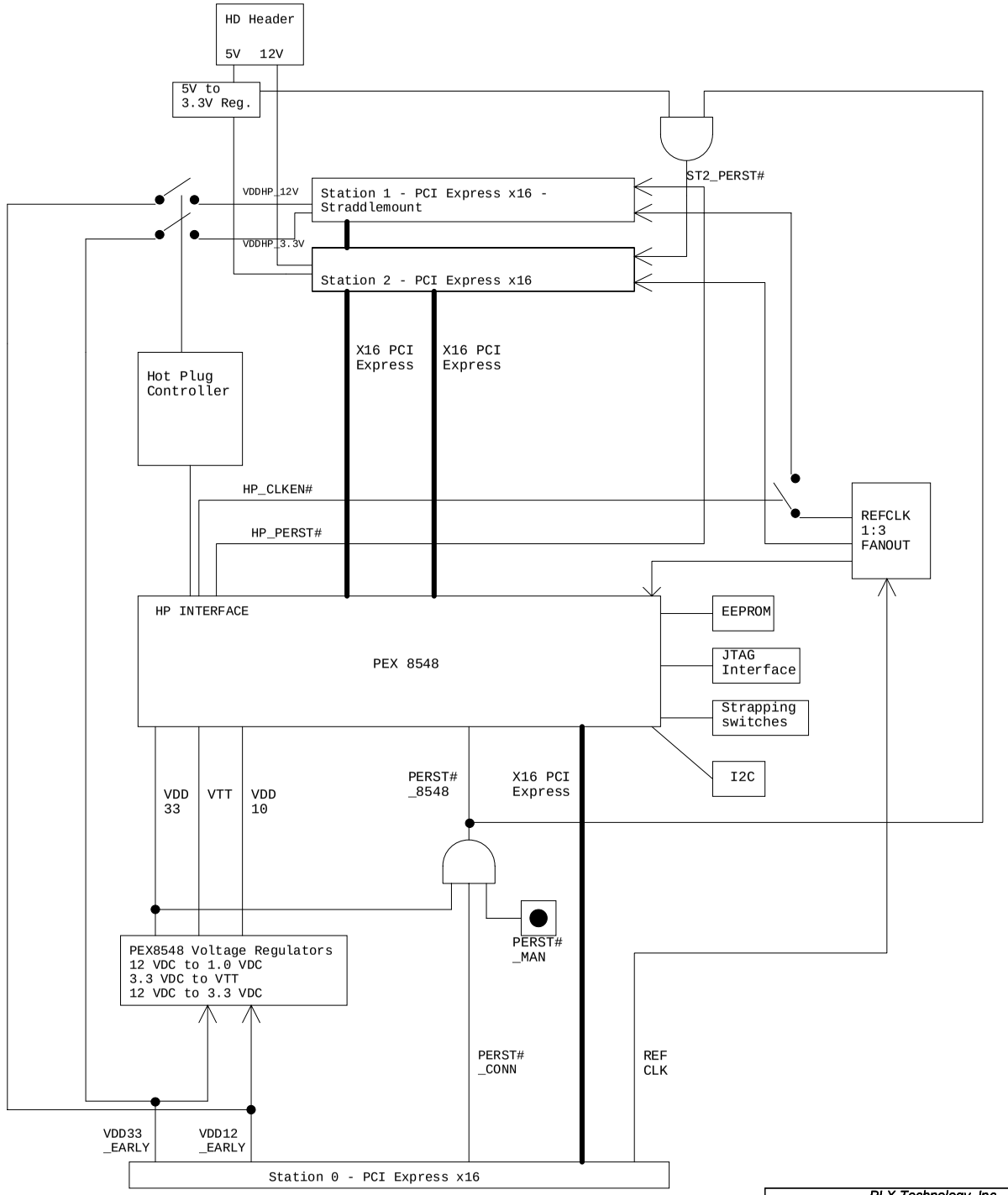
Item #	Qty	Mfgr	Mfgr Part #	Desc	Package Type	Component Designator(s)	Distributor	Dist Part #	Part
51	1	Belfuse	S7AH-08B330	IC, Non-iso DC/DC converter, 5V-to-3.3V @ 8A	SMT, 7-pin Belfuse	U8			S7AH-08B330
52	1	Maxim	MAX6412UK29-T	IC, Reset controller, 2.9V threshold, Adj. reset timeout	SOT23-5	U11			MAX6412
53	1	Fairchild	NC7SZ08P5X	IC, AND Gate, Tpd=15nsec	SC70-5	U12			NC7SZ08
54	1	Belfuse	S7AH-08E1A00	IC, Non-iso DC/DC converter, 12V-to-1V @ 8A	SMT, 7-pin Belfuse	U15			S7AH-08E1A00
55	1	Maxim	MAX8556ETE	IC, V-REG, 4 A, ADJ, Enable, POK	Thin QFN16	U16			MAX8556
THROUGH-HOLE COMPONENTS									
100	3	Vishay	94SP187X0016EBP	CAP, Oscon, 180uF, 16V	E case	C83, C123, C124			180uF
101	1	Amp	103308-1	CONN HEADER LOPRO STR 10POS 15AU	0.1" 2x5	JP1	Digi-Key	A26267-ND	I2C
102	1	3M	929710-10-02	CONN HEADER .100 DUAL STR 4POS	0.1" 2x2	JP2	Digi-Key	929710-10-02-ND	HEADER 2X2
103	1	Amp	103308-1	CONN HEADER LOPRO STR 10POS 15AU	0.1" 2x5	JP3	Digi-Key	A26267-ND	JTAG Header
104	1	Molex	87715-3302	PCI Express x16 Through-hole connector	TH, 164-pin	J2			PCI_EXP_X16_FEMALE_CONN
105	1	Molex	15-24-4449	Header, HD 4-pin, straight		P2	Arrow		IDE4_HEADER

Item #	Qty	Mfgr	Mfgr Part #	Desc	Package Type	Component Designator(s)	Distributor	Dist Part #	Part
106	4	Grayhill	76SB06T	SWITCH DIP EXT RCKR UNSEALD 6POS	DIP12	SW3, SW5, SW6, SW8	Digi-Key	GH7174-ND	SW DIP-6
107	2	Grayhill	76SB04T	SWITCH DIP EXT RCKR UNSEALD 4POS	DIP8	SW4, SW7	Digi-Key	GH7170-ND	SW DIP-4
108	8	FCI	76201-023	TERM, PIN, PRESS-FIT, .025inSq, .230Lng		TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8			Stakepin
109	1	Mill-Max	210-93-308-41-001000	Socket, EEPROM, DIP8, Thru-hole	DIP8	U14	Digi-Key	ED60000-ND	AT25128A
MANUALLY INSERTED COMPONENTS									
200	1	Atmel	AT25128A-10PI-2.7	IC SRL EE 128K 2.7V 8DIP	DIP-8	U14	Digi-Key	AT25128A-10PI-2.7-ND	AT25128A
MISCELLANEOUS COMPONENTS									
300	1	Keystone	9203	Bracket, PCI, blank					
301	1	PLX Technology	90-0062-100-A	PCIe 48 LANE SWITCH RDK PCB Rev 100					
PARTS THAT SHOULD NOT BE ASSEMBLED									
400	7	Yageo	9C06031A0R00JLHFT	RES 0.0 OHM 1/10W 5% 0603 SMD	SMT, 0603	R52, R53, R70, R72, R73, R74, R75	Digi-Key	311-0.0GCT-ND	NL

7 Schematics

This section provides a copy of the PEX 8548RDK Schematics.

Schematic Table of Contents



Revision History

Rev. #	Date	Reason for Revision
000	June 11, 2006	Distributed for Comprehensive Design Review
001	July 7, 2006	Power-Up Circuit Changed to Reduce Cost
002	July 19, 2006	Results of July 7 Design Review Incorporate
003	August 18, 2006	DIP switch pullups changed to pullup/pulldown
100	September 29, 2006	VDD10S connections corrected

PLX Technology, Inc.
870 Maude Avenue
Sunnyvale, CA 94085
www.plxtech.com

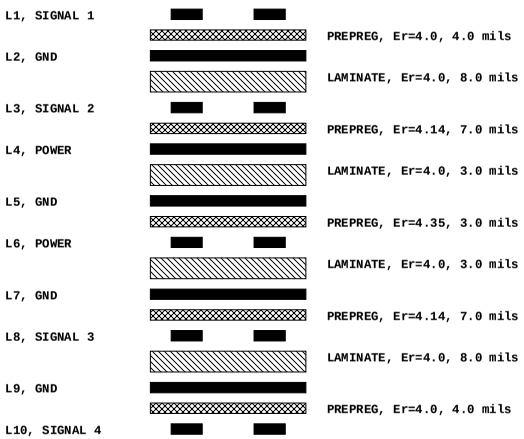
Title: PEX8548 RDK - Functional Block Diagram

Size: C | Document Number: 91-0062-100-A | Rev: 100

Date: Friday, September 29, 2006 | Sheet 1 of 9

Board Thickness = 63 mils

LAYER STACKUP



PEX 8548 voltages are carried on 3.3V, 1.0V, and VTT.

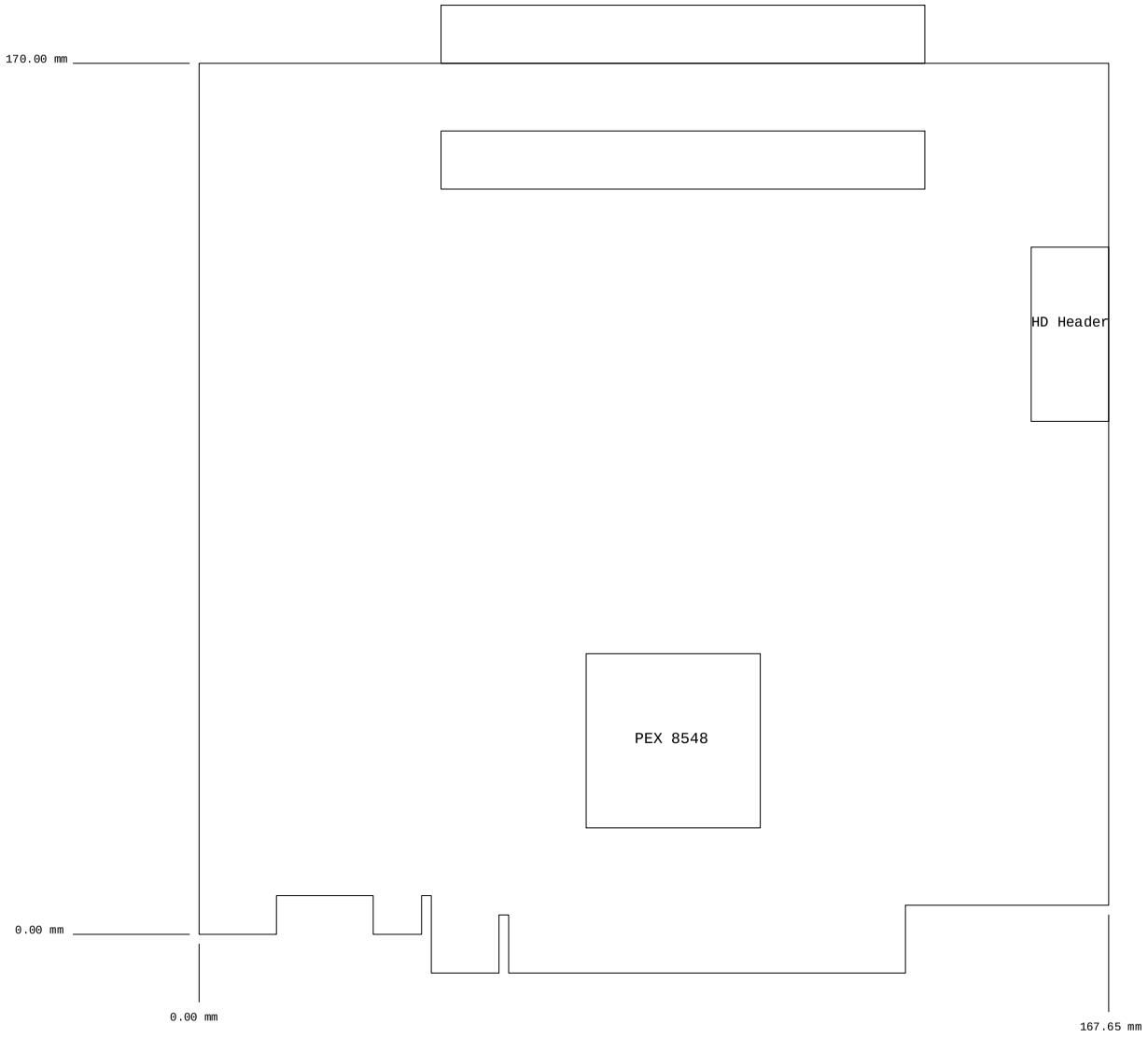
OUTER TRACES

WIDTH = 5.0 mils
Cu = 1.50 oz
Trave Zo = 52 ohm
DIFF Trace Zo = 100 ohm

INNER TRACES

WIDTH = 4.0 mils
Cu = 0.50 oz
Trace Zo = 52 ohm
DIFF Trace Zo = 100 ohm

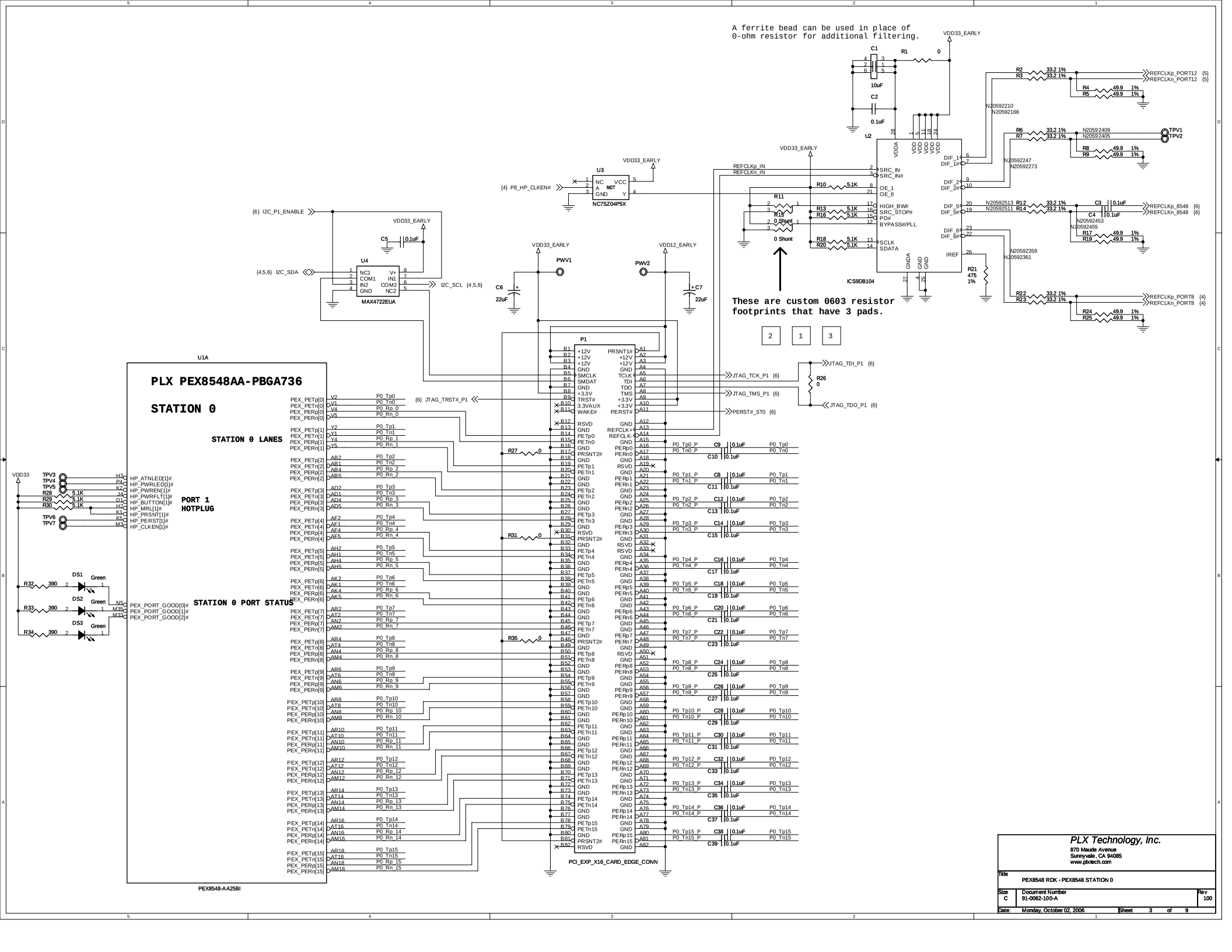
NL = No Load



PLX Technology, Inc. 870 Maude Avenue Sunnyvale, CA 94085 www.plxtech.com		
Title: PEX8548 RDK - Board Layout Information		
Size: C	Document Number: 91-0062-100-A	Rev: 100
Date: Friday, September 29, 2006	Sheet 2 of 9	

A ferrite bead can be used in place of
0-ohm resistor for additional filtering.

These are custom 0603 resistor
footprints that have 3 pads.



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Sunnyvale, CA 94085
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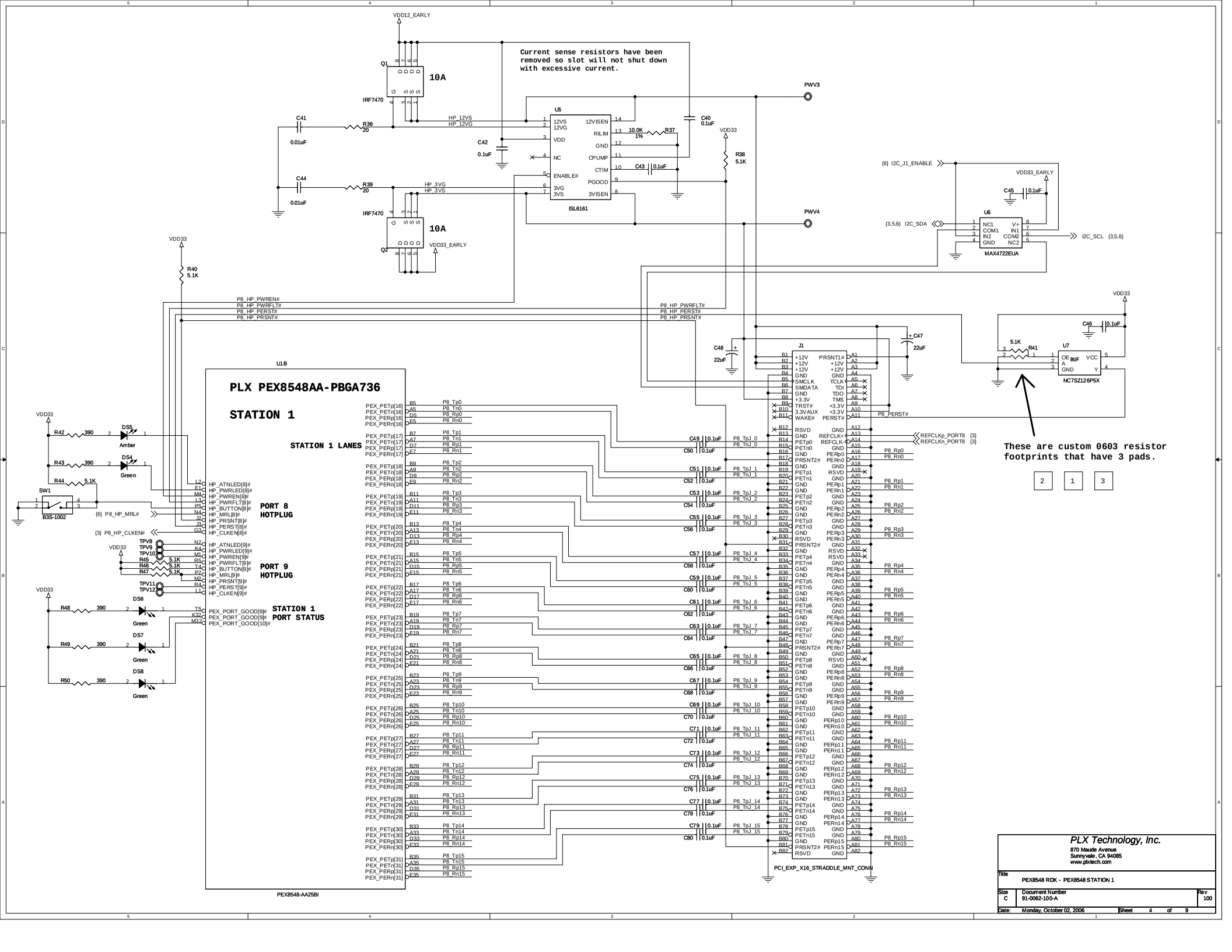
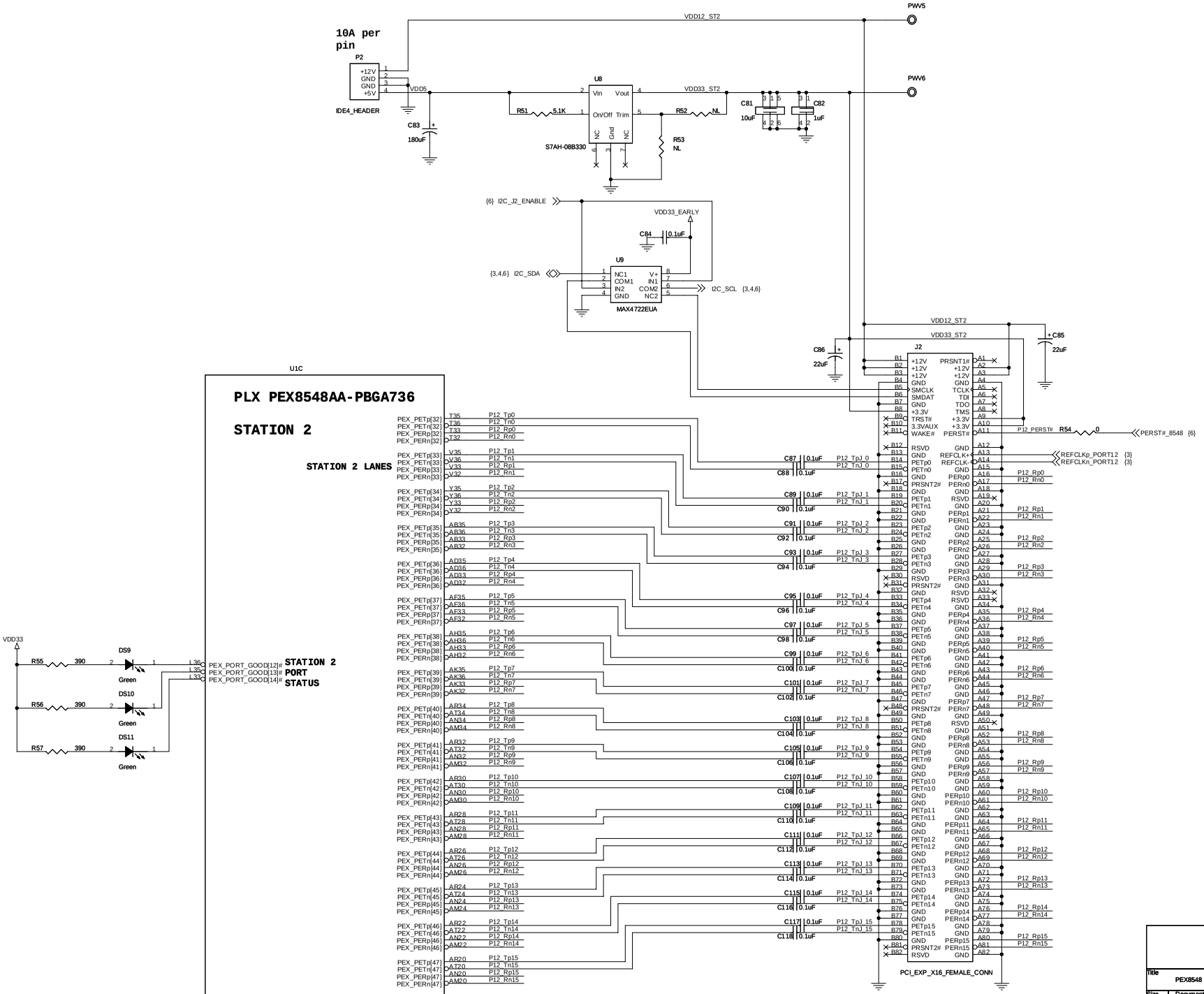
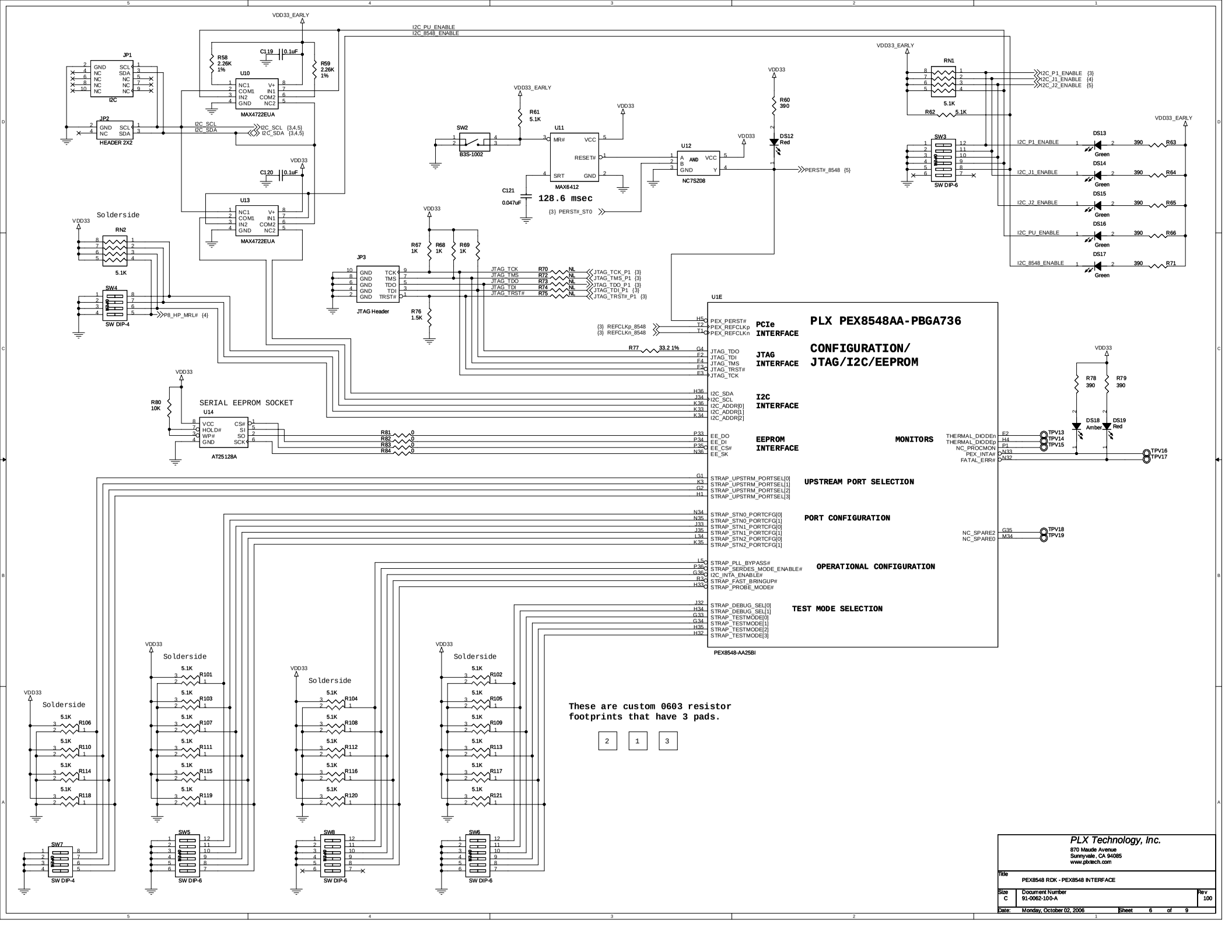
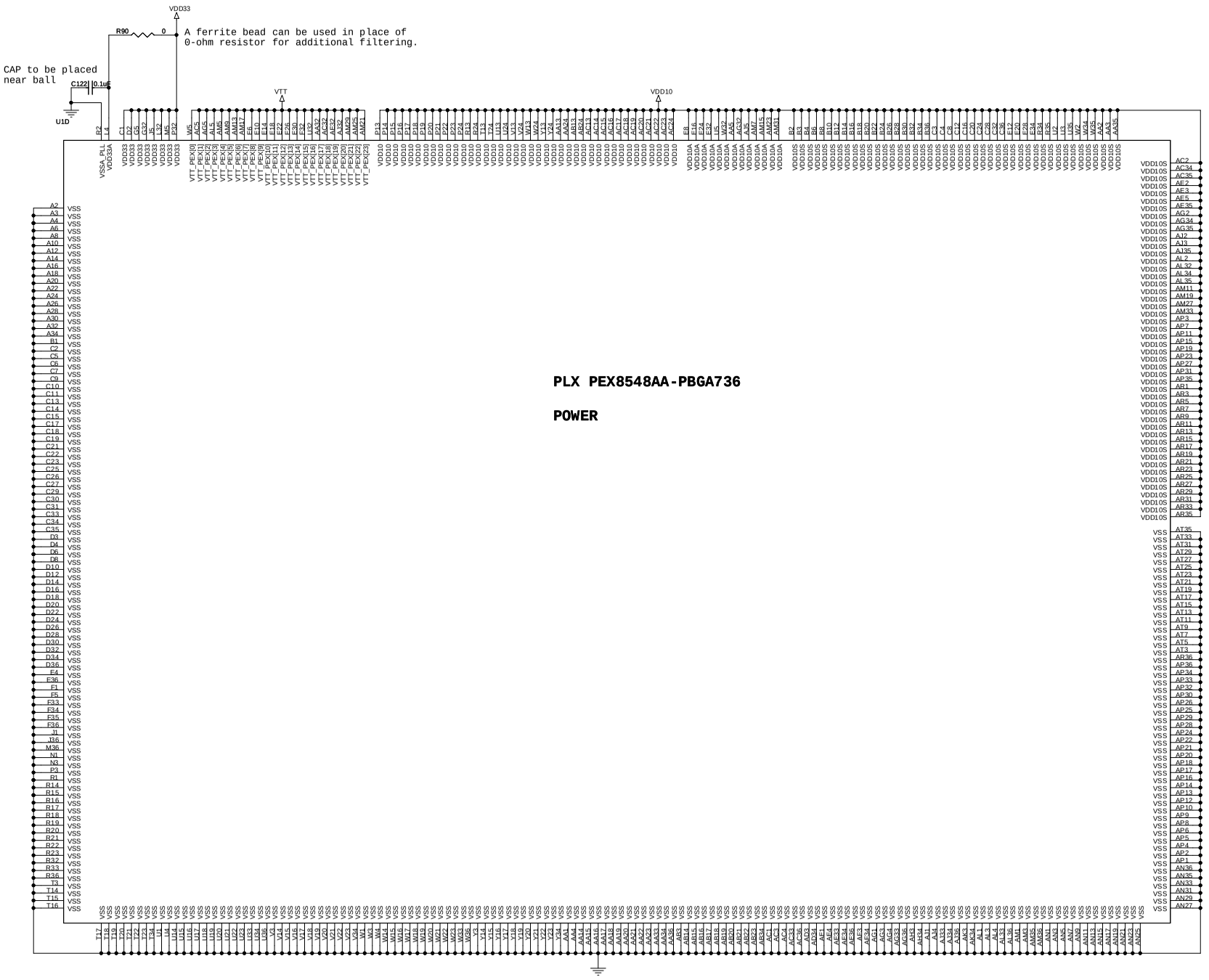
Title	PEX8548 RDK - PEX8548 STATION 0	
Size: C	Document Number: 91-0062-100-A	Rev: 100
Date: Monday, October 02, 2006	Sheet 3 of 9	


Current sense resistors have been removed so slot will not shut down with excessive current.
VDD12_EARLY
Q1
IRF7470
10A
Q2
IRF7470
10A
VDD33_EARLY
U5
ISL6161
12VS
12VG
VDD
NC
ENABLE#
3VG
3VS
12VISEN
RILIM
GND
CPUMP
CTIM
PGOOD
3VISEN
HP_12VS
HP_12VG
HP_3VG
HP_3VS
C41
0.01uF
C42
0.1uF
C43
0.1uF
C44
0.01uF
C40
0.1uF
R36
20
R37
10.0K
1%
R38
5.1K
R39
20
PWV3
PWV4
VDD33
U6
MAX4722EUA
NC1
COM1
IN2
GND
V+
IN1
COM2
NC2
{6} I2C_J1_ENABLE
{3,5,6} I2C_SDA
I2C_SCL {3,5,6}
VDD33_EARLY
C45
0.1uF
R40
5.1K
P8_HP_PWREN#
P8_HP_PWRFLT#
P8_HP_PERST#
P8_HP_PRSNT#
C48
22uF
C47
22uF
C46
0.1uF
R41
5.1K
U7
NC7SZ126P5X
OE
A
GND
VCC
Y
8UF
These are custom 0603 resistor footprints that have 3 pads.
2
1
3
U1B
PLX PEX8548AA-PBGA736
STATION 1
STATION 1 LANES
PEX8548-AA25BI
PORT 8 HOTPLUG
PORT 9 HOTPLUG
STATION 1 PORT STATUS
HP_ATNLED[8]#
HP_PWRLED[8]#
HP_PWREN[8]#
HP_PWRFLT[8]#
HP_BUTTON[8]#
HP_MRL[8]#
HP_PRSNT[8]#
HP_PERST[8]#
HP_CLKEN[8]#
HP_ATNLED[9]#
HP_PWRLED[9]#
HP_PWREN[9]#
HP_PWRFLT[9]#
HP_BUTTON[9]#
HP_MRL[9]#
HP_PRSNT[9]#
HP_PERST[9]#
HP_CLKEN[9]#
PEX_PORT_GOOD[8]#
PEX_PORT_GOOD[9]#
PEX_PORT_GOOD[10]#
{6} P8_HP_MRL#
{3} P8_HP_CLKEN#
SW1
B3S-1002
DS5
Amber
DS4
Green
DS6
Green
DS7
Green
DS8
Green
R42
390
R43
390
R44
5.1K
R45
5.1K
R46
5.1K
R47
5.1K
R48
390
R49
390
R50
390
TPV8
TPV9
TPV10
TPV11
TPV12
J1
PCI_EXP_X16_STRADDLE_MNT_CONN
P8_PERST#
REFCLKp_PORT8 {3}
REFCLKn_PORT8 {3}
PLX Technology, Inc.
870 Maude Avenue
Sunnyvale, CA 94085
www.plxtech.com
Title
PEX8548 RDK - PEX8548 STATION 1
Size C
Document Number 91-0062-100-A
Rev 100
Date: Monday, October 02, 2006
Sheet 4 of 9

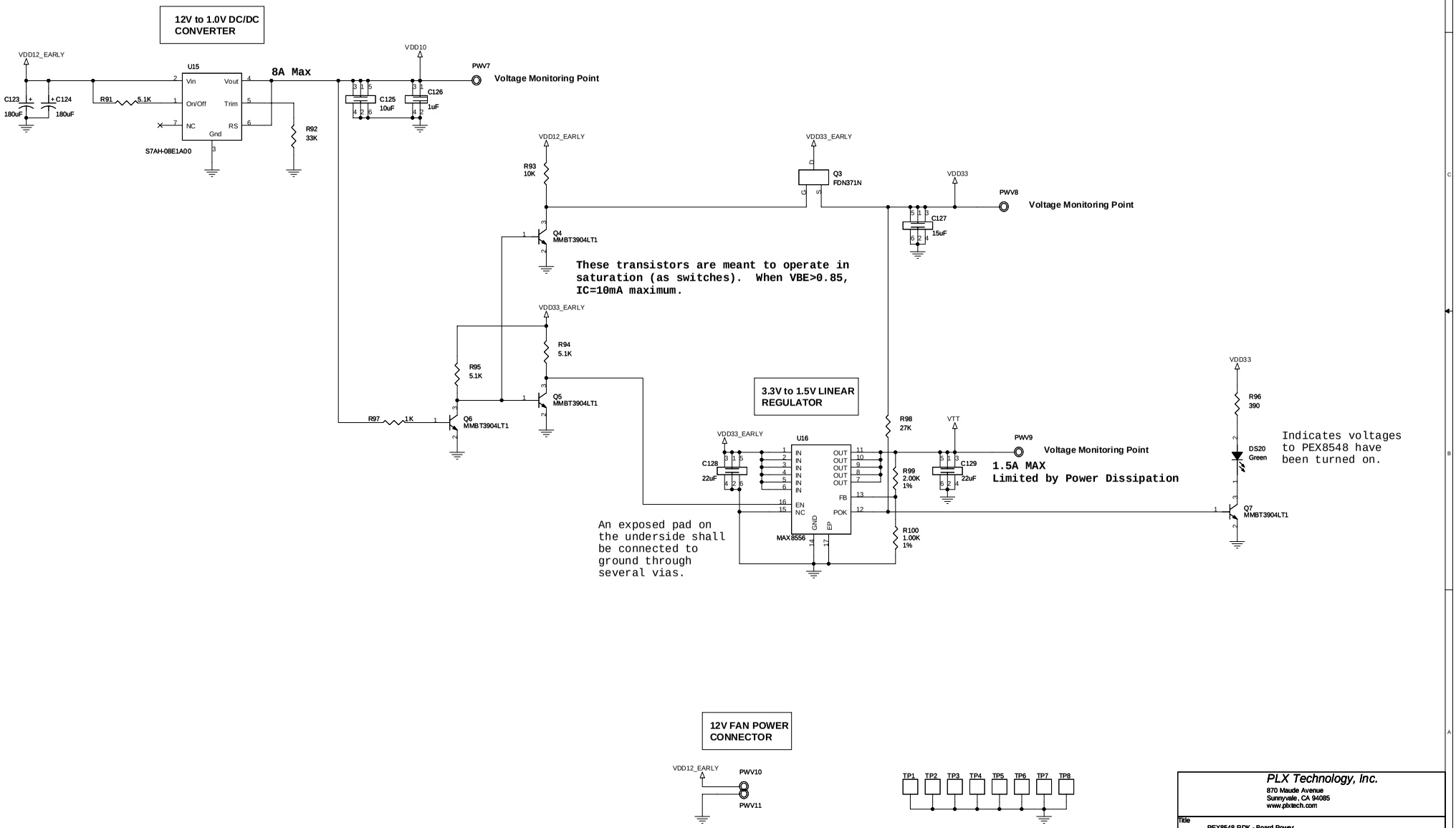


PLX Technology, Inc.		
870 Maude Avenue Sunnyvale, CA 94085 www.plxtech.com		
Title: PEX8548 RDK - PEX8548 STATION 2		
Size: C	Document Number: 91-0062-100-A	Rev: 100
Date: Monday, October 02, 2006	Sheet 5 of 9	


PLX PEX8548AA-PBGA736
CONFIGURATION/
JTAG/I2C/EEPROM
PCIe INTERFACE
JTAG INTERFACE
I2C INTERFACE
EEPROM INTERFACE
MONITORS
UPSTREAM PORT SELECTION
PORT CONFIGURATION
OPERATIONAL CONFIGURATION
TEST MODE SELECTION
SERIAL EEPROM SOCKET
JTAG Header
128.6 msec
Solderside
These are custom 0603 resistor footprints that have 3 pads.
PLX Technology, Inc.
870 Maude Avenue
Sunnyvale, CA 94085
www.plxtech.com
PEX8548 RDK - PEX8548 INTERFACE
Document Number 91-0062-100-A
Rev 100
Monday, October 02, 2006
Sheet 6 of 9



PLX Technology, Inc.	
870 Maude Avenue Sunnyvale, CA 94085 www.plxtech.com	
Title	PEX8548 RDK - PEX8548 POWER
Size: C	Document Number: 91-0062-100-A
Rev: 100	
Date: Monday, October 02, 2006	Sheet 7 of 9



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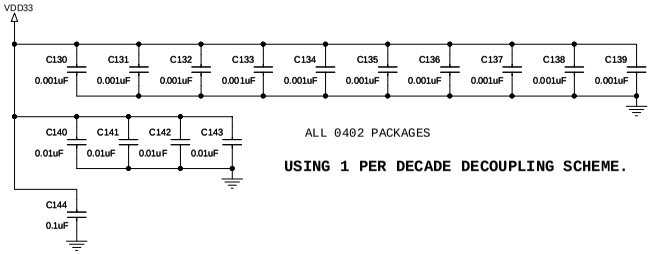
Title	PEX8548 RDK - Board Power	
Size: C	Document Number: 91-0062-100-A	Rev: 100
Date: Friday, September 29, 2006	Sheet 8 of 9	



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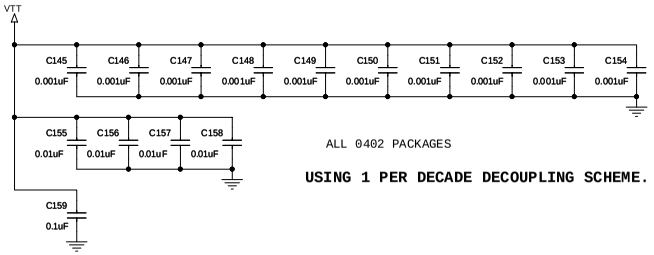
USING 1 PER DECADE DECOUPLING SCHEME.



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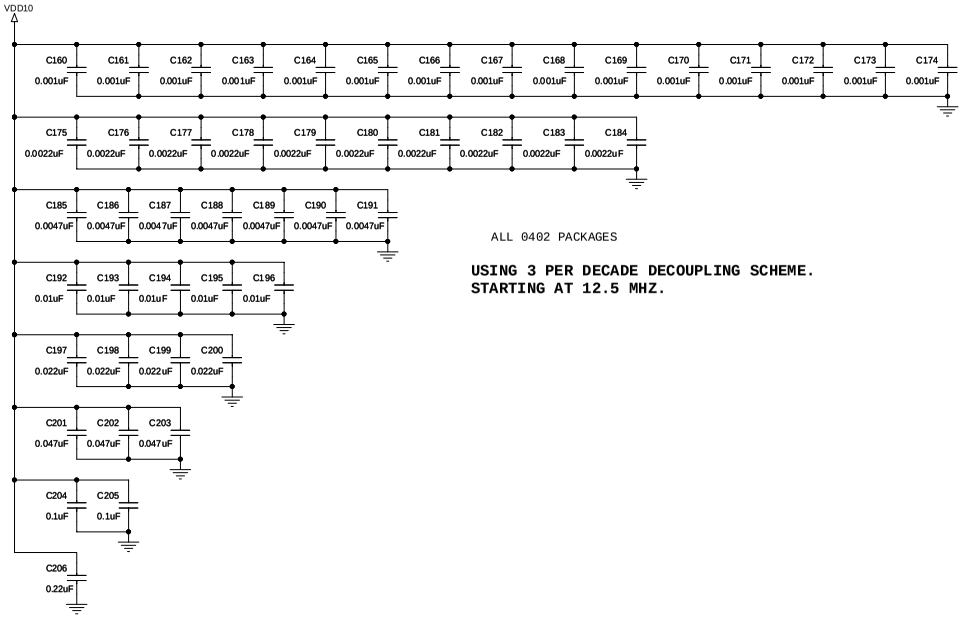

ALL 0402 PACKAGES

USING 3 PER DECADE DECOUPLING SCHEME.
STARTING AT 12.5 MHZ.

PLX Technology, Inc.
870 Maude Avenue
Sunnyvale, CA 94085
www.plxtech.com

Title	PEX8548 RDK - Power Decoupling	
Size: C	Document Number: 91-0062-100-A	Rev: 100
Date: Friday, September 29, 2006	Sheet 9 of 9	

8 References

The following is a list of documentation to provide further details.

- PLX Technology, Inc.
  870 W Maude Avenue, Sunnyvale, CA 94085 USA
  Tel: 800 759-3735 (domestic only) or 408 774-9060, Fax: 408 774-2169, www.plxtech.com
  - *PEX 8548AA Data Book, Version 1.0* or higher
- PCI Special Interest Group (PCI-SIG)
  3855 SW 153rd Drive, Beaverton, OR 97006 USA
  Tel: 503 619-0569, Fax: 503 644-6708, www.pcisig.com
  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI Bus Power Management Interface Specification, Revision 1.2*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2*
  - *PCI Express Base Specification, Revision 1.1*
  - *PCI Express Card Electromechanical (CEM) Specification, Revisions 1.0a and 1.1*
- *NXP Semiconductors*
  www.standardics.nxp.com
  - *The I2C-Bus Specification, Version 2.1*