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PEX 8508RDK
Hardware Reference Manual

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Hardware Reference Manual

Version 1.3

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PREFACE

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ABOUT THIS MANUAL

This document describes the PLX PEX 8508RDK, a Rapid Development Kit, from a hardware perspective. It contains a description of all major functional circuit blocks on the board and also is a reference for the creation of software for this product. This manual also includes complete schematics and bill of materials.

REVISION HISTORY

Date	Version	Comments
December 2005	0.90	Hardware Reference Manual initial release.
December 2005	0.91	Update schematic
January 2006	1.0	Update schematic and BOM. Added D27, D28, R136, and R137
May 2006	1.1	Updated the PEX 8508 schematic symbol to match the databook.
November 2006	1.2	Updated the schematic and BOM. Updated to rev AB silicon.
April 2007	1.3	Updated the schematic and BOM. Updated to rev AC silicon.

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1. General Information

The PLX PEX 8508RDK is a Rapid Development Kit based on the PEX 8508, a 8-lane, 5-port PCI Express switch. The PEX 8508RDK provides a complete hardware and software development platform to facilitate getting designs up and running quickly, lowering risk and reducing time-to-market. This RDK allows the upstream port of the PEX 8508 to be directly plugged into a system board's x16/x8/x4 PCI Express connector, or plugged into an x1 PCI Express connector by using card edge adapters.

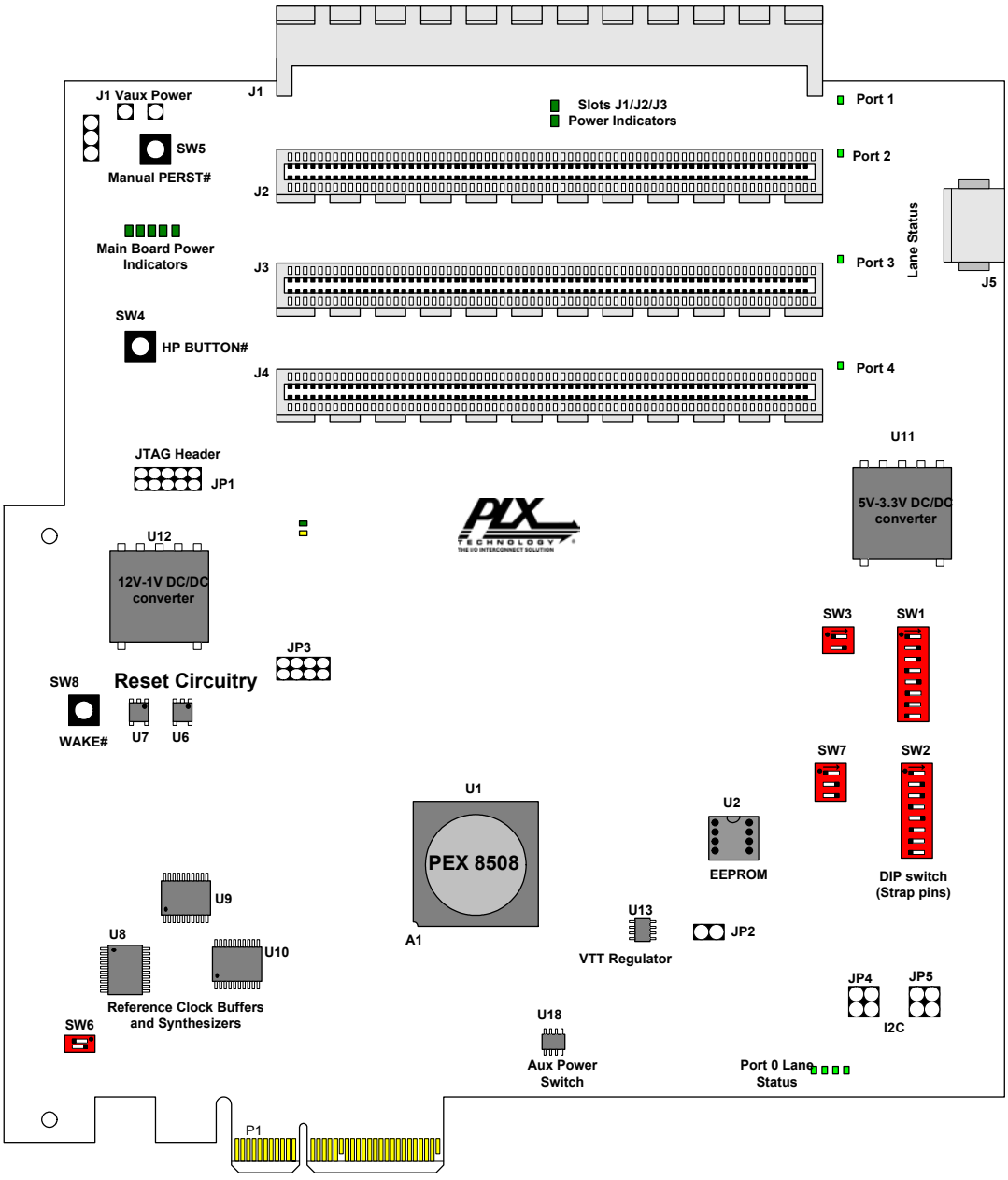

Figure 1-1. PEX 8508RDK Component Side View

1.1 PEX 8508 Features

- 8-lane, 5-port (maximum) PCI Express switch
- PCI Express Base Specification version r1.1 and PCI Standard Hot-Plug Controller and Subsystem Specification, revision 1.0 compliance
- Eight PCI Express lanes provide 40 Gbps aggregate bandwidth
- Non-blocking internal crossbar architecture supports full wire speed
- Out of band communication/initialization interfaces (Serial EEPROM and I2C)
- Maximum packet payload size of 256 bytes
- Performance tuning
- Up to 5-ports (Up to 9 possible port configurations)
- Assign x1, x2, x4, or x8 lanes per port
- Allows any port to be designated as upstream port
- Configuration with strapping pins and/or EEPROM
- Lane reversal
- Quality of Service (QoS) With Two Virtual Channels (VC) and Eight Traffic classes (TC)
- Non-Transparent Bridging

1.2 PEX 8508RDK Features

- PLX PEX 8508 PCI Express switch in a 296-ball PBGA package
- Form factor based on PCI Express Card Electromechanical (CEM) Specification 1.1
- Four downstream PCI Express Slot connectors
- DIP switches for hardware configuration of PEX 8508 and on-board clock circuitry
- Transparent or Non-Transparent switch support
- On-board PCI Express RefClk buffers and generator allows selection of two reference clock schemes.
- Support for Spread Spectrum Clocking (SSC) and downstream SSC isolation
- One Hot Plug controllable slot
- Socketable Serial EEPROM (3.3V)
- Standard 0.1” headers to connect up to I2C
- On-board power-on sequencing
- Manual push-button PERST# capability
- Lane Status indicator LEDs for visual inspection of link status
- Auxiliary ATX Hard disk connector for supporting additional power requirements for add-in cards
- Support for PCI Express L2 link state and wakeup mechanisms, including auxiliary power generation, and WAKE# push-button switch.

2. PEX 8508RDK Hardware Architecture

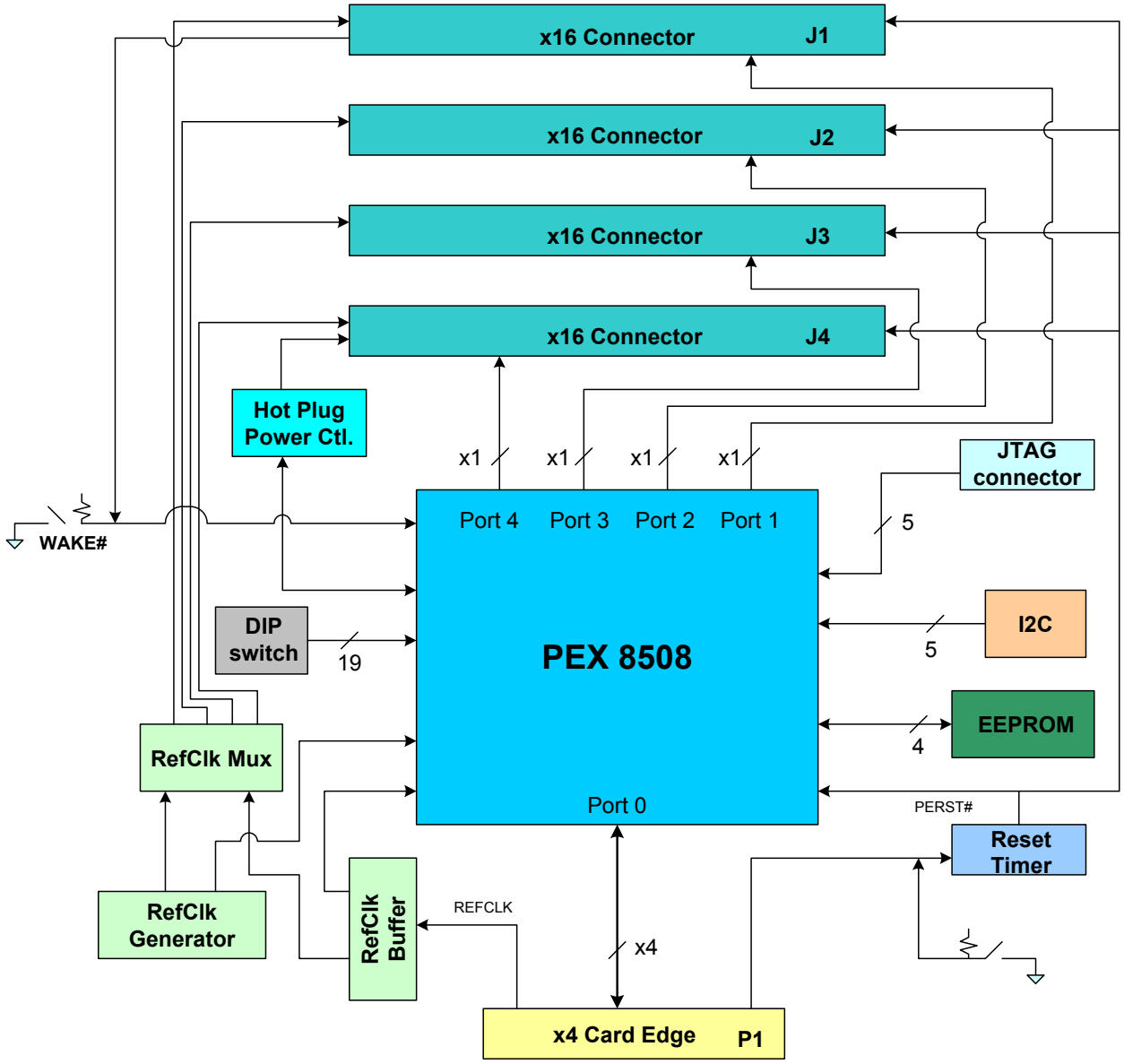

Figure 2-1. PEX 8508RDK Hardware Architecture

2.1 PEX 8508 PCI Express Switch

The PEX 8508 is an 8-lane, 5-port (maximum) PCI Express switch, which can be configured using strap pins or EEPROM. The RDK's onboard PEX 8508 is set up as a 5-port switch; with one x4 upstream port (Port 0) and four x1 downstream ports (Ports 1-4). Port 0 connects to the card edge (P1), while Ports 1, 2, 3, and 4 connect to x16-sized slot connectors (J1, J2, J3, and J4 respectively).

2.2 PCI Express Card Edge P1

The RDK form factor is based on the PCI Express CEM 1.1 specification. The board can directly plug into a PCI Express x4, x8, or x16 connector. All four lanes from the card edge connect to the PEX 8508's Port 0. The default configuration of the PEX 8508RDK set's Port 0 to be the upstream port. The card edge provides the main source of +12V and +3.3V power, along with PERST# and REFCLK_P/N.

2.3 PCI Express Slot Connectors

The PEX 8508RDK contains four PCI Express slot connectors, which connect to the downstream ports of the PEX 8508. All four connectors are x16 sized connectors, although the PEX 8508 connects less than 16-lanes to each of these four connectors. The PCI Express Card Electromechanical Specification 1.1 refers to this as down-shifting, and in general is not allowed to be implemented. The RDK does this for testing purposes only; therefore, customers designing the PEX 8508 onto a platform board should size the slot connector to match the link width of the port routing to that connector (For example, an x4 should route to an x4 slot connector). Sizing all connectors to x16 allows any PCI Express CEM form factor card (x16, x8, x4 or x1) to directly plug into the RDK without the use of adapters. The link between the PEX 8508 port and the plug-in card's port will auto-negotiate to the highest common link width.

2.3.1 PCI Express Connector J1

Connector J1 is a straddle-mount (SMT), x16 PCI Express connector. Cards plugging into this slot will be in-line with the RDK. Port 1 connects one lane (x1) to the lowest lane of connector J1. The upper fifteen lanes are unconnected. Power is provided to connector J1 from the ATX hard disk connector J5.

2.3.2 PCI Express Connector J2

Connector J2 is a vertical-mount (through-hole) x16 PCI Express connector. Cards plugging into this slot will be perpendicular to the RDK. Port 2 connects one lane (x1) to the lowest lane of connector J2. The upper fifteen lanes are unconnected. Power is provided to connector J2 from the ATX hard disk connector J5.

2.3.3 PCI Express Connector J3

Connector J1 is a vertical-mount (through-hole) x16 PCI Express connector. Cards plugging into this slot will be perpendicular to the RDK. Port 3 connects one lane (x1) to the lowest lane of connector J3. The upper fifteen lanes are unconnected. Power is provided to connector J3 from the ATX hard disk connector J5.

2.3.4 PCI Express Connector J4

Connector J4 is a vertical-mount (through-hole) x16 PCI Express connector. Cards plugging into this slot will be perpendicular to the RDK. Port 4 connects one lane (x1) to the lowest lane of connector J4. The upper fifteen lanes are unconnected. Connector J4 is implemented as a Hot Plug controlled slot, via the PEX 8508 Hot Plug controller and an Intersil power controller (see section 2.6 for more details). Power for this slot is gated by two power FETs, which will only turn-on if a card is present in the slot (HP_PRSNT[4]# and HP_MRL[4]# asserted).

2.4 Reference Clock Circuitry

The PEX 8508RDK reference clock circuitry has been designed to allow for the demonstration of two different clocking schemes supported by the PEX 8508. The first scheme utilizes a single clock domain for the entire board. In this scheme, the differential reference clock is taken from the PCIe card-edge, and

distributed to the PEX 8508's PEX_REFCLKP/N input and to all four downstream slot connectors, via U9 and U10. The second scheme utilizes two different clock domains. The card-edge reference clock is again distributed to the PEX 8508's PEX_REFCLKP/N input. The clock may or may not be a spread spectrum clock source (SSC). The second clock domain is created on-board via a reference clock generator (U8). This clock domain must be derived from a constant frequency clock (CFC) source. The CFC clock is distributed to the PEX 8508's PEX_REFCLK_CFCP/N input, and the four downstream slot connectors. In the latter scheme, downstream cards behind the switch are isolated from the spread spectrum clock source, and may optionally operate from their own local oscillators as long as they operate within +/-300ppm of the PCI Express generation 1 data rate. Selecting between the two clocking schemes is accomplished using the STRAP_SSC_XING_ENA strap signal, which is connected to SW1, pin 2.

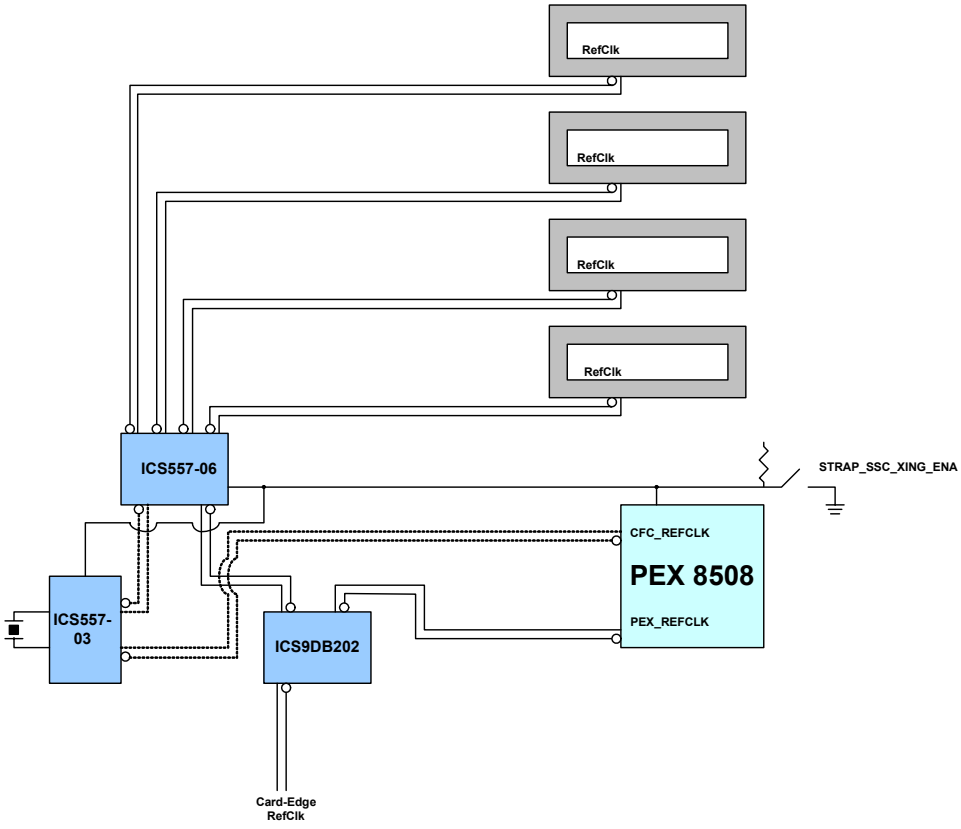

Figure 2-2. PEX 8508RDK Reference Clock Circuit

2.4.1 On-board Clock Buffer

The Integrated Circuit Systems ICS9DB202 1-to-2 PCI Express clock buffer (U10) provides on-board REFCLK distribution to the PEX 8508 and the on-board reference clock multiplexer (U9). The ICS9DB202 input is sourced by the card edge P1. The ICS9DB202 provides two differential CML (current mode logic) clock outputs. The REFCLK output pair that drives the PEX 8508's PEX_REFCLKP/N is AC-coupled (C108 and C109). This is required to block the DC information of the transmitter from the PEX 8508 clock receiver, which has on-chip biasing and termination circuitry. Both REFCLK outputs are source terminated, per PCI Express CEM 1.1 specification. Two control inputs are switch selectable on the RDK. (see section 3.1.4 for details).

2.4.2 On-Board Clock Generator

An Integrated Circuit Systems ICS557-03 PCI Express clock generator (U8) provides on-board REFCLK synthesis from a 25.000MHz source crystal (Y1). Outputs from the ICS9557-03 connect to the on-board

clock multiplexer and the PEX 8508's PEX_REFCLK_CFCP/N input. The latter is connected through AC-coupling capacitors. The ICS557-03 is used to provide a constant frequency clock source, when the RDK is setup to run on two clock domains.

2.4.3 On-Board Clock Multiplexer/Buffer

The final stage of the reference clock circuit is a two input/four output reference clock multiplexer/buffer (U9). The ICS557G-06 is used to select between two clock sources (buffered card-edge clock or on-board clock generator). The four outputs are connected to the four x16 slot connectors.

2.5 Reset Circuitry

The PEX 8508RDK reset circuitry includes a MAX6420 adjustable reset timer (U7) and manual reset push-button switch (SW5). The reset timer accepts PERST# from the card edge (P1) and from SW5 (logical-OR via U6). The MAX6420 has the capability of adjusting the reset timeout period by changing the value of C91 (0.001 µF ~= 3 ms).

2.6 Hot Plug Circuitry

Each PEX 8508 port provides a 9-pin Hot Plug controller (HPC) interface. The RDK can be enabled (via switch SW3 position 1) to allow Port 4's HPC to provide full Hot Plug hardware functionality to slot J4.

Port 4's HPC interfaces to an Intersil ISL6161 PCI Express Hot Plug power controller (U3), which is used to control and monitor +12V and +3.3V power to J4. The HPC provides an active-low power enable output (HP_PWREN[4]#), which directly enables the ISL6161 to begin ramping up the gates of Q1 and Q2 (+12V and +3.3V respectively). After both power rails are stable, the ISL6161 monitors the current being supplied on both rails via R40 and R46. If either rail exceeds its programmable current threshold (2.5A for +12V and 3.3A for +3.3V), the ISL6161 will assert HP_PWRFLT[4]# (i.e. de-assert PGOOD) to the PEX 8508's HPC, enter current regulation mode, and eventually drive the gates of Q1 and Q2 to 0V. HP_PWRFLT[4]# will remain asserted until HP_PWREN[4]# is de-asserted via software. The de-assertion of HP_PWREN[4]# will reset the ISL6161.

Attention and power indicators (D19 and D20 respectively) provide visual status regarding the state of slot J4. The attention button (HP_BUTTON[4]#) is implemented as a push-button switch SW4. The manually-operated retention latch (HP_MRL[4]#) is implemented as a DIP switch controlled input to the HPC (SW3). The PERST# signal supplied to J4 is directly controlled by the HPC (HP_PERST[4]#). By default, the Hot Plug control over slot J4 in not enabled. The user can enable Hot Plug control of power and reset to J4, by placing switch SW3, pin 1 to the OFF position.

2.7 Serial EEPROM

The PEX 8508RDK contains an 8-pin DIP socket for a serial EEPROM (U2). The board is populated with a blank Atmel AT25256A 32-Kbyte device. To use the serial EEPROM, place a shunt between pins 1 and 2 of JP2 (see section 3.4 for more details). The AT25256A device can directly interface to the PEX8508.

2.8 I2C Interface

The PEX 8508 implements an I2C slave interface, which allows an external I2C master to read and write device registers through an out-of-band mechanism. The PEX 8508 I2C interface is accessible via a 7-bit address, at data rates up to 400kbits/sec. The RDK provides two cascaded 2x2, 0.1" pitch headers (JP4 and JP5), which interface to the PEX 8508's I2C port. This allows for cascading multiple RDKs together using standard ribbon cable, or connecting various 3rd party I2C test equipment such as the Total Phase Aardvark I2C controller.

2.9 Power Distribution

2.9.1 Power Generation/Conversion

The PEX 8508RDK has two sources for DC power. The first source is the card edge connector (P1). The x4 connector provides up to 2.1A at +12V and 3.0A at +3.3V. Card edge power is intended to power only RDK board components and slot J4. Slots J1, J2 and J3 receive power via a 4-pin ATX hard disk connector (J5). Add-in cards that require more that 25W of power (such as graphics cards) should use slots J1, J2 and/or J3. These slots are power limited only by the ATX power supply that is used.

PEX8508 core and SerDes +1.0V supply is derived from the +12V rail through a non-isolated DC/DC converter (U12). The PEX 8508's +3.3V I/O supply receives power directly from the +3.3V card edge power rail. The VTT supply for the PEX8508 PCI Express transmitters, is regulated from the +3.3V card edge power via an adjustable LDO regulator (U13). The regulator output voltage is normally set to +1.50V, but can be adjusted by changing the values of R103 and R107.

The ATX 4-pin connector provides +12V and +5V DC power. The +5V is converted down to +3.3V for slots J1, J2 and J3 through a Bel S7AH-08B330 non-isolated DC/DC converter (U11). The +12V power rail is used directly.

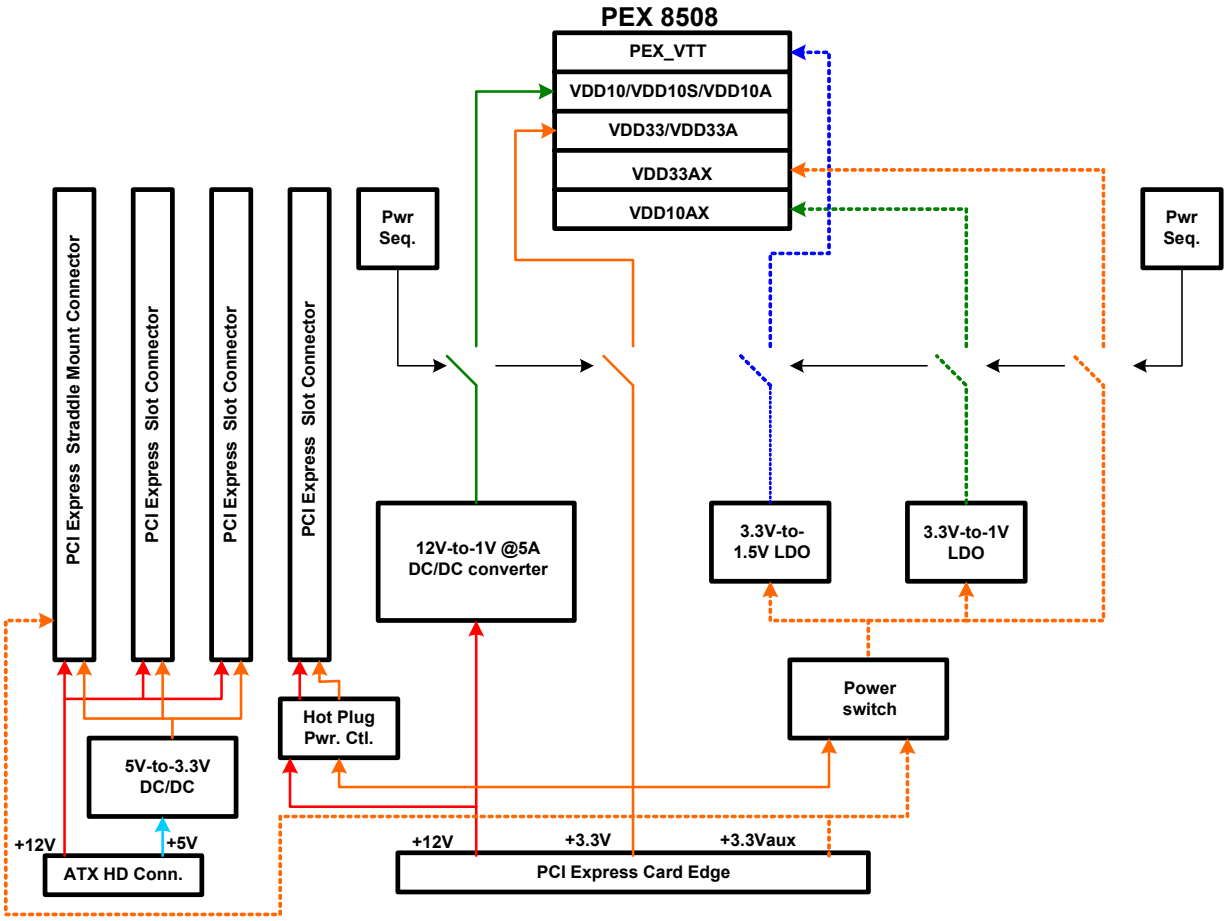

Figure 2-3. PEX 8508RDK Power Subsystem

2.9.2 PCI Express Auxiliary Power

The PEX 8508 supports the L2 link state. While in this state, main power to the chip is removed (VDD10S, VDD10A, VDD10, VDD33, and VDD33A), while VDD10X, VDD33X, and VTT_PEX continue to be powered by the systems auxiliary power rail (+3.3Vaux). The RDK uses a California Micro Devices CMPWR025 (U18) to switch the input power to the VTT_PEX regulator (U13), the VDD10X regulator (U19), and the VDD33X supply pins. While the main +3.3V rail is powered on, the auxiliary power circuits will be driven from that rail. Once the main +3,3V rail is powered down, the CMPWR025 switches to the +3.3Vaux rail and in doing so, providing uninterrupted power to the PEX 8508.

2.9.3 Power Sequencing

Two Maxim MAX6820 power supply sequencers are used for power sequencing and monitoring. The first MAX6820 (U20) monitors the main power rails (VDD_1.0V and VDD_3.3V). Once the +3.3V rail exceeds +2.125V and the +1.0V rail exceeds +0.80V, the sequencer begins to drive the gate of Q7. The MAX6820 provides a tuning capacitor for adjusting the delay from when the monitored voltages cross the detection thresholds to the gate turn-on time. The board's power sequencing is designed to allow +1.0V to power-on, followed by +3.3V.

The second power sequencer (U17) is used to sequence the three auxiliary power rails (VDD_VTT, VDDAUXIO_3.3V and VDDAUX_1.0V). This sequencer is used to drive the gates of Q5 and Q6, providing a power-on sequence of +1.0V, followed by VTT and +3.3V.

2.10 LED Indicators

The PEX 8508RDK provides a number of LED indicators including power-on indication, PEX 8508 lane status indication, and Hot Plug status indication. Table 2-1 provides a quick explanation of the various board indicators.

Table 2-1. PEX 8508RDK LED Indicator descriptions

Indicator Type	Locations	LED On	LED Off
Main Board/ PEX8508 Power indication	D21, D22, D24, D25	1.0V, 1.5V, 12V, 3.3V power on	1.0V, 1.5V, 12V, 3.3V power off
Aux Power Indication	D7	+3.3Vaux power is on	+3.3Vaux power is off
Slot J1/J2/J3 indication	D26, D27	+3.3V and +12V power on	+3.3V and +12V power off
Slot J1/J2/J3 Power Fault	D23	+12V or +3.3V power to slots J1/J2/J3 had dropped below -15% on either supply.	+12V and +3.3V power to slots J1/J2/J3 is good.
Slot J4 Power indication	D17, D18	Slot J4 +12V and +3.3V power on	Slot J4 +12V and +3.3V power off
PEX 8508 Port 0 Lane Status	D1, D5, D9, D13	Port 0 link is up and lane n is active	If all LEDs off, Port 0 link is down
PEX 8508 Port 1 Lane Status	D2	Port 1 link is up	Port 1 link is down
PEX 8508 Port 2 Lane Status	D3	Port 2 link is up	Port 2 link is down
PEX 8508 Port 3 Lane Status	D4	Port 3 link is up	Port 3 link is down
PEX 8508 Port 4 Lane Status	D12	Port 4 link is up	Port 4 link is down
PEX 8508 Fatal Error Indication	D6	PEX 8508 detected a fatal error.	No fatal errors reported
Hot Plug Attention indication	D20	**On:** Operation problem **Blinking:** Slot is being identified at user's request	Normal operation
Hot Plug Power indication	D19	**On:** Slot is powered on **Blinking:** Slot is being powered up or powered down	Slot power indication is off

3. On-Board Connectors, Switches, and Jumpers

3.1 DIP Switches

The PEX 8508RDK contains five user controllable DIP switches (SW1, SW2, SW3, SW6 and SW7) for selecting various functionality. Each DIP switch position can be either ON (0b) or OFF (1b). The gray squares in Figures 3-1 through 3-5 indicate which way the switch position is connected.

3.1.1 Upstream Port and Mode Selection (SW1)

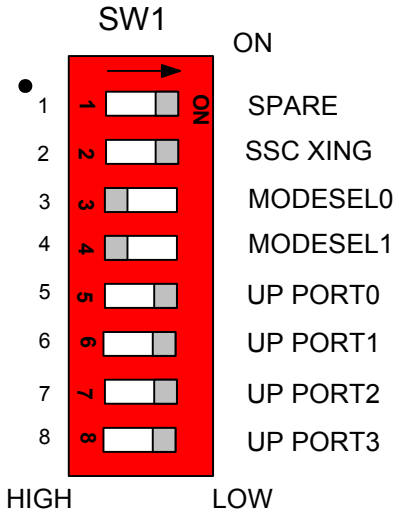

Figure 3-1. Switch SW1 Default Settings

Table 3-1. Switch SW1 Description

SW1 Functional Description	Switch Position Settings
Spare Switch. Extra DIP switch for general purpose use. Connects to TPV19. Default setting 0b.	1: SPARE Value: 0b – Switch closed; 1b – Switch opened.
STRAP_SSC_XING_ENA Selects PEX 8508's clocking scheme. Default setting is 0b.	2: STRAP_SSC_XING_ENA Value: 0b – Single clock domain for all ports.; 1b – Dual clock domain for upstream port.
STRAP_MODE_SEL[1:0] Selects PEX 8508 Operating Mode. Default setting is 11b.	3: STRAP_MODE_SEL[0] 4: STRAP_MODE_SEL[1] Bus Encodings [1:0] / PEX 8508 Operating Mode: 00b – Reserved 01b – NT Intelligent Adapter Mode 10b – NT Dual Host Mode 11b – Transparent Mode
STRAP_UPSTRM_PORTSEL [3:0] Selects the PEX 8508 Upstream Port. Default setting is 0000b.	5: STRAP_UPSTRM_PORTSEL[0] 6: STRAP_UPSTRM_PORTSEL[1] 7: STRAP_UPSTRM_PORTSEL[2] 8: STRAP_UPSTRM_PORTSEL[3] Bus Encodings [3:0] / Upstream Port: 0000b – 0 0001b – 1 0010b – 2

SW1 Functional Description	Switch Position Settings	
	0011b	3
	0100b	4
	0101b-1111b	Reserved

3.1.2 Port Configuration, NT Port Selection, and Slot J3 control (SW2)

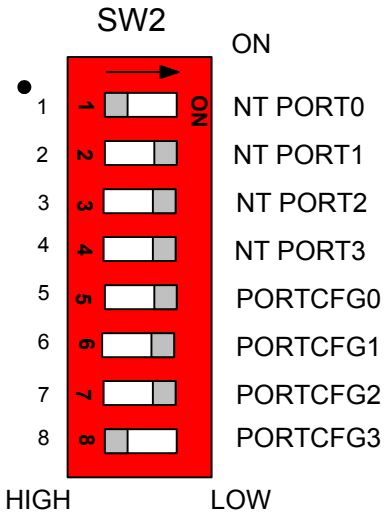

Figure 3-2. Switch SW2 Default Settings

Table 3-2. Switch SW2 Description

<table>
<tr><th>SW2 Functional Description</th><th>Switch Position Settings</th></tr>
<tr><td>STRAP_NT_UPSTRM_PORTSEL[3:0]
Selects PEX 8508 NT Port depending on STRAP_MODE_SEL[1:0] settings.
Default Setting is 0001b.</td><td>1: STRAP_NT_UPSTRM_PORTSEL[0]
2: STRAP_NT_UPSTRM_PORTSEL[1]
3: STRAP_NT_UPSTRM_PORTSEL[2]
4: STRAP_NT_UPSTRM_PORTSEL[3]
<table><tr><th>Bus Encodings [3:0]</th><th>NT Port</th></tr><tr><td>0000b</td><td>0</td></tr><tr><td>0001b</td><td>1</td></tr><tr><td>0010b</td><td>2</td></tr><tr><td>0011b</td><td>3</td></tr><tr><td>0100b</td><td>4</td></tr><tr><td>0101b-1111b</td><td>Reserved</td></tr></table></td></tr>
<tr><td>STRAP_STN_PORTCFG[3:0]
Selects PEX 8508 Port Configuration
Default Setting is 1000b.</td><td>5: STRAP_STN_PORTCFG[0]
6: STRAP_STN_PORTCFG[1]
7: STRAP_STN_PORTCFG[2]
8: STRAP_STN_PORTCFG[3]
<table><tr><th>Bus Encodings [3:0]</th><th>Port Configuration</th></tr><tr><td>0000b</td><td>X2,x2,x2,x2,x0</td></tr><tr><td>0010b</td><td>X4,x4,x0,x0,x0</td></tr><tr><td>0011b</td><td>X4,x2,x2,x0,x0</td></tr><tr><td>0100b</td><td>X4,x2,x1,x1,x0</td></tr><tr><td>0101b</td><td>X4,x1,x1,x2,x0</td></tr><tr><td>0110b</td><td>X4,x1,x2,x1,x0</td></tr><tr><td>0111b</td><td>X2,x2,x2,x2,x0</td></tr><tr><td>1000b</td><td>X4,x1,x1,x1,x1</td></tr><tr><td>1001b</td><td>X2,x2,x2,x1,x1</td></tr><tr><td>All other combinations</td><td>X2,x2,x2,x2,x0</td></tr></table></td></tr>
</table>

3.1.3 Hot Plug Controller (SW3)

Switch SW3 is used for Hot Plug control. Table 3-3 defines the functions associated with each position on the switch.

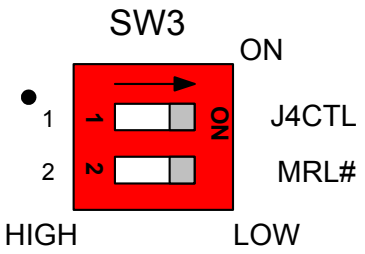

Figure 3-3. Switch SW3 Default Settings

Table 3-3. Switch SW3 Description

SW3 Functional Description	Switch Position Settings
Slot J4 Hot Plug Control. Allows the user to select whether slot J4 is controlled via the PEX 8508 Hot Plug controller or normal board power-up sequencing. Default Setting is 0b.	1: J4CTL **Value** / **Function** 0b – J4 is not Hot Plug controlled. 1b – J4 is controlled via Hot Plug
Hot Plug MRL[4]#. Used to simulate MRL sensor behavior. Default setting is 0b.	2: HP_MRL[4]# **Value** / **Function** 0b – Latch closed 1b – Latch open

3.1.4 Clock Generator and Buffer Control (SW6)

Switch SW6 is used to generate controls for the on-board RefClk clock buffer (ICS9DB202).

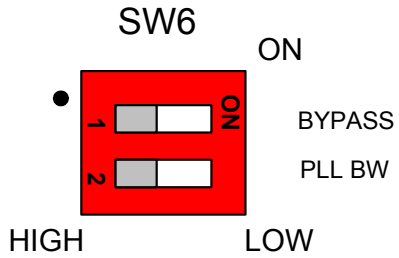

Figure 3-4. Switch SW6 Default Settings

Table 3-4. Switch SW6 Description

<table>
<tr><th>SW6 Functional Description</th><th>Switch Position Settings</th></tr>
<tr><td>BYPASS selects whether U10 operates as a fanout buffer (PLL bypassed) or as a zero delay buffer (PLL active). Default setting is 1b.</td><td>1: BYPASS
<table><tr><th>Value</th><th>Xtal Frequency</th></tr><tr><td>0b</td><td>PLL Enabled</td></tr><tr><td>1b</td><td>PLL Bypassed</td></tr></table></td></tr>
<tr><td>PLL BW selects between one of two PLL loop bandwidths. Default setting is 1b.</td><td>2: PLL BW
<table><tr><th>Value</th><th>Xtal Frequency</th></tr><tr><td>0b</td><td>BW = 500 kHz</td></tr><tr><td>1b</td><td>BW = 1 MHz</td></tr></table></td></tr>
</table>

3.1.5 PEX 8508 I2C Address Selection (SW7)

Switch SW7 is used to select the lower three address bits of the PEX 8508's I2C slave address.

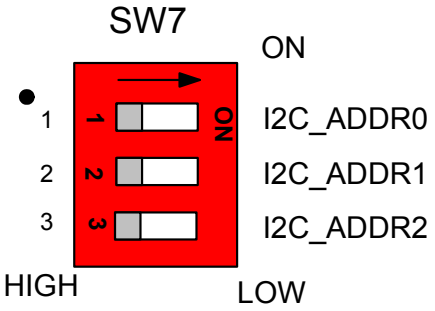

Figure 3-5. Switch SW7 Default Settings

Table 3-5. Switch SW7 Description

<table>
<tr><th>SW7 Functional Description</th><th>Switch Position Settings</th></tr>
<tr><td>PEX 8508 I2C Address bits[2:0]. Default setting is 111b.</td><td>1: I2C_ADDR[0]
2: I2C_ADDR[1]
3: I2C_ADDR[2]
<table><tr><th>Bus Encodings [1:0]</th><th>PEX 8508 I2C Slave Address</th></tr><tr><td>000b</td><td>70h</td></tr><tr><td>001b</td><td>71h</td></tr><tr><td>010b</td><td>72h</td></tr><tr><td>011b</td><td>73h</td></tr><tr><td>100b</td><td>74h</td></tr><tr><td>101b</td><td>75h</td></tr><tr><td>110b</td><td>76h</td></tr><tr><td>111b</td><td>77h</td></tr></table></td></tr>
</table>

3.2 Push-Button Switches

3.2.1 Hot Plug Attention Button# (SW4)

Switch SW4 provides a push-button switch control for the PEX 8508 Hot Plug Controller's HP_BUTTON[4]# input pin. The PEX 8508 contains internal debounce circuitry for this input.

3.2.2 Manual Reset# (SW5)

The PEX 8508 RDK provides a manual PERST# capability. Note that manual PERST# will only apply warm reset to the PEX 8508, and slots J1, J2, J3, and J4 (not P1).

3.2.3 WAKE# (SW8)

The RDK supports placing the PEX 8508 into the L2 link state, and provides a means for generating a wakeup mechanism from this state. SW8 is connected as a wire-OR with the WAKE# pin from slot J1. This signal connects to the PEX 8508 WAKE# input. When the PEX 8508 is in the L2 link state (i.e. auxiliary power is applied, and PERST# is asserted) pushing SW8 will cause a low pulse on the PEX 8508 WAKE# signal. The PEX 8508 will then generate a Beacon signal from lane 0 of the upstream port.

3.3 EEPROM Present Jumper (JP2)

JP1 is used to provide an EEPROM presence detection signal (EE_PR#) to the PEX 8508. Install a shunt between pins 1 - 2 to indicate a Serial EEPROM is present. Un-install the shunt to indicate a Serial EEPROM is not present.

Table 3-6. Jumper JP2 settings

JP1 Setting	EEPROM Status
Shunt installed	Serial EEPROM present
Shunt not installed	Serial EEPROM not present

3.4 JTAG Header (JP1)

Header JP1 provides a direct connection to the PEX 8508 JTAG interface. The 10-pin connector is designed to allow a direct interface to 3rd party JTAG controllers, such as the Corelis USB-1149.1/E controller.

3.5 Non-Transparent Mode Reset (TPV11)

Test point via TPV11 provides a location for accessing the PEX_NT_RESET# pin of the PEX 8508. This signal can be used to propagate reset from the host address domain to the local address domain.

3.6 PCI Express Fatal Error Indication (D6)

The PEX 8508 provides an output status pin (FATAL_ERR#), which reports the event of a PCI Express fatal error condition. The RDK connects this output to D6, which is lit when a fatal error is detected. Examples of fatal error conditions are data link layer protocol errors, receiver overflow, malformed TLPs, etc… The PCI Express Base specification provides a complete listing of fatal error conditions.

3.7 Slots J1/J2/J3 Power Fault Indication (D23)

Slots J1, J2, and J3 are power by the ATX 4-pin hard disk connector and a DC/DC converter (U11). No circuitry is provided to current limit the power consumed by those three slots; however, a voltage supervisor is provided to monitor under-voltage conditions on the +12V and +3.3V supply rails going to those slots. If either rail drops below 15% of its nominal supply voltage, the power good signal from U15 is used to clear a D-flip flop (U14), which will in turn light a red indicator LED (D23). Once the LED is lit, it remains lit until board power is cycled.

4. Serial EEPROM Registers

4.1 Serial EEPROM Contents

The PEX 8508RDK is shipped with a programmed AT25256A EEPROM. PLX Technology provides the necessary binary image files and software tools required to program the EEPROM. Install a jumper between JP2 pins 1 and 2, before applying power to the RDK.

5. Bill of Materials/ Schematics

Item #	Qty	Man	Man's Part #	Des	Package Type	Comp Des(s)	Subcon. Part #
SURFACE MOUNT COMPONENTS							
1	1	PLX Technology	PEX8508-AC25BI	IC, 8-lane, 5-port, PCI Express switch	SMT, 296-pin PBGA	U1	
2	1	Intersil	ISL6161CB	IC, Dual-power Hot Plug Controller	SMT, 14-lead SOIC	U3	
3	2	Maxim	MAX6820UT-T	IC, Power Sequencer	SMT, 6-pin SOT-23	U17, U20	
4	1	Intersil	ISL6536IB	IC, Four Channel Supervisor	SMT, 8-pin SOIC	U15	
5	1	ICS	ICS557G-03	IC, PCI Express Clock Generator	SMT, 16-pin TSSOP	U8	
6	1	ICS	ICS557G-06	IC, PCI Express Clock Mux/Buffer	SMT, 20-pin TSSOP	U9	
7	1	ICS	ICS9DB202CG	IC, PCI Express Clock Buffer	SMT, 20-pin TSSOP	U10	
8	1	Maxim	MAX6420UK29-T	IC, Reset controller, Adj. reset timeout	SMT, SOT23-5	U7	
9	1	Belfuse	S7AH-08B330	Non-iso DC/DC converter, 5V-to-3.3V @ 8A	SMT, 7-pin	U11	
10	1	Belfuse	S7AH-05A1AF	Non-iso DC/DC converter, 12V-to-1V, Wide trim, @ 5A. Fast turn-on	SMT, 7-pin	U12	
11	1	California Micro Devices	CMPWR025M	Dual-input, Power switch	SMT, 8-pin MSOP	U18	
12	2	Maxim	MAX1806EUA15	LDO regulator, 500mA adjustable	SMT, 8-pin uMax	U13, U19	
13	2	TI	SN74LVC1G3157DCKR	1-bit, SPDT Analog switch	SMT, 6-pin SC-70	U4, U5	
14	2	Fairchild	NC7S04M5X	IC, Tiny Logic Inverter	SMT, 5-pin SOT-23	U16	
15	1	Fairchild	NC7S08M5X	IC, Tiny Logic 2-input AND gate	SMT, 5-pin SOT-23	U6	
16	1	TI	SN74LVC2G74DCTR	IC, Single Positive Edge D Flip flop	SMT, 8-pin SSOP	U14	
17	1	Adex	CONN-PCIEXP-16X-SM	PCI Express x16 straddle-mount connector	SMT, 164-pin	J1	
18	2	International Rectifier	IRF7470	IC, N-Channel MOSFET	SMT, 8-pin, SO-8	Q1, Q2	
19	2	On Semiconductor	MMBT3904LT1	IC, Bipolar Transistor	SMT, SOT-23	Q3, Q4	Digikey P/N: MMBT3904LT1OSCT-ND
20	3	Fairchild Semiconductor	FDN339AN	IC, N-Channel MOSFET	SMT, 3-pin SOT-23	Q5, Q6, Q7	
21	1	Lumex	SML-LXT0805YW-TR	LED, Yellow	SMT, 0805	D20	Digikey P/N: 67-1554-1-ND
22	10	Lumex	SML-LXT0805GW-TR	LED, Green	SMT, 0805	D7, D17, D18, D19, D21, D22, D24, D25, D27,	Digikey P/N: 67-1553-1-ND

Item #	Qty	Man	Man's Part #	Des	Package Type	Comp Des(s)	Subcon. Part #
						D28	
23	2	Lumex	SML-LX0603IW-TR	LED, Red	SMT, 0603	D6, D23	Digikey P/N: 67-1548-1-ND
24	8	Lumex	SML-LX0603GW-TR	LED, Green	SMT, 0603	D1, D2, D3, D4, D5, D9, D12, D13	Digikey P/N: 67-1549-1-ND
25	1	ITTCANNON	TDA02H0SK1	Dip Switch, 2-pos, half pitch, tape seal	SMT	SW6	Digikey P/N: CKN1362-ND
26	1	ITTCANNON	SDA02H1SKD	Dip Switch, 2-pos, half pitch, tape seal	SMT	SW3	Digikey P/N: CKN1286-ND
27	1	ITTCANNON	SDA03H1SKD	Dip Switch, 3-pos, half pitch, tape seal	SMT	SW7	Digikey P/N: CKN1287-ND
28	2	ITTCANNON	SDA08H1SKD	Dip Switch, 8-pos, half pitch, tape seal	SMT	SW1, SW2	Digikey P/N: CKN1292-ND
29	3	Omron	B3S1002	Switch, Push Button	SMT	SW4, SW5, SW8	Digikey P/N: SW416-ND
30	9	CTS	742C083512J	Chip Res. Array, 5.1K ohm, 4R isolated	SMT	RN1, RN3, RN4, RN5, RN6, RN7, RN8, RN9, RN10	Digikey P/N: 742C083512JCT-ND
31	17	Panasonic	ERJ-3GEY0R00V	Res. 1/10W, zero ohm 5%	SMT, 0603	R10, R19, R20, R21, R22, R23, R26, R31, R32, R44, R51, R55, R57,R107, R120, R121, R124, R134	Digikey P/N: P0.0GCT-ND
32	4	Panasonic	ERJ-6GEY0R00V	Res. 1/8W, zero ohm 5%	SMT, 0805	R1, R12, R130, R132	Digikey P/N: P0.0ACT-ND
33	1	TTelectronics	LR2512-01-R030-F	Res. 2W, 0.03 ohm 1%	SMT, 2512	R46	Mouser P/N: 66-LR2512-01-R030-F
34	1	TTelectronics	LR2512-01-R040-F	Res. 2W, 0.04 ohm 1%	SMT, 2512	R40	Mouser P/N: 66-LR2512-01-R040-F
35	2	Panasonic	ERJ-6RQJ4R7V	Res. 1/8W, 4.7 ohm 5%	SMT, 0805	R58, R80	Digikey P/N: P4.7DCT-ND
36	19	Panasonic	ERJ-2GEJ330X	Res. 1/16W, 33 ohm 5%	SMT, 0402	R9, R41, R45, R59, R60, R63, R64, R65, R66, R72, R73, R78, R79, R84, R85, R86, R88, R92, R93	Digikey P/N: P33JCT-ND
37	16	Panasonic	ERJ-2RKF49R9X	Res. 1/16W, 49.9 ohm 1%	SMT, 0402	R61, R62, R67, R68, R69, R70, R74, R75, R81, R83, R87, R89, R91, R94, R95, R127	Digikey P/N: P49.9LCT-ND
38	18	Panasonic	ERJ-3GEYJ151V	Res. 1/10W, 150 ohm 5%	SMT, 0603	R3, R4, R5, R6, R7, R11, R14, R15, R18, R39, R49, R50, R108, R109, R110, R112, R133, R137	Digikey P/N: P150GCT-ND

Item #	Qty	Man	Man's Part #	Des	Package Type	Comp Des(s)	Subcon. Part #
39	3	Panasonic	ERJ-3EKF4750V	Res. 1/16W, 475 ohm 1%	SMT, 0603	R71, R82, R96	Digikey P/N: P475HCT-ND
40	2	Panasonic	ERJ-3EKF1001V	Res. 1/16W, 1K ohm 1%	SMT, 0603	R38, R111	Digikey P/N: P1.00KHCT-ND
41	4	Panasonic	ERJ-3EKF2261V	Res. 1/16W, 2.26K ohm 1%	SMT, 0603	R29, R30, R123, R136	Digikey P/N: P2.26KHCT-ND
42	3	Panasonic	ERJ-3EKF2741V	Res. 1/16W, 2.74K ohm 1%	SMT, 0603	R90, R116, R125	Digikey P/N: P2.74KHCT-ND
43	19	Yageo America	9C06031A5101FKHFT	Res. 1/10W, 5.1K ohm 1%	SMT, 0603	R2, R13, R16, R25, R34, R35, R36, R37, R43, R47, R48, R52, R76, R77, R97, R98, R99, R102, R122	Digikey P/N: 331-5.10KHCT-ND
44	1	Panasonic	ERJ-3EKF7681V	Res. 1/16W, 7.68K ohm 1%	SMT, 0603	R115	Digikey P/N: P7.68KHCT-ND
45	3	Panasonic	ERJ-3EKF8251V	Res. 1/10W, 8.25K ohm 1%	SMT, 0603	R117, R126, R135	Digikey P/N: P8.25KHCT-ND
46	5	Panasonic	ERJ-3GEYJ103V	Res. 1/10W, 10K ohm 5%	SMT, 0603	R24, R42, R54, R113, R118	Digikey P/N: P10KGCT-ND
47	1	Yageo America	RC0603FR-0716KL	Res. 1/10W, 16K ohm 1%	SMT, 0603	R28	Digikey P/N: 311-16.0KHRCT-ND
48	1	Yageo America	9C08052A2202FKHFT	Res. 1/8W, 22K ohm 1%	SMT, 0805	R106	Digikey P/N: 311-22.0KCCT-ND
49	3	Yageo America	RC0603FR-0751KL	Res. 1/10W, 51.0K ohm 1%	SMT, 0603	R33, R53, R56	Digikey P/N: 311-51.0KHRCT-ND
50		Yageo America	9C06031A7502FKHFT	Res. 1/10W, 75k ohm 1%	SMT, 0603	R114	Digikey P/N: 311-75.0KHCT-ND
51	2	Panasonic	ERJ-3GEYJ104V	Res. 1/10W, 100k ohm 5%	SMT, 0603	R27, R105	Digikey P/N: P100KGCT-ND
52	1	Littlefuse	0429 007.WRM	Fuse, Very fast acting, 7A	SMT, 1206	F2	Digikey P/N: F1276CT-ND
53	1	Littlefuse	0429 005.WRM	Fuse, Very fast acting, 5A	SMT, 1206	F1	Digikey P/N: F1275CT-ND
54	3	Kemet	C0603C102J5RACTU	Cap. Ceramic, 0.001uF, X7R, 50V 5%	SMT, 0603	C67, C91, C127	Digikey P/N: 399-1083-1-ND
55	15	Kemet	C0402C103K3RACTU	Cap. Ceramic, 0.01uF, X7R, 25V 10%	SMT, 0402	C32, C33, C34, C35, C55, C56, C92, C93, C99, C100, C102, C103, C104, C105, C106	Digikey P/N: 399-1278-1-ND

Item #	Qty	Man	Man's Part #	Des	Package Type	Comp Des(s)	Subcon. Part #
56	6	Kemet	C0603C103 K5RACTU	Cap. Ceramic, 0.01uF, X7R, 50V 20%	SMT, 0603	C86, C89, C96, C97, C108, C109	Digikey P/N: 399-1091-1-ND
57	4	AVX Corporation	0402YC223 KAT2A	Cap. Ceramic, 0.022uF, X7R, 16V 10%	SMT, 0402	C36, C37, C38, C39	Digikey P/N: 478-1118-1-ND
58	35	Kemet	C0402C104 K8PACTU	Cap. Ceramic, 0.1uF, X5R, 10V 10%	SMT, 0402	C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C26, C27, C28, C29, C30, C31, C40, C41, C42, C43, C45, C47, C48, C49, C50, C51, C53, C54	Digikey P/N: 399-3027-1-ND
59	10	Kemet	C0603C104 K3RACTU	Cap. Ceramic, 0.1uF, X7R, 25V 10%	SMT, 0603	C59, C61, C63, C66, C85, C87, C88, C90, C120, C126	Digikey P/N: 399-1281-1-ND
60	2	Panasonic	ECJ-1VB1C105K	Cap. Ceramic, 1uF, X5R, 16V 10%	SMT, 0603	C24, C25	Digikey P/N: PCC2224CT-ND
61	8	Kemet	C0805C105 K4RACTU	Cap. Ceramic, 1uF, X7R, 16V 20%	SMT, 0805	C64, C112, C114, C115, C117, C118, C121, C125	Digikey P/N: 399-1284-1-ND
62	18	Panasonic	ECJ-3YB1C106M	Cap. MLCC , 10uF, X5R, 16V 20%	SMT, 1206	C20, C21, C22, C23, C44, C46, C52, C57, C58, C60, C62, C65, C94, C101, C107, C113, C119, C124	Digikey P/N: PCC2227TR-ND
63	1	Panasonic	ECJ-3YB0J226M	Cap. MLCC , 22uF, X5R, 6.3V 20%	SMT, 1206	C123	Digikey P/N: PCC2242CT-ND
64	12	AVX Corporation	TAJB226K020R	Cap. Tantalum, 22uF, 20V 20%	SMT, B-case	C1, C2, C77, C78, C79, C80, C81, C82, C83, C84, C110, C116	Digikey P/N: 478-1683-1-ND
THROUGH-HOLE COMPONENTS							
100	2	Molex	87715-3302	PCI Express x16 Through-hole connector	TH, 164-pin	J2. J3, J4	
101	1	AMP	103185-2	Header, 1x2, 100mil	TH, 2-pin	JP2	
102	1	AMP	103185-3	Header, 1x3, 100mil	TH, 3-pin	JP7	
103	2	AMP	103240-2	Header, 2x2, 100mil	TH, 4-pin	JP4. JP5	
104	1	AMP	103240-5	Header, 2x5, 100mil	TH, 10-pin	JP1	
105	1	AMP	103240-4	Header, 2x4, 100mil	TH, 8-pin	JP3	
106	1	AMP	103185-2	Header, 1x2 seperated as two Header Posts	TH, 1-pin	JP8, JP12	
107	1	Molex	53113-0410	Connector, ATX Hard Disk, 4-pin	TH, 4-pin	J5	
108	1	Samtec	ICA-308-S-TT	Socket, 8-pin DIP, 300 mil	TH, 8-pin DIP	U2	

Item #	Qty	Man	Man's Part #	Des	Package Type	Comp Des(s)	Subcon. Part #
109	1	Ecliptek	EC2E-16-25.000M	Crystal, HC-49/US, 25.000MHz, fundamental, 16pF load capacitance, +/-30ppm	TH, 2-pin	Y1	
110	2	Vishay	94SP187X0 016EBP	Cap. Oscon, 180uF, 16V	TH, 2-pin	C111, C122	
MANUALLY INSERTED COMPONENTS							
200	1	Atmel	AT25256A-10PI-2.7	SPI Serial EEPROM	8-lead PDIP	U2	
201	1	Keystone Electronics	9203	PCI bracket w/ two tabs			Mouser P/N: 534-9203
202	2	Building Fasteners	PMSSS 440 0025 PH	Phillips Panhead screw, 4-40 thread, 0.25"			Digikey P/N: H703-ND
203	2	Amp/Tyco	382811-6	Jumpers		JP2, JP7	Digikey P/N: A26227-ND
MISCELLANEOUS COMPONENTS							
300	1	PLX	90-0048-000-A	PEX8508RDK Bare Board rev 000			
PART THAT SHOULD NOT BE ASSEMBLED							
	1	Yageo America	9C06031A5 101FKHFT	Res. 1/10W, 5.1K ohm 1%	SMT, 0603	R17	
	3	Panasonic	ERJ-3GEY0R00V	Res. 1/10W, zero ohm 5%	SMT, 0603	R8, R128, R129	
	2	Panasonic	ERJ-3GEYJ103V	Res. 1/10W, 10K ohm 5%	SMT, 0603	R119, R131	
	3	Littlefuse	0429 005.WRM	Fuse, Very fast acting, 5A	SMT, 1206	F3, F4, F7	
	2	Littlefuse	0433 001	Fuse, Very fast acting, 1A	SMT, 1206	F5, F6	
	1	AMP	103185-3	Header, 1x3, 100mil	TH, 3-pin		
	3			Resistor, Value not specified	SMT, 0805	R100, R101, R104	
	1			Resistor, Value not specified	SMT, 0603	R103	
	2	Murata	GRM1885C 1H160JA01 D	Cap. Ceramic, 16pF, C0G, 50V 5%	SMT, 0603	C95, C98	Digikey P/N: 490-1408-1-ND
	4	AMP	103185-2	Header, 1x2, 100mil	TH, 1-pin	JP6, JP9, JP10, JP11	
SECOND SOURCE / ALTERNATIVE PARTS							
17	1	TwinHunter	TW-164PL	PCI Express x16 straddle-mount connector	SMT, 164-pin		
18	6	ST Microelectronics	STS12NH3LL	IC, N-Channel MOSFET	SMT, 8-pin, SO-8		
19	2	Infineon Tech.	SMBT3904E 6327	IC, Bipolar Transistor	SMT, SOT-23		Digikey P/N: SMBT3904INCT-ND
53	1	Littlefuse	0433 005	Fuse, Very fast acting, 5A	SMT, 1206		
107	1	AMP	SD-53113-0410	Connector, ATX Hard Disk, 4-pin	TH, 4-pin		
109	1	Citizens America Corp.	HC49US25.000000MABI	Crystal, HC-49/US, 25.000MHz, fundamental, 16pF	TH, 2-pin		

Item #	Qty	Man	Man's Part #	Des	Package Type	Comp Des(s)	Subcon. Part #
				load capacitance, +/-30ppm			
Customer Name: PLX							
PLX Part #: 91-0048-007-A							
Product Name: PEX8508RDK							

PEX 8508RDK

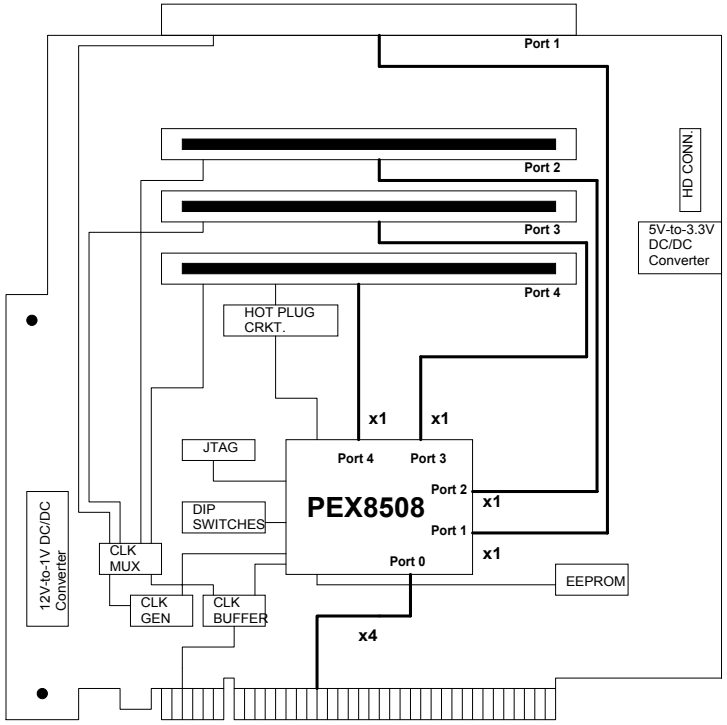

TABLE OF CONTENTS

NOTE: NL INDICATES COMPONENT NOT LOADED

Revision History

Rev#	Date	Changes from last revision
000	08/16/2005	Initial Revision
001	12/05/2005	Incorporated feedback from design review.
002	12/06/2005	Added ball K3 (VSS) to PEX8508 symbol.
003	12/09/2005	Added D26, D27, R136, R137.
004	1/24/2006	PEX8508 symbol update, and BOM fixes. Changed C95 and C98 to NL.
005	4/24/2006	PEX8508 symbol update.
006	11/7/2006	PEX8508 updated to rev AB.
007	03/29/2007	PEX8508 updated to rev AC.

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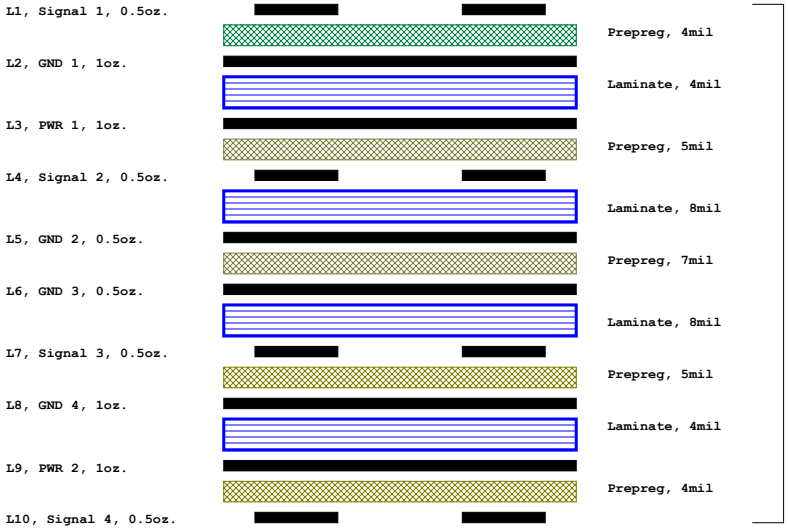
Title	PEX8508RDK - Functional Block Diagram	
Size: C	Document Number: 91-0048-007-A	Rev: 007
Date: Thursday, March 29, 2007	Sheet 1 of 10	



L3, PWR 1 IS A SPLIT PLANE USED FOR VDD_1V AND VDDEARLY_1V

L9, PWR 2 IS SPLIT BETWEEN VDD_12V, VDDEARLY_12, VDD_3.3V, VDDEARLY_3.3V, VDD_VTT, VDDEARLY_VTT, VDDHD_12V, AND VDDHD_3.3V

Material	Thickness	Dielectric Constant	Layer#	Description	Weight/Thickness
			1	TOP - SIGNAL + COMPONENTS	1/2 oz, .0022
FR4	0.004	4.3	2	GROUND PLANE	1 oz, .0013
FR4	0.004	4.3	3	POWER PLANE	1 oz, .0013
FR4	0.005	4.3	4	SIGNAL	1/2 oz, .0007
FR4	0.008	4.3	5	GROUND PLANE	1/2 oz, .0007
FR4	0.007	4.3	6	GROUND PLANE	1/2 oz, .0007
FR4	0.008	4.3	7	SIGNAL	1/2 oz, .0007
FR4	0.005	4.3	8	GROUND PLANE	1 oz, .0013
FR4	0.004	4.3	9	POWER PLANE	1 oz, .0013
FR4	0.004	4.3	10	BOTTOM - SIGNAL + COMPONENTS	1/2 oz, .0022

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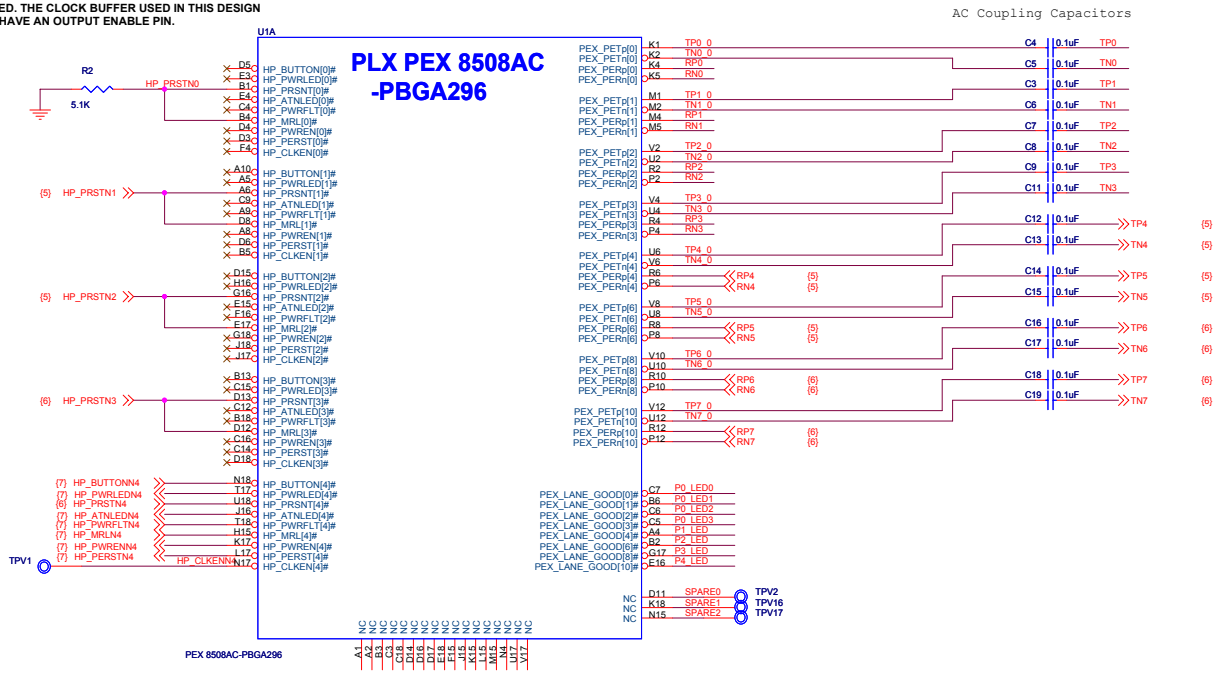
Title: PEX8508RDK - Board Layout Information

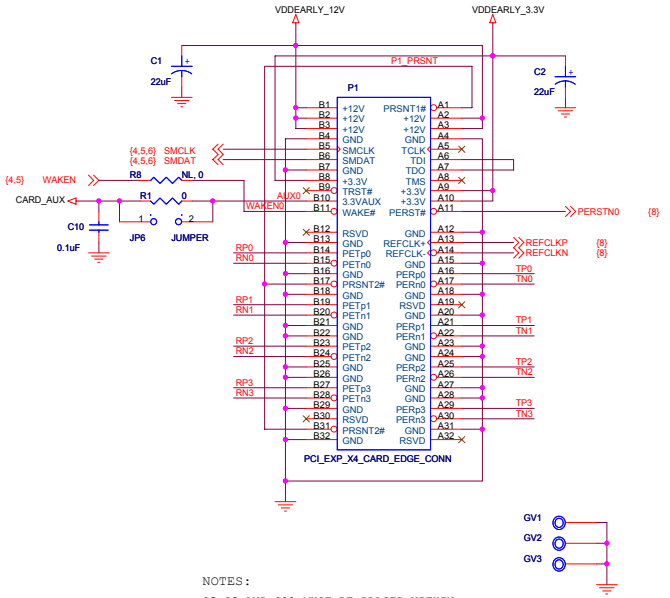
Size: C | Document Number: 91-0048-007-A | Rev: 007

Date: Thursday, March 29, 2007 | Sheet 2 of 10

NOTE: HP_PRSNT[1:3]# AND HP_MRL[1:3]# ARE CONNECTED TO SLOTS J1-J3 FOR TESTING PURPOSES. IF A HOT PLUG PORT IS UNUSED, THESE SIGNALS MAY BE LEFT UNCONNECTED..

NOTE: HP_CLKEN[N]# SHOULD BE USED DISABLE A CLOCK BUFFER OUTPUT TO A PARTICULAR SLOT WHEN DEASSERTED. THE CLOCK BUFFER USED IN THIS DESIGN DOES NOT HAVE AN OUTPUT ENABLE PIN.





NOTES:

C3-C9 AND C11 MUST BE PLACED WITHIN 250MIL FROM P1 ON SOLDER SIDE

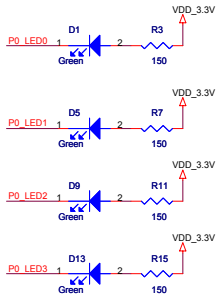
PLACE GV1-GV3 NEAR P1.

C12-C13 MUST BE PLACED WITHIN 400MIL FROM J1 ON COMPONENT SIDE

C14-C15 MUST BE PLACED WITHIN 400MIL FROM J2 ON COMPONENT SIDE

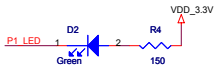
C16-C17 MUST BE PLACED WITHIN 400MIL FROM J3 ON COMPONENT SIDE

PORT 0 LANE STATUS INDICATORS

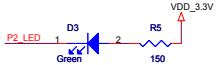


PLACE LEDS NEAR P1

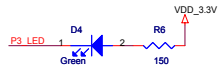
PORT 1 LANE STATUS INDICATOR



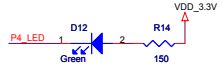
PORT 2 LANE STATUS INDICATOR



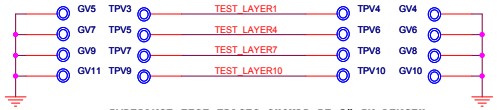
PORT 3 LANE STATUS INDICATOR



PORT 4 LANE STATUS INDICATOR



IMPEDANCE TEST TRACES



IMPEDANCE TEST TRACES SHOULD BE 8" IN LENGTH. GROUND VIAS SHOULD BE SPACED 0.1" FROM THE CORRESPONDING TEST POINT VIA. TVP3-TVP10 AND GV4-GV11 DIAMETERS ARE 30-MIL

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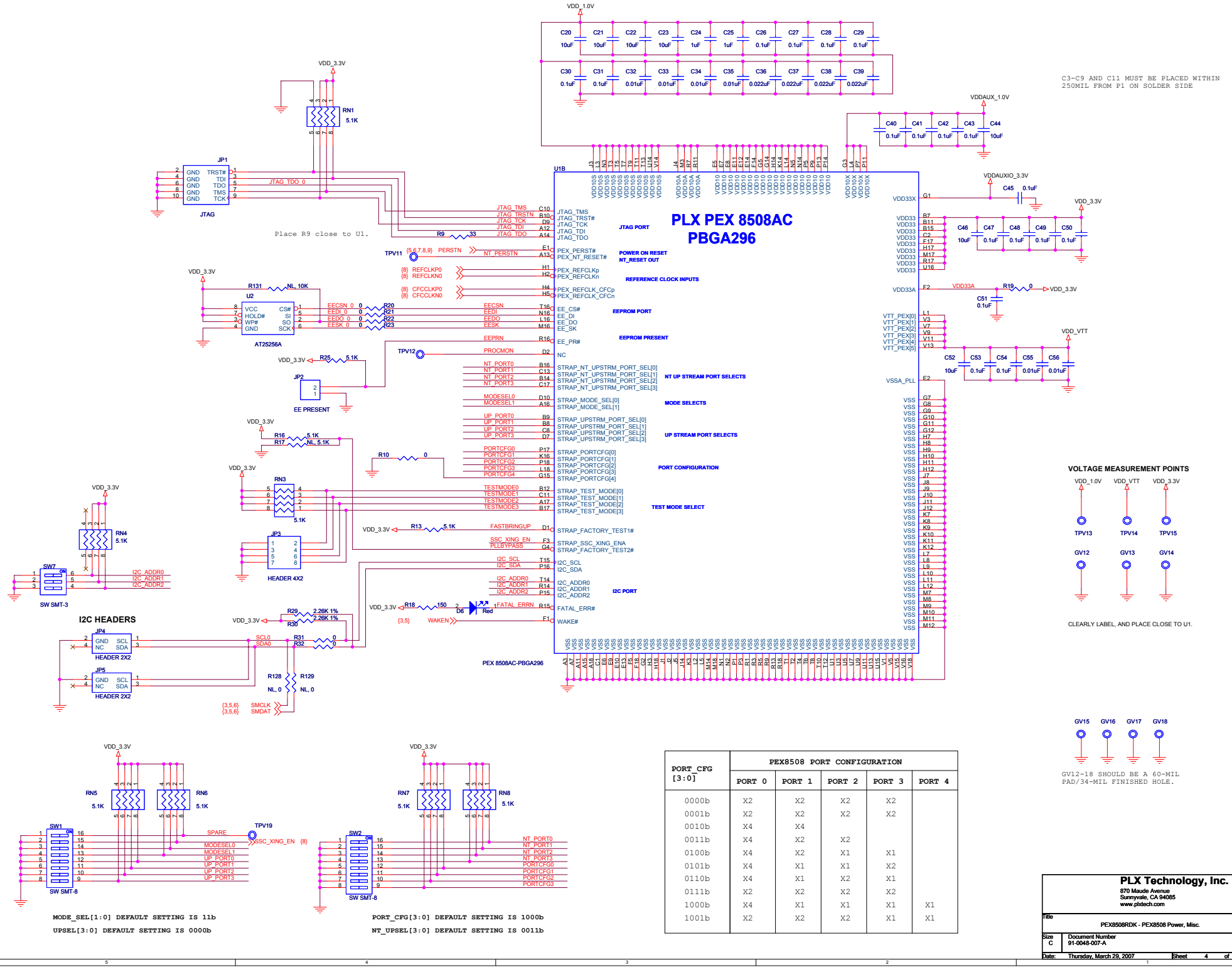

PORT_CFG [3:0]	PEX8508 PORT CONFIGURATION				
	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4
0000b	X2	X2	X2	X2	
0001b	X2	X2	X2	X2	
0010b	X4	X4			
0011b	X4	X2	X2		
0100b	X4	X2	X1	X1	
0101b	X4	X1	X1	X2	
0110b	X4	X1	X2	X1	
0111b	X2	X2	X2	X2	
1000b	X4	X1	X1	X1	X1
1001b	X2	X2	X2	X1	X1

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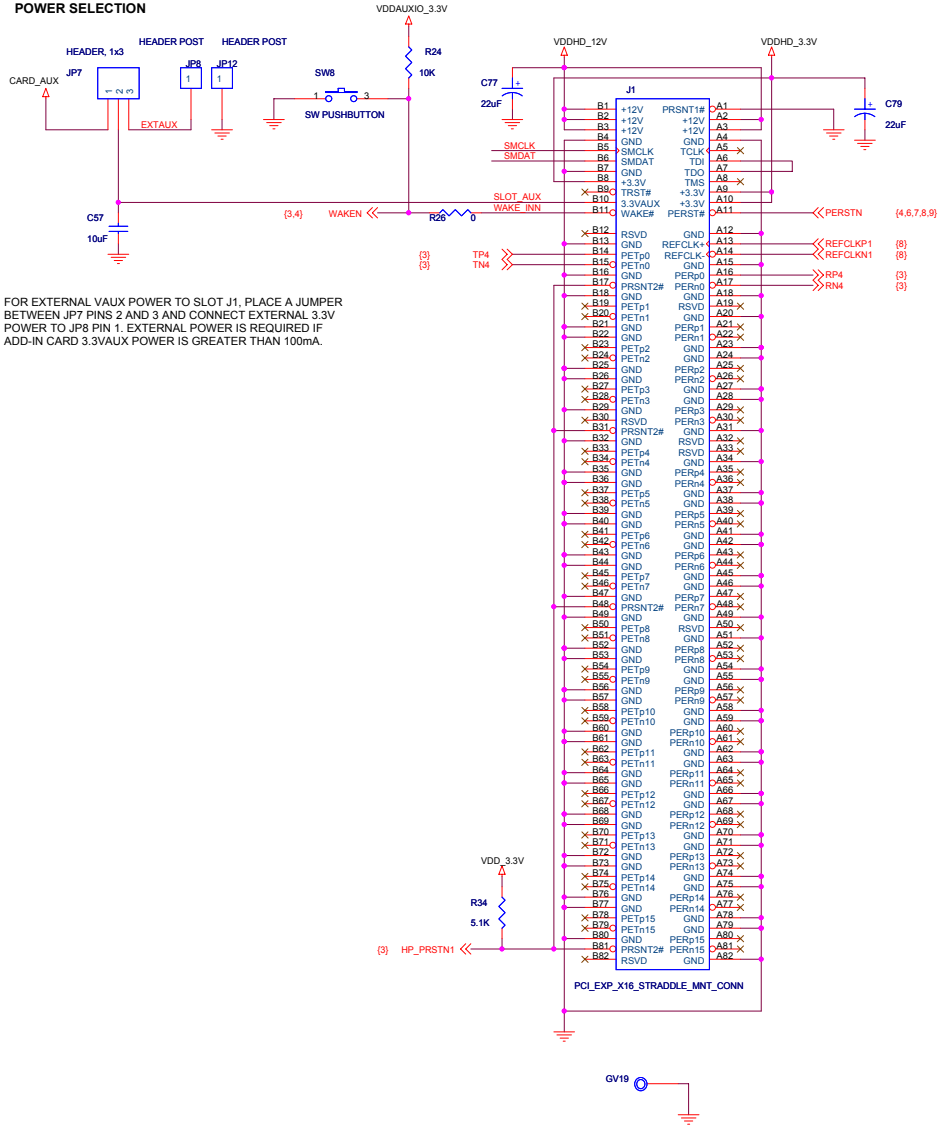
PORT 1 SLOT CONNECTOR

PORT 2 SLOT CONNECTOR

DOWNSTREAM VAUX POWER SELECTION



FOR EXTERNAL VAUX POWER TO SLOT J1, PLACE A JUMPER BETWEEN JP7 PINS 2 AND 3 AND CONNECT EXTERNAL 3.3V POWER TO JP8 PIN 1. EXTERNAL POWER IS REQUIRED IF ADD-IN CARD 3.3VAUX POWER IS GREATER THAN 100mA.

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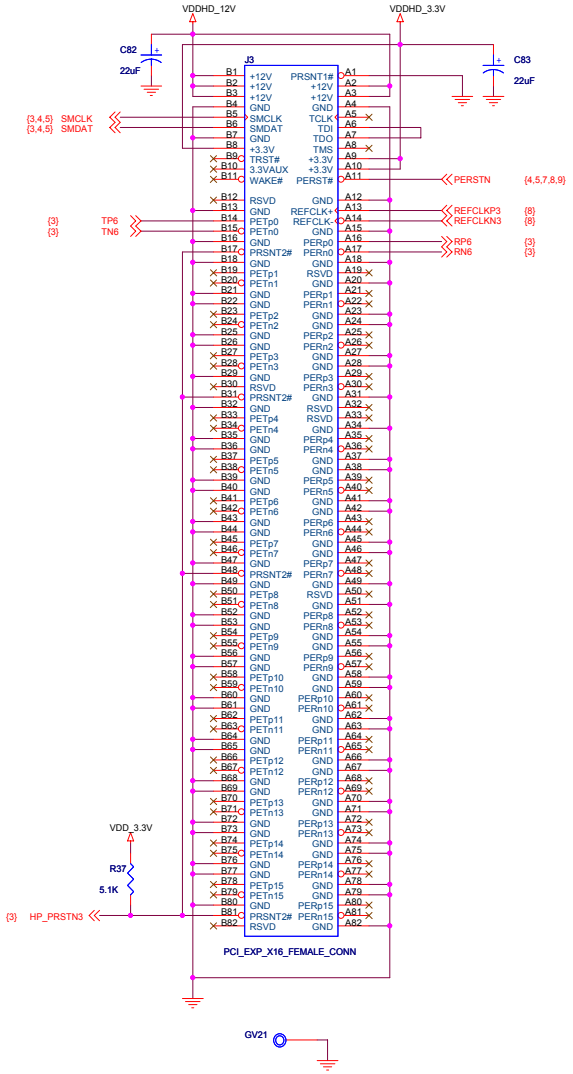
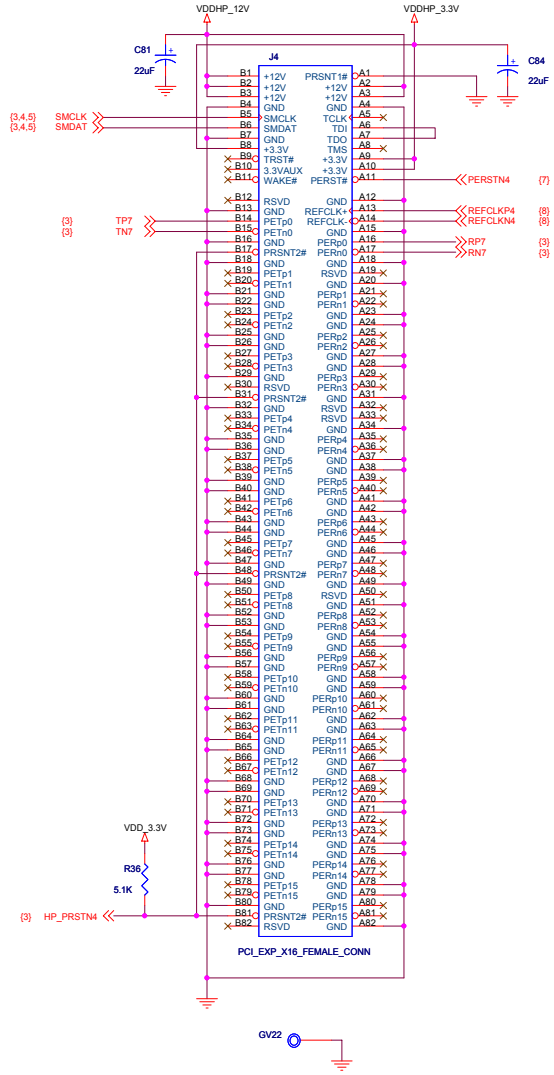
PORT 3 SLOT CONNECTOR



PORT 4 SLOT CONNECTOR



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Title: PEX8508RDK - PCI Express Slot Connectors 2

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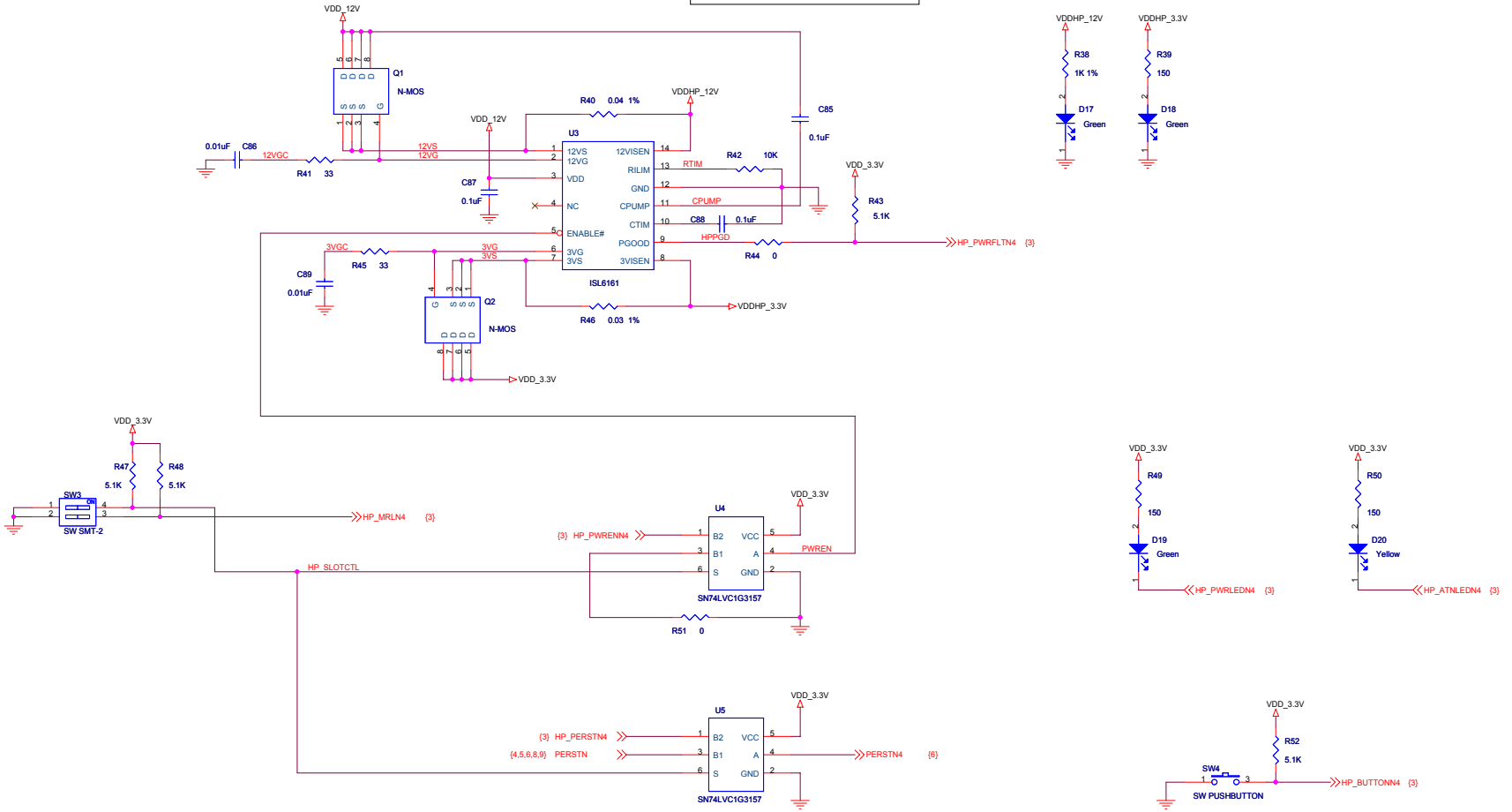
HOT PLUG CIRCUIT

PLACE D17 AND D18 NEAR J4.



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Title	PEX8508RDK - Hot Plug Circuitry	
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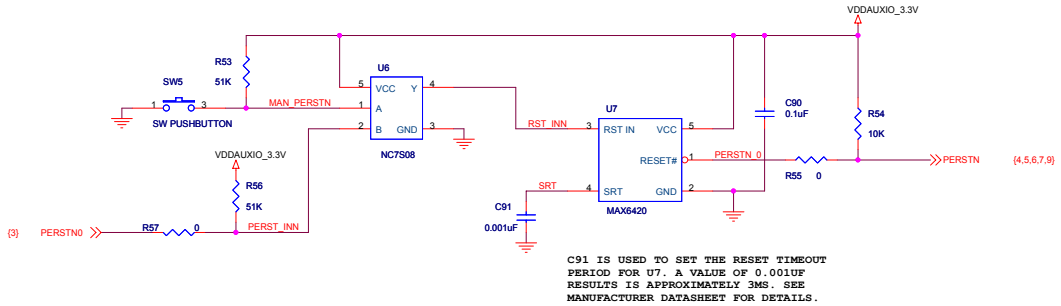
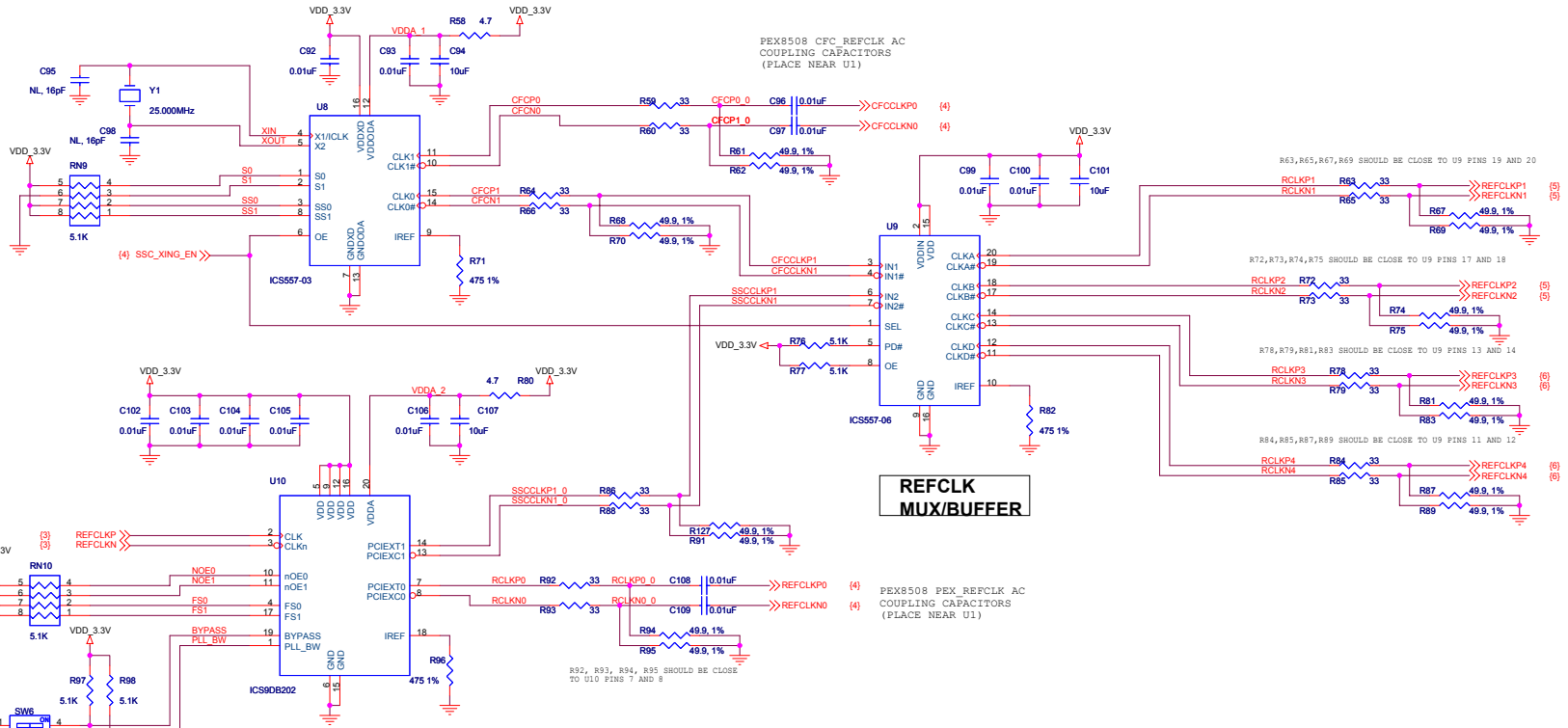
RESET CIRCUIT



REFCLK GENERATOR



REFCLK MUX/BUFFER

REFCLK BUFFER

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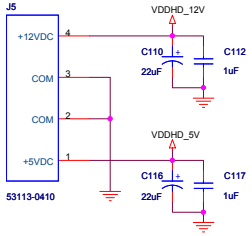
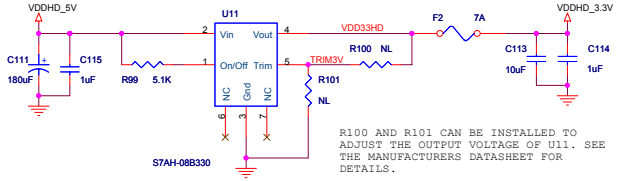
J1/J2/J3 SLOT POWER

ATX 4-PIN HARD DISK CONNECTOR



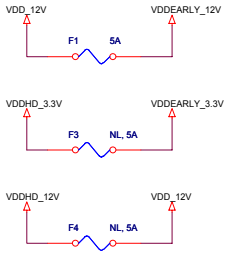
NOTE: THE PCI EXPRESS CEM 1.1 SPEC DOES NOT ALLOCATE ENOUGH POWER FOR ADD-IN CARDS TO USE ON FANOUT SLOTS. J5 IS USED TO GENERATE POWER FOR THE SLOT CONNECTORS J1 AND J2. THE +12V IS USED DIRECTLY, WHILE THE +5V IS CONVERTED TO +3.3V VIA U12. IF THE USER WANTS TO USE P1 TO GENERATE POWER FOR J1 AND J2, INSTALL F3 AND F4, AND REMOVE F1 (DO NOT USE J5).

5V-TO-3.3V DC/DC CONVERTER



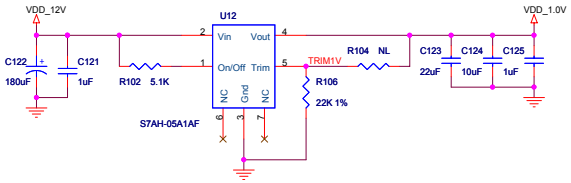
R100 AND R101 CAN BE INSTALLED TO ADJUST THE OUTPUT VOLTAGE OF U11. SEE THE MANUFACTURERS DATASHEET FOR DETAILS.

PLANE JOINING FUSES



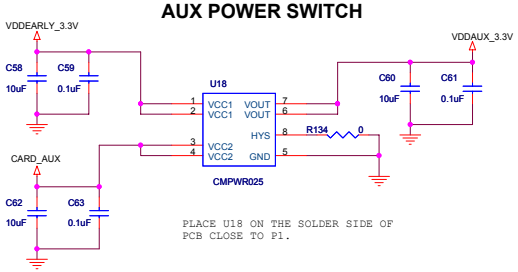
PEX 8508 POWER

12V-TO-1V DC/DC CONVERTER



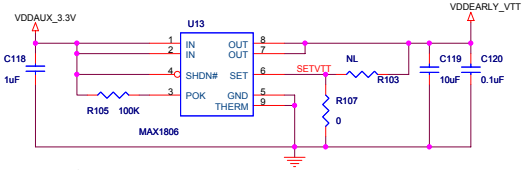
U12 VOUT CAN RANGE FROM 3.63V TO 0.9V, BY VARING R106. A VAULE OF 22KOHM SETS VOUT TO 1.06V.

AUX POWER SWITCH



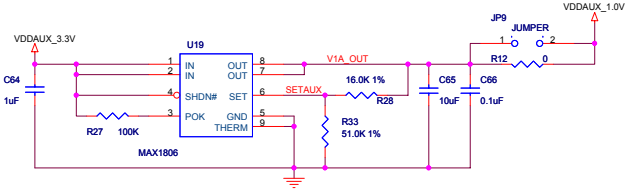
PLACE U18 ON THE SOLDER SIDE OF PCB CLOSE TO P1.

VTT REGULATOR



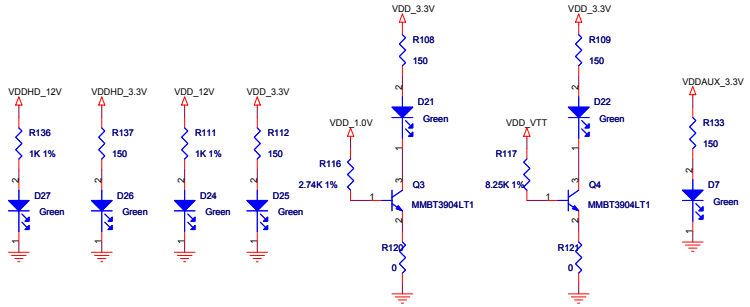
PIN 9 IS A THERMAL PAD UNDERNEATH U13.

1.0V AUX REGULATOR

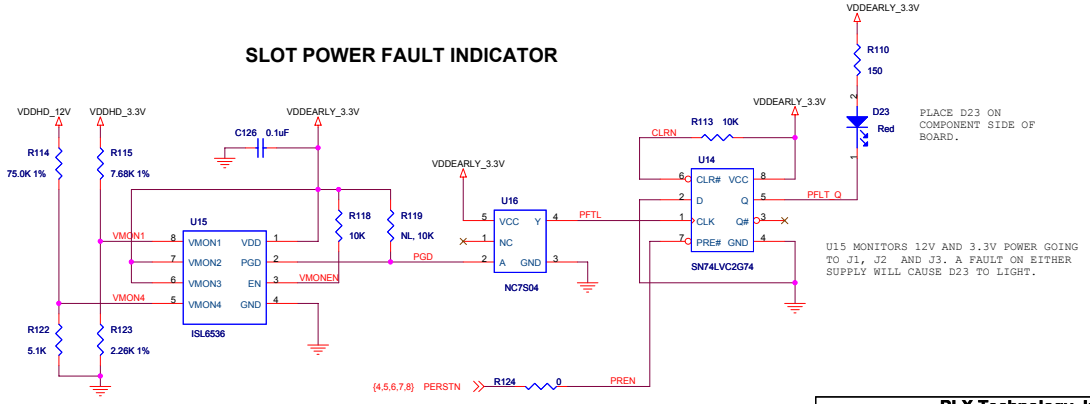


PIN 9 IS A THERMAL PAD UNDERNEATH U19.

BOARD POWER ON INDICATOR LEDS



SLOT POWER FAULT INDICATOR



PLACE D23 ON COMPONENT SIDE OF BOARD.

U15 MONITORS 12V AND 3.3V POWER GOING TO J1, J2 AND J3. A FAULT ON EITHER SUPPLY WILL CAUSE D23 TO LIGHT.

PLACE U16, U17, AND U18 ON SOLDER SIDE.

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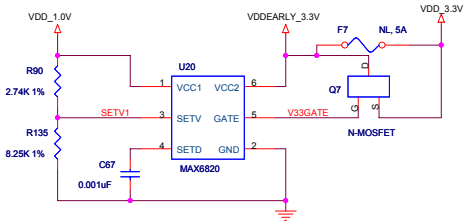
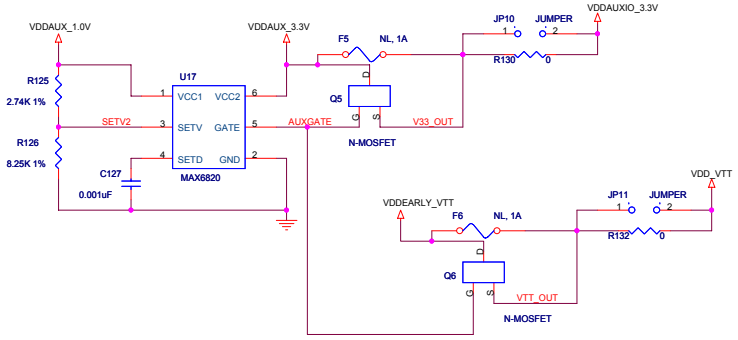
BOARD POWER SEQUENCER



NOTE: FUSE LOCATIONS F5, F6, AND F7 HAVE BEEN PLACED SIMPLY TO ALLOW THE ABILITY OF BYPASSING THE POWER SEQUENCING CIRCUITRY. THESE LOCATIONS CAN BE POPULATED WITH PROPERLY SIZED FUSES OR 0-OHM RESISTORS. TO BYPASS POWER SEQUENCING, FETS Q5, Q6, AND Q7 SHOULD BE REMOVED.

NOTE: C67 AND C127 PROVIDE A DELAY OF T_DELAY = (2.48X10^6) * (0.001X10^-6) = 2.48MS



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Title: PEX8508RDK - Power Sequencing Circuitry		
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