PEX 8505 Schematic Design Checklist

November 29, 2007
Version 1.1

Purpose and Scope

The purpose of this document is to provide a checklist of recommendations for successfully implementing the PEX 8505 device in a schematic and PCB design. It provides basic guidelines for consideration when performing schematic design and PCB design of the PEX 8505. References to other PLX documents are provided for additional information.

1 OrCAD Symbol

The ORCAD symbols for the PEX 8505 are shown in Figure 1 and Figure 2 below. These symbols are generated by the PLX and are used internally in the design of the Rapid Development Kits (RDKs). It is highly recommended to use the OrCAD symbols provided by PLX whenever possible.

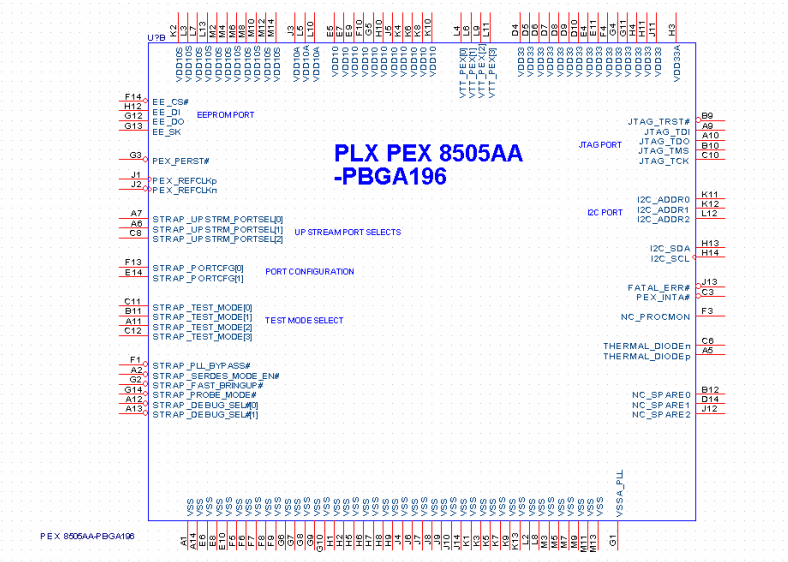

Figure 1. PEX 8505 OrCAD Symbol

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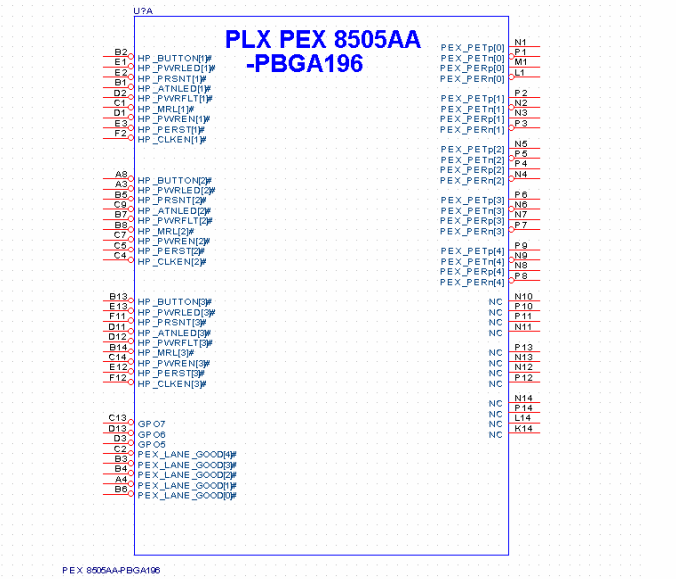

Figure 2. PEX 8505 OrCAD Symbol

2 Silicon Requirements

The current silicon revision for the PEX8505 is Revision AA. Although the PEX 8505 supports a serial EEPROM interface for register configuration purposes, a serial EEPROM is *not required* for this device; that is, the PEX 8505 default configuration is appropriate for many applications. However, in the case where additional configuration is required for performance tuning or other functional changes, a serial EEPROM can be used. For assistance in generating an EEPROM image for the PEX 8505, please contact the PLX Applications Group.

Any known errata for the PEX 8505 are documented and can be obtained from the PLX website at the following URL: http://www.plxtech.com/ 8505.

An NDA is required to access the Errata Document. Please follow the instructions on the website for details.

3 Schematic Guidelines

Please review the PEX 8505 Quick Start Design Guide for important information on how to design with the PEX 8505. Another good reference is the Rapid Development Kit for the PEX 8505. The schematic for the PEX8505 RDK is included in the PEX 8505 Hardware Reference Manual. This design has been extensively tested by PLX and it makes for a good starting point in the case of a new PEX8505 design.

3.1 Schematic Connections – Transparent Port

APPLICATION: **ADD-IN CARD** ☐ **EMBEDDED** ☐ **DAUGHTER CARD** ☐ **UNKNOWN** ☐

CUSTOMER: **DATE:**

8505 SCHEMATIC CHECKLIST – Transparent Mode

3.1.1 CLOCK INTERFACE:

Table 1. Transparent Port Clock Interface Connections

CLOCK SOURCES/ PIN NAMES	PIN #	TYPE	TERMINATION	RECOMMENDATIONS
PCI-EXPRESS				
External REFCLK Clock Transmitter	N/A	External-CML	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Recommended: 33Ohm series and 49Ohm shunt required on each differential Pair. **Maximum clock Frequency Tolerance allowed for REFCLK source is +/- 300PPM. Make sure your REFCLK oscillator supports this**
	N/A	External-LVPECL	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Please verify for your system. 100Ohm shunt required on each differential pair.
	N/A	External-LVDS	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Please verify for your system. 2KOhm coupling resistor required across differential signal pairs close to PEX 8505 Clock inputs
PEX_REFCLKn Input	J2	CMLCLKn	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Requires 100nF AC Coupling Capacitor in series with each

CLOCK SOURCES/ PIN NAMES	PIN #	TYPE	TERMINATION	RECOMMENDATIONS
				differential signal.
PEX_REFCLKp Input	J1	CMLCLKp	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Requires 100nF AC Coupling Capacitor in series with each differential signal.

3.1.2 RESET

Table 2. Transparent Port Chip Reset Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
PEX_PERST#	G3	I	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCI Express Reset. Propagates to Downstream ports.

3.1.3 SERIAL EEPROM

Table 3. Transparent Port Serial EEPROM Connections

EPROM TYPE	PIN#	STATUS	SUPPLY	RECOMMENDATIONS
AT25256A	N/A	**NOT PRESENT** ☐ **PRESENT** ☐	**+3.3V** ☐ **Other** ☐	Existing +3.3V supply must be used. Default recommended EEPROM.
PIN NAME	**PIN#**	**TYPE**	**PIN STATUS**	**RECOMMENDATIONS**
EE_CS#	F14	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Serial EEPROM Chip select Output. Weakly pulled up. Can be left floating if not used or stronger pull-ups (5K-10KOhms) used. ***This signal is an output. Verify that signal is being used accordingly on the schematic***.
EE_DI	H12	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Serial EEPROM Data Input. Weakly pulled up. Can be left floating if not used or stronger pull-ups (5K-10KOhms used) ***This signal is an output. Verify that signal is being used accordingly on the schematic***
EE_DO	G12	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Serial EEPROM Data Output. Weakly pulled up. Can be left floating if not used or stronger pull-ups (5K-10KOhms used). ***This signal is an input. Verify that signal is being used accordingly on the schematic***.
EE_SK	G13	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Serial EEPROM Clock Output Programmable [by way of the Serial EEPROM Clock Frequency Register EepFreq[2:0] field (offset 268h[2:0])] to the following: • 1 MHz • 1.98 MHz

EPROM TYPE	PIN#	STATUS	SUPPLY	RECOMMENDATIONS
				• 5 MHz • 9.62 MHz • 12.5 MHz • 15.6 MHz • 17.86 MHz Serial EEPROM Clock output. Weakly pulled up. Can be left floating if not used or stronger pull-ups (5K-10KOhms) used. ***This signal is an input. Verify that signal is being used accordingly on the schematic***.

3.1.4 PORT STRAPPING BALLS

Table 4. Port Strapping Ball Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
STRAP_DEBUG_SEL[1:0]#	A13, A12	I STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	For Factory Test Only (2 Balls) Must be tied High. (VDD33). 5K-10Kohm pull up preferred
STRAP_FAST_BRINGUP#	G2	I STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	For Factory Test Only Must be tied High. (VDD33). 5K-10Kohm pull up preferred
STRAP_PLL_BYPASS#	F1	I STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	For Factory Test Only Must be tied High. (VDD33A). 5K-10Kohm pull up preferred
STRAP_PORTCFG[1:0]	E14, F13	I STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Strapping Signals to Select Number of Lanes in Port Configuration for Ports 0,1,2,3,4(2 Balls) Register/Bits – Port Configuration Register Port Configuration field (Port 0, offset 224h[1:0]) LL,HH=x1,x1,x1,x1,x1 LH=x2,x1,x1,x1 HL=x2,x2,x1 ***Verify Strapping of these pins matches the desired operating mode of the switch.***
STRAP_PROBE_MODE#	G14	I STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	For Factory Test Only Must be tied High. (VDD33). 5K-10Kohm pull up preferred
STRAP_SERDES_MODE_ENABLE#	A2	I STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	For Factory Test Only Must be tied High.

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
				(VDD33). 5K-10Kohm pull up preferred
STRAP_TESTMODE[3:0]	C12, A11, B11, C11	I STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Test Mode Selects (4 Balls) Reserved for Factory Test Only. HHHH = Default (Test modes are disabled) Must be tied High (VDD33). 5K-10Kohm pull up preferred ***Verify Strapping of these pins matches the desired operating mode of the switch*.**
STRAP_UPSTR_PORTSEL[2:0]	C8, A6, A7	I STRAP	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Strapping Signals to Select Upstream Port (3 Balls) Register/Bits – Debug Control register Upstream Port ID field (Port 0, offset 1DCh[11:8]) LLL = Port 0 (Default) LLH = Port 1 LHL = Port 2 LHH = Port 3 HLL = Port 4 HLH = Reserved HHL = Reserved HHH = Reserved Signals must not be strapped to "**Reserved**" settings. ***Verify Strapping of these pins matches the desired operating mode of the switch*.**

3.1.5 POWER SUPPLY

Table 5. Power Supply Connections

POWER SEQUENCING	STATUS	RECOMMENDATIONS
VDD10/S, VTT, VDD33/A	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Schematic should include power sequencing circuitry to assure that: (1) VDD10/S power up first and power down last. (2) All power rails should power within 50ms of each other

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
VDD10	E5, E7, E9, F10, G5, H10, J5, K4, K6, K8, K10	CPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	***1.0V Power for Core Logic.*** *The discrete decoupling capacitors are meant to cover frequencies from 1Mhz to 200MHz without creating frequency holes.*

				The design also relies on the plane capacitance following are the recommended values for the decoupling capacitors. 1. *Four 0.01uF* 2. *Four 0.022uF* 3. *Four 0.1uF* 4. *Two 1uF* 5. *Four 10uF*
VDD10A	J3, L5, L10	APWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	*ANALOG PWR:* *320Mhz Low Pass Filter should be used to improve noise tolerance. 100nF and 10uF Decoupling Caps can be shared with VDD10 supply. However, decoupling caps are required right at the supply pins.* *Filter should reject VCC noise between 600Khz to 320Mhz.* ***Verify that VDD10A is at 1.0V +/- 10%.***
VDD10S	K2, L3, L7, L13, M2, M4, M6, M8, M10, M12, M14	SerDesPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	*DIGITAL PWR:* *Decoupling Caps can be shared with VDD10 supply. However, decoupling caps are required right at the supply pins* ***Verify that VDD10A is at 1.0V +/- 10%.***
VDD33	D4, D5, D6, D7, D8, D9, D10, E4, E11, F4, G4, G11, H4, H11, J11	I/OPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	*I/O LOGIC PWR:* *>Four 0.01uF Decoupling Caps placed as close to Balls as possible* *>One 10uF Decoupling Caps placed as close to Balls as possible* ***Verify that VDD33 is at 3.3V +/- 10%.***
VDD33A	H3	PLLPWR	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	*PLL PWR:* *Additional .1uF capacitors should be placed near to this pin depending on the extent of supply noise.* ***Verify that VDD33A is at 3.3V +/- 10%.***
VSS	A1, A14, E6, E8, E10, F5, F6, F7, F8, F9, G6, G7, G8, G9, G10, H1, H2, H5, H6, H7, H8, H9, J4, J6, J7, J8, J9, J10, J14, K1, K3, K5, K7, K9, K13, L2, L8, M3, M5, M7, M9, M11, M13	GND	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	*Ground and Thermal Ball-Ground Connections.*
VSSA_PLL	G1	PLL_GND	**YES** ☐ **NO** ☐	*PLL Ground Connection.*

			UNKNOWN ☐	
VTT_ PEX[3:0]	*L11, L9, L6, L4*	*Supply*	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	*SERDES Termination Supply.* *>Four 0.1uF Decoupling Caps placed as close to Balls as possible* *>One 10 uF Decoupling Caps placed as close to Balls as possible* ***This supply should be implemented separate from other supplies.*** ***Verify that VTT is between 1.0V to 1.8V.***

3.1.6 JTAG PINS

Table 6. JTAG Ball Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
JTAG_TCK	C10	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	JTAG Test Clock Input. JTAG Test Access Port (TAP) Controller clock source. JTAG_TCK frequency can be from 0 to 10 MHz. Should be pulled up to VDD33 if unused.
JTAG_TDI	A9	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	JTAG Test Data Input Serial input to the TAP Controller for test instructions and data. Should be pulled up to VDD33 if unused
JTAG_TDO	A10	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	JTAG Test Data Output Serial output to the TAP Controller for test instructions and data
JTAG_TMS	B10	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	JTAG Test Mode Select Input Input decoded by the TAP Controller to control test operations. Should be pulled up to VDD33 with a 3K to 10KOhm resistor if unused
JTAG_TRST#	B9	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	JTAG Test Reset. Active Low input Active-Low input, to place the Test Access Port(TAP) Controller into Test-Logic-Reset state, which enables normal logic operation. Tie to VSS through a 1.5KOhm resistor when Test Access Port is not being used.

3.1.7 I²C PINS

Table 7. JTAG Ball Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
I2C_ADDR[2:0]	L12, K12, K11	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	I²C Slave Address Bits 2 through 0. Used to set the PEX 8505 address on the I²C Bus. Must be pulled up to VDD33 through external resistors.
I2C_SCL	H14	I OD	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	I²C Serial Clock Line I²C Clock Source Use a 2.26 K Ohm Pull-up.
I2C_SDA	H13	I/O OD	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	I²C Serial Data Output Transfer and receives I²C data.

3.1.8 FATAL ERROR/ PEX_INTA# SIGNAL

Table 8. Fatal Error and PEX_INTA#

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
FATAL_ERR#	J13	I/O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	***Fatal Error*** Asserted Low when a Fatal error is detected in the PEX8505. The Device Control Register Fatal Error Detected bit (offset 70h[18]) is set. ***No Pull up Required.***
PEX_INTA#	C3	OD	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	**Interrupt Message** Interrupt output enabled when INTA# messages are enabled (**Command** register *Interrupt Disable* bit, offset 04h[10]=0) and Message Signaled Interrupts (MSI) are disabled (**MSI Control** register *MSI Enable* bit, offset 48h[16]=0). ***Pull up 5-10 K ohms if used.*** ***No Pull up Required if not used.***

3.1.9 NO CONNECT BALLS

Table 9. No Connect Balls

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
N/C	N10, N11, N12, N13, N14, K14, L14, P10, P11, P12, P13, P14	Reserved	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	***No Connect.*** ***Do not connect this pin to any electrical path on the board.***
NC_PROCM	F3	RESERVED	**YES** ☐ **NO** ☐	***No Connect.***

ON			**UNKNOWN** ☐	***Do not connect this pin to any electrical path on the board.***
NC_SPARE[2:0]	J12, D14, B12	RESERVED	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	***No Connect.*** ***Do not connect this pin to any electrical path on the board.***
THERMAL_DIODEn	C6	Reserved	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	No Connect: Don't connect this to electrical Path.
THERMAL_DIODEp	A5	Reserved	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	No Connect: Don't connect this to electrical Path.

3.1.10 HOT PLUG CONTROLLER INTERFACE

Table 10. Hot Plug Port Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
HP_ATNLED[3,1]#	D11, C9, B1	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Hot Plug Attention LED for Ports 3,2 and 1 (3 Balls). Active Low Output. Don't Care if Hot-Plug is unused
HP_BUTTON[3,1]#	B13, A8, B2	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Hot Plug Attention Button for Ports 3 ,2 and 1 (3 Balls). If Hot-Plug is unused leave unconnected or pulled up to VDD33. Otherwise, driven active low Recommended Resistance 3K to 10K Ohms.
HP_CLKEN[3,1]#	F12, C4, F2	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Reference clock enable outputs for Ports 3, 2 and 1 (3 Balls). Don't care if Hot-Plug is unused
HP_MRL[3,1]#	B14, B8, C1	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Hot-Plug Manually-operated retention latch If Hot-Plug is unused, leave unconnected or pull up to VDD33 Otherwise, driven active low
HP_PERST[3,1]#	E12, C5, E3	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Active low reset output for Downstream Ports 3, 2 and 1 (3 Balls). Don't Care if Hot Plug is unused Recommended Resistance 3K to 10K Ohms.
HP_PRSNT[3,1]#	F11, B5, E2	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Combination of Hot Plug PRSNT1# and PRSNT2# Input for Ports 3, 2 and 1 (3 Balls). If Hot-Plug is unused, leave unconnected or pull up to VDD33. Otherwise, driven active low

				Recommended Resistance 3K to 10K Ohms.
HP_PWREN[3,1]#	C14, C7, D1	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Active Low Hot Plug Power Enable Output for Station 0 Ports. Don't Care if Hot Plug is unused
HP_PWRFLT[3,1]#	D12, B7, D2	I/PU	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Hot Plug Power Fault Input for Ports 3, 2 and 1 (3 Balls). If Hot-Plug is unused, leave unconnected or pull up to VDD33. Otherwise, driven active low Recommended Resistance 3K to 10K Ohms.
HP_PWRLED[3,1]#	E13, A3, E1	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	Hot Plug Power LED Output for Ports 3, 2 and 1 (3 Balls). Don't Care if Hot-Plug is unused.

3.1.11 PCI EXPRESS BUS INTERFACE

Table 11. PCI Express Interface Connections

PIN NAME	PIN#	TYPE	PIN STATUS	RECOMMENDATIONS
PEX_PERn[4:0]	P8, P7, N4, P3, L1	CMLRn	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Receive Signals for Station 0
PEX_PERp[4:0]	N8, N7, P4, N3, M1	CMLRp	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe positive polarity differential Lane Receive Signals for Station 0
PEX_PETn[4:0]	N9, N6, P5, N2, P1	CMLTn	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Transmit Signals for Station 0 ***Series 100nF AC coupling capacitor required on each transmit pair***.
PEX_PETp[4:0]	P9, P6, N5, P2, N1	CMLTp	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	PCIe negative polarity differential Lane Transmit Signals for Station 0 ***Series 100nF AC coupling capacitor required on each transmit pair***
PEX_LANE_GOOD[4:0]#	C2, B3, B4, A4, B6	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	These outputs can directly drive common-anode LED modules. External current-limiting resistors are required. **Highly recommended that customer implement these signal on schematic and**

				PCB to verify Link Training status.
GPO[7:5]#	D3, C13, D13	O	**YES** ☐ **NO** ☐ **UNKNOWN** ☐	These outputs can be used as general purpose Output signals. External current-limiting resistors are required.

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3.2 Additional Schematic Guidelines

3.2.1 Power Sequencing

The PEX 8505 requires its power supplies to be sequenced in a specific order. In particular during power on, VDD10, VDD10A and VDD10S should be powered up first followed by 3.3V I/O supply and VTT (SerDes Transmitter power). The power down sequence is 3.3V I/O supply, and VTT (SerDes Transmitter power) off followed by VDD10, VDD10A and VDD10S. Please make sure to implement power sequencing circuitry on your board to meet the sequencing requirements of the PEX 8505. Additional information about power sequencing can be found in the PEX8505 Quick Start Design Guide. Additionally, you can refer to the PEX 8505 RDK Hardware Reference Manual for a suggested power sequencing logic example.

3.2.2 Reset

The PEX 8505 requires the PERST# signal to be asserted for at least 100ms after the power is applied and stable to allow the chip to initialize correctly. Please make sure to implement Power-On-Reset and Power-Valid detection circuitry to meet the Reset requirements. Please refer to the PEX 8505 RDK Hardware Reference Manual for suggested reference circuits.

3.2.3 Mid-Bus Probe Pads

If the design contains an embedded PCIe link, for example, PCIe connection(s) between the PEX 8505's port(s) and endpoint(s) embedded on the same board. It is of interest to add probe pads to the PCB design for each embedded PCIe link connected to the PEX 8505. Probe pads can be useful when debugging a problem on a PCIe link with a PCIe analyzer. PCIe Analyzer Manufacturers provide circuitry, called Mid-Bus Probes, to aid in the debugging effort of the embedded links. Be advised that jitter and/or loss of signal integrity can be introduced when implementing Mid-Bus Probe footprints in the design and are outside the scope of this document.

For more information please contact PLX Technical Applications.

3.2.4 Lane Good Logic

The PEX 8505 contains 5 PEX_LANE_GOOD outputs for each SerDes Lane on the device. There outputs are active low so they can drive LEDs on the board. These signal provide a visual indication to determine whether a specific SerDes lane is up and active (In the L0, normal operating) mode on any port on the PEX 8505. Implementation of these signals is highly recommended for monitoring the lane/port status of the PEX 8505.

3.2.5 Spread Spectrum Clocking (SSC)

The PEX 8505 supports a Spread Spectrum REFCLK source. The SSC clock *must* originate from the PCIe connector on a slot in the motherboard or through a common clock source that is being distributed to all add-in cards and/or PCIe devices in the system.

If your REFCLK source is non-SSC, then you may have separate REFCLK sources on different cards or devices as long as their frequency difference is within +/- 300ppm. (~30ps for a 100Mhz Clock source) Please refer to the PEX 8505 Quick Start Design Guide for more information.

4 PEX 8505 Power Consumption Notes

The power consumption of the PEX 8505 is divided in to four sources. There are separate power consumption values for the Core (VDD10/A) SerDes Digital Supply (VDD10S), SerDes Analog Supply (VTT) and 3.3V IO (VDD33A) The total power consumption of the device is the sum of the power draw from all of these four sources. The amount of power the device actually consumes depends largely on the application and traffic patterns on the switch; the higher the traffic flow through the switch, the power consumption of the device will be higher. Please refer to “Electrical Specifications” section of PEX 8505 Data book for more details.

5 General PCB Routing Guidelines

Since PCIe links operate at very high speeds (2.5GHz), proper PCB routing of each RX and TX pair in each lane is critical for maintaining signal integrity on each PCIe link. The PCI-SIG provides numerous suggestions about how to correctly design PCB’s containing PCIe links. Several important guidelines are listed below. Additional information is available from the PCI-SIG website.

1. Recommended Microstrip Trace Routing Guidelines:
   - Differential Impedance 4, 6 layer: 100 Ohms +/- 20% 8, 10 layer: 85 Ohms +/- 20%
   - Single ended Impedance 4, 6 layer: 60 Ohms +/- 15% 8, 10 layer: 55 Ohms +/- 15%
2. Recommended Stripline Trace Routing Guidelines:
   - Differential Impedance 6 layer: 100 Ohms +/- 15% 8, 10 layer: 85 Ohms +/- 15%
   - Single ended Impedance 6 layer: 60 Ohms +/- 15% 8, 10 layer: 55 Ohms +/- 15%
3. Recommended for all differential signal pairs: maintain >= 20 mil trace edge to plane edge gap
4. Recommended Length matching Intra-pair: max 5 mil delta, matching maintained segment to segment, match at point of discontinuity, but avoid "tight bends"
5. Gnd referenced signals is recommended. Use stitching caps with PWR referenced signal traces.
6. Use Gnd stitching vias by signal layer vias for layer changes
7. Do not route over plane splits or voids. Allow no more than 1/2 trace width routed over via antipad
8. Match left/right turn bends where possible. No 90-degree bends or "tight" bend structures.
9. The reference clock signal pair should maintain the same reference plane for the entire routed length and should not cross any plane splits (breaks in the reference plane)
10. Reference clock terminating components should be placed as close as possible to their respective device, ideally within 100 mils of the clock/receiver component pin
11. Match all segment lengths between differential pairs along the entire length of the pair.
12. Maintain constant line impedance along the routing path by keeping the same line width and line separation.
13. Avoid routing differential pairs adjacent to noisy signal lines or high speed switching devices such as clock chips.
14. Recommended reference clock differential pair spacing (clock to clock#) < = 11.25 mils.
15. Recommended reference clock trace spacing to other traces is >= 20 mils.
16. Recommended reference clock line width >= 5 mils.
17. When routing the 100Mhz differential clock, do not divide the two halves of the clock pair between layers.
18. Recommended reference clock trace impedance:
    - Single ended: 50-60 Ohms +/- 15%
    - Differential: 100 Ohms +/- 20%
19. Recommended PCI Express reference clock to PCI express reference clock length matching to within 25 mils

20. AC Coupling Capacitors: The same package size and value of capacitor should be used for each signal in a differential pair.
21. AC Coupling Capacitors: Locate capacitors for coupled traces in a differential pair at the same location along the differential traces. Place them as close to each other as possible.
22. AC Coupling Capacitors: The "breakout" into and out of the capacitor mounting pads should be symmetrical for both signal lines in a differential pair.
23. Test points and probing structures should not introduce stubs on the differential pairs.
24. Use Tantalum or Low ESR Lane AC Coupling Caps.

6 Reference Documents

- PEX 8505 Databook. URL: http://www.plxtech.com/8505
- PEX 8505 Quick Start Design Guide. URL: http://www.plxtech.com/8505
- PEX 8505 Errata[1] URL: http://www.plxtech.com/8505
- PEX 8505 EEPROM Application Note[1] – http://www.plxtech.com/8505
- PCI Express Add-in Card Compliance Checklist, Revision 1.0. PCI-SIG. http://www.pcisig.com/developers/compliance_program/compliance_checklist (Membership to PCI-SIG is required to access this document.)
- PEX 8505 Hardware Reference Manual URL: http://www.plxtech.com/8505

[1] Access to these documents requires an NDA. Please see the website for more details or contact the PLX Sales Department.