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PEX 8311RDK
Hardware Reference Manual

PEX 8311RDK
Hardware Reference Manual

Version 0.90

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ABOUT THIS MANUAL

This document describes the PLX PEX 8311RDK, the PEX 8311 Rapid Development Kit, from a hardware perspective. It contains a description of all major functional circuit blocks on the board and also is a reference for the creation of software for this product. This manual also includes a complete bill of materials and schematics.

REVISION HISTORY

Date	Version	Comments
December 2005	0.90	Initial Blue Book Release

1. General Information

The PLX PEX 8311RDK is a Rapid Development Kit based on the PEX 8311, a single-lane, PCI Express-to-local bus bridge device. The PEX 8311RDK provides a complete hardware and software development platform to facilitate getting designs up and running quickly, lowering risk and reducing time-to-market. The PEX 8311RDK allows the upstream PCI Express port of the PEX 8311 device to be connected to a host system slot by way of a standard PCI Express edge connector (the PEX 8311RDK is designed to plug into a PCI Express motherboard slot). On board Synchronous burst SRAM allows testing of data transfers and DMA operation.

The PEX 8311RDK is shipped pre-configured for de-multiplexed generic address/data bus (C mode) operation, but is very easily reconfigured for multiplexed address/data bus (J mode) applications. The RDK provides 5 surface mount QFP/SOIC/SSOP footprints and for hardware designers to easily add processors, DSPs, ASICs, FPGAs, memory, and I/O devices to test, simulate, and debug their designs without fabricating their own boards, saving considerable of time in the development process and reducing time to market. The PEX 8311RDK's software, hardware and registers are backward-compatible with the PCI 9056RDK-LITE and PCI 9656RDK-LITE, simplifying the migration of existing PCI designs into PCI Express products.

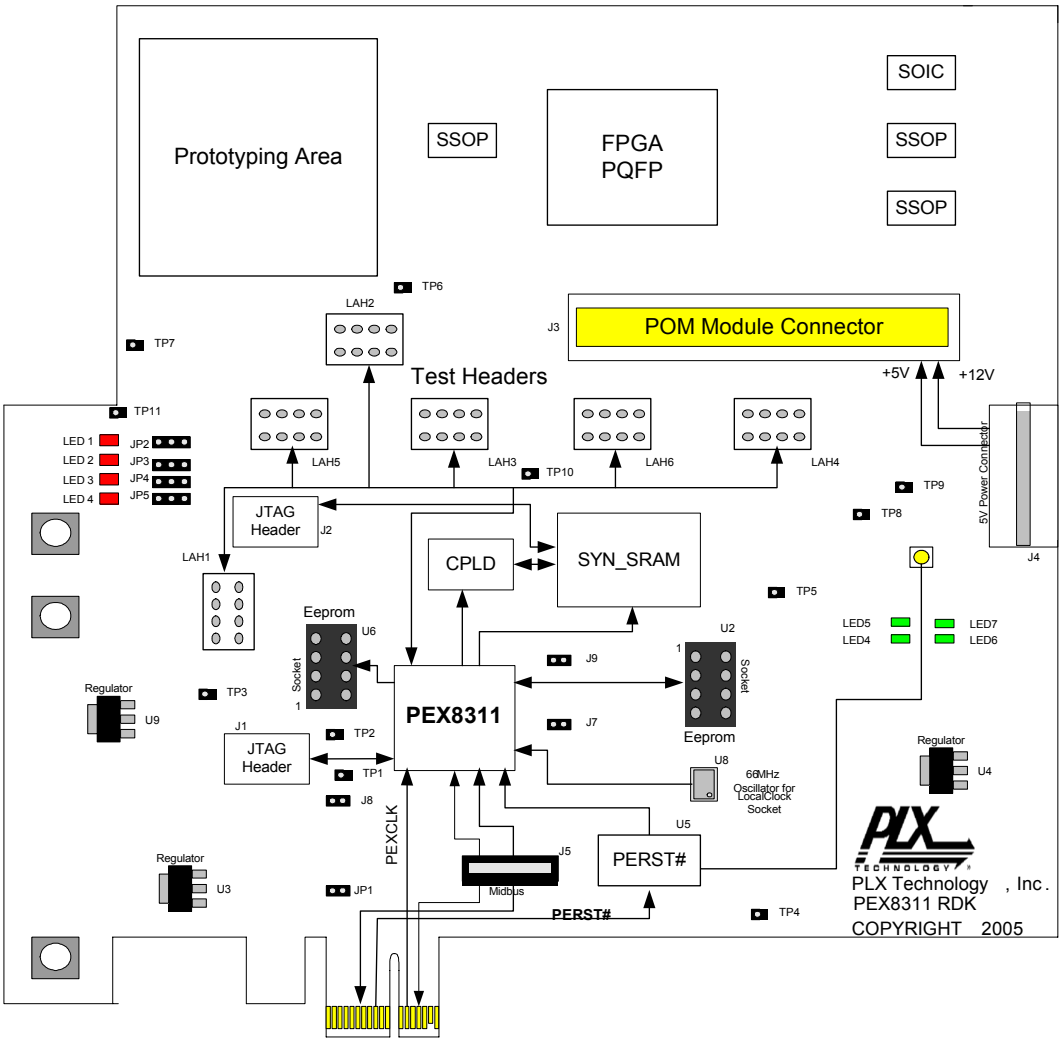


Figure 1-1. PEX 8311RDK – Component Side View

1.1 PEX 8311 Features

- Compliant to *PCI Express Base Specification, Revision 1.0a*
- Local bus and register compatibility with PCI 9056 and PCI 9656 allows systems to migrate to PCI Express and leverage software compatibility
- Integrated single PCI Express port and interface with x1 link, dual-simplex 2.5 Gbps SerDes
- Configurable local bus supporting 8, 16 and 32 bit local bus architectures
- Multiplexed and non-multiplexed local bus operation
- Powerful high performance DMA engine supporting block, scatter gather, ring management and demand mode
- Supports Endpoint and Root Complex Modes
- Small package, enabling compact design
- Low power consumption
- 3.3V I/O and 5V tolerant local bus
- Serial EEPROMs used for optional boot configuration with Serial Peripheral Interface (SPI) and Microwire Interface
- 8-KB general-purpose shared RAM

1.2 PEX 8311RDK Features

- PLX PCI Express-to-PCI bridge device in a 21 x 21 mm, 337-ball PBGA package
- Single x1 PCI Express Edge connector for insertion into standard PCI Express slot of x1 or greater link width
- Supports 32-bit C (default) or J mode Processor/Local Bus operation with speeds up to 66MHz
- 128KB synchronous burst SRAM with the CPLD memory controller demonstrates the PEX 8311 continuous burst feature
- Jumpers for PEX 8311 hardware configuration
- Socketable SPI and Microwire serial EEPROMs (3.3V devices supported)
- Onboard probing points and logic analyzer connections
- LEDs for link status visual inspection and power supply operation
- Auxiliary ATX hard disk connector for additional power requirement support
- Prototyping area with five (5) surface mount footprints, one (1) voltage regulator footprint, and one (1) 20x10, 0.1” through-hole grid
- Pushbutton reset module
- Socketed oscillator for Processor/Local Bus clock and local logic
- PLX J-Bus Option Module (POM) connector for expansion
- Option for on board PCI Express reference clock generation

2. PEX 8311RDK System Architecture

The PEX 8311RDK assists customers in evaluating PLX Technology's PEX 8311 PCI Express to local bus bridge device, and to facilitate early development of customer designs with the PEX 8311. The board is designed to operate with the PEX 8311 configured in Endpoint mode. This allows bridging between a PCI Express base board and local bus processors or logic. The PEX 8311RDK is designed to showcase many of the PEX 8311 features when operating in Endpoint mode.

The PEX 8311RDK's form factor is a eight-layer assembled 6.6"L x 8.15"W PC board. The local bus interface supports 8, 16 or 32-bit transfers, at up to 66 MHz. The PCI Express interface supports one lane operating at 2.5 Gbps.

PEX 8311RDK power is generated from the +12VDC and +3.3VDC, provided through the PCI Express edge connector. Additional +5VDC and +12VDC power can be provided using an external power supply plugged into the on board 4-pin ATX header.

3. PEX 8311RDK Hardware Architecture

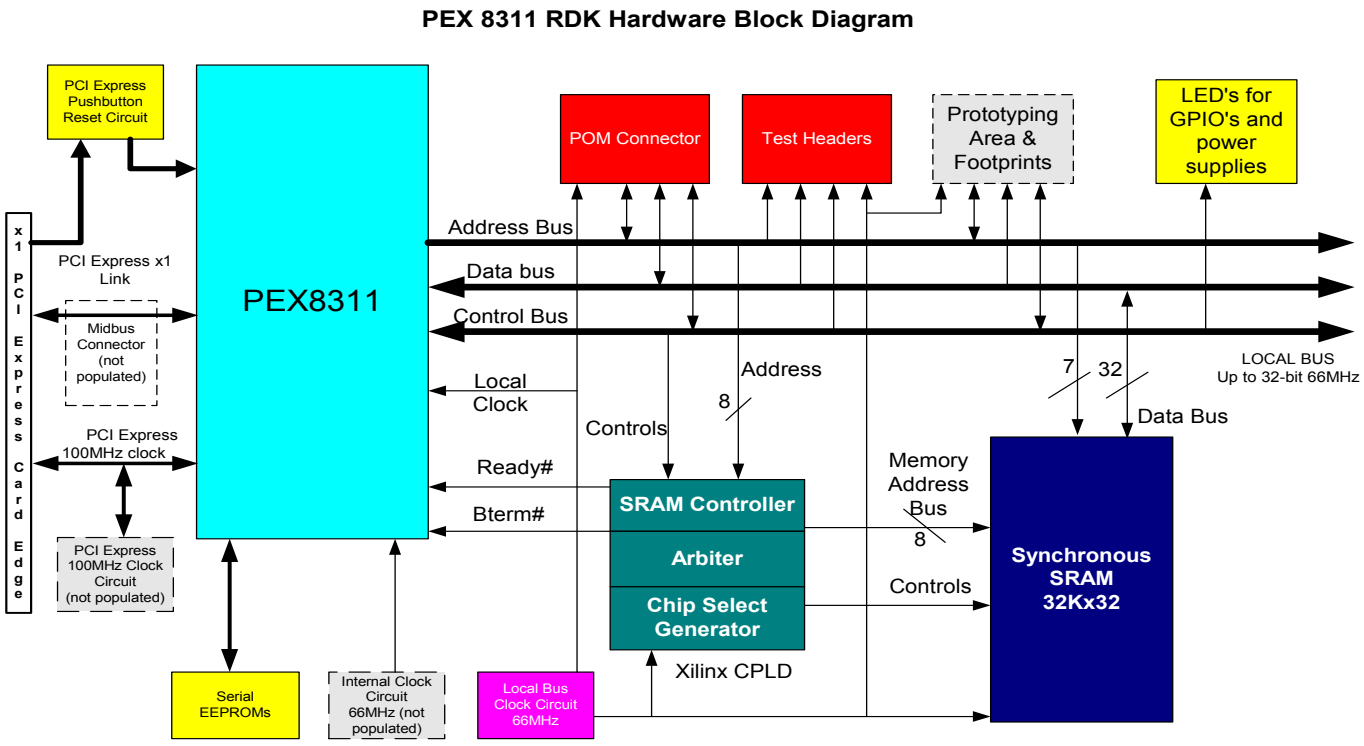


Figure 3-1. PEX 8311RDK Hardware Architecture

3.1 PEX 8311 PCI Express Bridge Device

The PEX 8311 (U1) is a high-performance PCI Express to local bus device that enables designers to migrate legacy designs to the new, advanced serial PCI Express. This 2-port device is equipped with a single-lane PCI Express port and a parallel local bus segment supporting multiplexed (J mode) and non-multiplexed (C Mode) operating modes. The PEX 8311 is capable of operating as an Endpoint or a Root Complex. The PEX 8311 bridge device is housed in a 21 x 21 mm, 337-ball PBGA package. Ball spacing is 1.0 mm. No additional cooling is required.

The PEX 8311 supports Direct Slave and Direct Master data transfers; in addition there are two DMA channels, and an Intelligent Messaging Unit. For more detailed information about the PEX 8311 please see the PEX 8311 data book.

3.2 Serial EEPROM

The PEX 8311 bridge device has two EEPROM's associated with it. These EEPROM's can be used to load configuration data on power-up.

3.2.1 SPI EEPROM

The SPI EEPROM (U2) is the Express Configuration EEPROM. This is largely used to control PCI Express performance and is not normally required to bring up the PEX 8311. The SPI EEPROM (U2) can also be used to pre-configure the on-chip 8K shared memory.

The SPI EEPROM (U2) is connected to an 8-pin DIP socket to allow removal and programming with external PROM programmer if required. The EEPROM can also be programmed through the PEX 8311 using the utilities provided. A pull-up resistor (R4) on the EERDDATA ball produces a value of FFh if there is no serial EEPROM installed.

The PEX 8311 supports up to 16 MB SPI serial EEPROM's, utilizing 1, 2, or 3-byte addressing. The PEX 8311 automatically determines the appropriate addressing mode. The SPI operates at up to 25 MHz and can directly interface with the PEX 8311. The Atmel AT25640 device as used in the PEX 8311RDK is recommended. Other compatible 128-byte serial EEPROM's include the Atmel AT25010A, Catalyst CAT25C01, and ST Microelectronics M95010W.

The SPI EEPROM on the PEX 8311RDK is blank when shipped.

3.2.2 Microwire Serial EEPROM

The socketed 2Kbit Microwire serial EEPROM (U6) is the Local Configuration EEPROM and is used to control local bus behavior and assign appropriate address ranges. It is connected directly to the PEX 8311 and provides the configuration data to initialize the device after the system reset is removed. The EEPROM image is compatible with those of the PLX PCI 9x56 devices and may be loaded with those images to speed development.

The Microwire EEPROM will be required for most designs to ensure that the correct address space ranges are assigned. A pull-up on EEDI/EEDO (R36) ensures that the RDK will boot if a blank EEPROM is installed. If no EEPROM is installed then a pull-down will be required on EEDI/EEDO (R39) to ensure that the device boots correctly.

3.2.2.1 Microwire Serial EEPROM Contents

Table 3-1. Long Serial EEPROM Load Registers

Serial EEPROM Offset	Serial EEPROM Hex Value	Description	Register Bits Affected
0h	86E1	Device ID	PCIIDR[31:16]
2h	10B5	Vendor ID	PCIIDR[15:0]
4h	0680	Class Code	PCICCR[23:8]
6h	00AA	Class Code, Revision of the PEX 8311	PCICCR[7:0] / PCIREV[7:0]
8h	0000	Maximum Latency, Minimum Grant	PCIMLR[7:0] / PCIMGR[7:0]
Ah	0100	Interrupt Pin, Interrupt Line Routing	PCIIPR[7:0] / PCIILR[7:0]
Ch	0000	MSW of Mailbox 0 (User Defined)	MBOX0[31:16]
Eh	0000	LSW of Mailbox 0 (User Defined)	MBOX0[15:0]
10h	0000	MSW of Mailbox 1 (User Defined)	MBOX1[31:16]
12h	0000	LSW of Mailbox 1 (User Defined)	MBOX1[15:0]
14h	FFFE	MSW of Range for PCI-to-Local Address Space 0	LAS0RR[31:16]
16h	0000	LSW of Range for PCI-to-Local Address Space 0	LAS0RR[15:0]
18h	0000	MSW of Local Base Address (Re-map) for PCI-to-Local Address Space 0	LAS0BA[31:16]
1Ah	0001	LSW of Local Base Address (Re-map) for PCI-to-Local Address Space 0	LAS0BA[15:0]
1Ch	0120	MSW of Mode/DMA Arbitration Register	MARBR[31:16]
1Eh	0000	LSW of Mode/DMA Arbitration Register	MARBR[15:0]
20h	2030	Local Miscellaneous Control Register 2 / Serial EEPROM Write-Protected Address Boundary	LMISC2[7:0] / PROT_AREA[7:0]
22h	8500	Local Miscellaneous Control Register 1 / Processor/Local Bus Big/Little Endian Descriptor Register	LMISC1 [7:0] / BIGEND [7:0]
24h	0000	MSW of Range for PCI-to-Local Expansion ROM	EROMRR[31:16]
26h	0000	LSW of Range for PCI-to-Local Expansion ROM	EROMRR[15:0]
28h	0000	MSW of Local Base Address (Re-map) for PCI-to-Local Expansion ROM	EROMBA[31:16]
2Ah	0000	LSW of Local Base Address (Re-map) for PCI-to-Local Expansion ROM	EROMBA[15:0]
2Ch	4343	MSW of Bus Region Descriptors for PCI-to-Local Address Space 0 and Expansion ROM	LBRD0[31:16]
2Eh	00C3	LSW of Bus Region Descriptors for PCI-to-Local Address Space 0 and Expansion ROM	LBRD0[15:0]
30h	0000	MSW of Range for Direct Master-to-PCI	DMRR[31:16]
32h	0000	LSW of Range for Direct Master-to-PCI	DMRR[15:0]
34h	6000	MSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[31:16]
36h	0000	LSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[15:0]
38h	5000	MSW of Processor/Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[31:16]
3Ah	0000	LSW of Processor/Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[15:0]
3Ch	0000	MSW of PCI Base Address (Re-map) for Direct Master-to-PCI	DMPBAM[31:16]
3Eh	0000	LSW of Processor/Local Bus Address for Direct Master-to-PCI Memory	DMPBAM[15:0]
40h	0000	MSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCRGA[31:16]
42h	0000	LSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCFGA[15:0]

Table 3-2. Extra Long Serial EEPROM Load Registers

Serial EEPROM Offset	Serial EEPROM Hex Value	Description	Register Bits Affected
44h	8311	Subsystem ID	PCISID[15:0]
46h	10B5	Subsystem Vendor ID	PCISVID[15:0]
48h	FFFE	MSW of Range for PCI-to-Local Address Space 1	LAS1RR[31:16]
4Ah	0000	LSW of Range for PCI-to-Local Address Space 1	LAS1RR[15:0]
4Ch	0000	MSW of Local Base Address (Re-map) for PCI-to-Local Address Space 1	LAS1BA[31:16]
4Eh	0001	LSW of Local Base Address (Re-map) for PCI-to-Local Address Space 1	LAS1BA[15:0]
50h	0000	MSW of Bus Region Descriptors for PCI-to-Local Address Space 1	LBRD1[31:16]
52h	01C3	LSW of Bus Region Descriptors for PCI-to-Local Address Space 1	LBRD1[15:0]
54h	0000	Hot Swap Control/Status Register	Reserved
56h	4C06	Hot Swap Control/Status Register / Hot Swap Next Capability Pointer	HS_NEXT[7:0] / HS_CNTL[7:0]
58h	0000	Reserved	Reserved
5Ah	0000	PCI Arbiter Control	PCIARB[15:4] / PCIARB[3:0]
5Ch	7A02	Power Management Capabilities	PMC[15:9,2:0]
5Eh	4801	Power Management Next Capability Pointer / Power Management Capability ID (the LSB is reserved)	PMNEXT[7:0] / PMCAPID[7:0]
60h	0000	Power Management Data / PMCSR Bridge Support Extensions (the LSB is reserved)	PMDATA[7:0]/ PMCSR_BSE[7:0]
62h	0000	Power Management Control/Status (Bits 15, 7:2, and 1:0 are reserved)	PMCSR[15:0]

3.3 Local and PCI Express Hardware Elements

As shown in Figure 3-1, the RDK hardware contains:

- PEX 8311 PCI Express I/O Accelerator
- Four PEX 8311 Local Bus components (Local clock distribution, CPLD, SBSRAM, Test Headers, and POM connector)
- LED's for GPIO and power supply status
- Small prototyping area – including an uncommitted FPGA footprint
- PCI Express Reset Circuitry (see section 3.4.2.1 Reset Circuitry)
- A hardware development module for PCI Express clock generation (see section 3.4.1 RefClk)
- A hardware development module for the PEX 8311 internal reference clock (see section 3.3.4 Internal Clock)

The RDK's Local Bus is pre-configured for non-multiplexed address and data bus operation (C mode), but it is user-configurable to allow multiplexed address and data operation (J Mode). (See Section 5 RDK Mode Configuration for details on re-configuring the RDK hardware for J Mode operation.) Once the board is correctly installed into a PC computer system, a host, such as the motherboard's processor, can perform single cycle memory read/write cycles, multiple memory read/write cycles, and burst memory read/write cycles from/to the on-board SBSRAM in Direct Slave mode. The host can also program the PEX 8311 to perform DMA data transfers between the PCI Express bus and the SBSRAM.

3.3.1 Local Clock

The PEX 8311 has a local clock input which is required for normal operation. The Cypress Semiconductor CY2305 Zero Delay 1-to-5 clock buffer (U7) provides onboard local clock distribution to the PEX 8311, SBSRAM, CPLD, test headers and the POM connector. The CY2305 input is sourced by the socketed onboard oscillator (U8). The socketed oscillator (U8) can be changed to allow PEX 8311 local bus operation at any frequency from 10 to 66MHz. The 10MHz minimum is a restriction of the CY2305, the local bus of the PEX 8311 can run at any frequency from 0 to 66MHz.

3.3.2 Synchronous Burst SRAM

A 100-pin, 7.5ns, 32K x 32 Micron Synchronous Burst SRAM (U11) is used for Processor/Local Bus data storage on the RDK. During Direct Slave memory burst cycles, the SBSRAM performs continuous back-to-back single read cycles or single write cycles. The Xilinx CPLD SBSRAM controller (U10) does all of the timing conversion and generates the lower 8 address bits to the SBSRAM. The SBSRAM takes 7 upper address lines (LA16-LA10) directly from the PEX 8311 and 8 lower address lines (MA[9:2]) from the SBSRAM controller. The data lines of the SBSRAM are directly connected to the PEX 8311 local data bus (LD31-LD0).

3.3.3 Xilinx CPLD

A 5ns Xilinx XC9572XL-5TQ100C CPLD (U10) is used as the SBSRAM controller, external Processor/Local Bus arbiter, and chip select generator.

The SBSRAM controller in the CPLD generates the lower 8-bit memory address (MA[9:2]), SBSRAM chip select (SRAMCS#), SBSRAM output enable (SRAMOE#), and SBSRAM byte write enables (SRAM_BW_[3:0]) to the SBSRAM. It latches the starting address signals (LA[9:2] for C mode and LAD[9:2] for J mode), and uses its built-in internal address counter to advance the addresses to the SBSRAM. The SBSRAM controller also generates the active low ready signal (READY#) to terminate normal PEX 8311 memory cycles and also generates the active low (BTERM#) input to the PEX 8311 to break the continuous burst memory cycle when its internal address counter reaches the final count (FFh).

The external Processor/Local Bus arbiter in the CPLD accepts the Processor/Local Bus request signals (LBR [1:0]) from Processor/Local Bus masters, if there are any, and the bus request from the PEX 8311 (LHOLD). It generates bus grant signals LBG [1:0] to the Processor/Local Bus masters and LHOLDA to the PEX 8311.

The chip select generator in the CPLD generates the SBSRAM chip select (SRAMCS#) and four additional active low chip selects for the Processor/Local Bus devices. The chip select signals are partially decoded from the upper four address lines (LA31-LA28) on the Processor/Local Bus. They can be re-programmed by altering the CPLD Verilog code.

3.3.4 Internal Clock

The PEX 8311 requires an internal clock source in addition to the PCI Express clock and the local clock. When the PEX 8311 is operating in Endpoint mode the PEX 8311 will generate the internal clock itself. The internal clock output (CLKOUT, ball A8) is fed directly to the internal clock input (CLKIN, ball A15) via the 0 ohm series resistor R53.

When the PEX 8311 is operating in Root Complex mode then the internal clock must be provided from an external source. While the PEX 8311RDK is not designed to operate in Root Complex mode provision has been made for an external clock oscillator to provide the internal clock to the PEX 8311. The components for the external clock are not assembled nor do they appear on the BOM. Customers who require this feature must source and assemble the components themselves. PLX takes no responsibility for boards damaged during this operation

If the external oscillator is to be used remove R53 and assemble R52, R150, C96, C97 and U13. The maximum operating frequency for U13 should be 66MHz.

3.3.5 PLX Option Module Connector

The PLX Option Module Connector (J3) assumes that the Local Bus is configured for 32-bit multiplexed address/data bus (J mode) operation. (See Section 5 - RDK Mode Configuration - for details on re-configuring the RDK hardware for J Mode operation.) It can be used for expansion and prototyping. Both/either a master and/or slave devices may be connected to this connector, which resides at Local Bus address range 1000 0000 – 1FFF_FFFFh. The external arbiter in the CPLD uses CS0# to select the POM module. Schematic sheet 6 provides the connector signal details.

The connector to mate to J3 can be purchased from AMP distributors the part number is: 6-104652-0

3.3.6 Hardware Memory Map

The PEX 8311RDK Local Bus memory map is shown in Table 3-3.

Table 3-3. PEX 8311RDK Processor/Local Bus Memory Map

Hex Address Range	Device	Chip Select	Comments
FFFF FFFF 5000 0000	Unused	–	Available
4FFF FFFF 4000 0000	Uncommitted FPGA (FP2)	CS3#	Available & Re-programmable
3FFF FFFF 3000 0000	Unused	CS2#	Available & Re-programmable
2FFF FFFF 2000 0000	Unused	CS1#	Available & Re-programmable
1FFF FFFF 1000 0000	J mode POM connector	CS0#	32-bit, multiplexed address/data bus
0FFF FFFF 0002 0000	Unused	–	Available
0001 FFFF 0000 0000	Synchronous burst SRAM 32Kx32	SRAMCS#	8-, 16-, or 32-bit access

3.4 PCI Express Interface

The PCI Express interface is a male card edge connector, based on the *PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a* for an x1 interface. In addition to the PCI Express TX/RX pairs the card edge provides +12 VDC and +3.3 VDC, RefClk, and PERST#. The PCI Express TX/RX signals are laid out as 100-Ohm, controlled-impedance, microstrip-differential pairs. Trace length mismatch within signal pairs is not greater than 0.005".

3.4.1 RefClk

PCI Express RefClk enters the PEX 8311RDK through the PCI Express card edge (male) connector. RefClk is laid out as a 100-Ohm, controlled-impedance, microstrip-differential pair. Trace length mismatch is not greater than 0.005".

Land is provided for the PCI Express RefClk to be generated onboard by an optional clock synthesizer (U12), using a 25-MHz crystal for the seed frequency. The PEX 8311RDK can use the IC557G-03 part from Integrated Circuit systems, Inc., though any comparable synthesizer is sufficient. RefClk is routed to the PEX 8311. An unused 100MHz reference clock (REFCLK2) is also available from (U12). RefClk routing is laid out as a 100-Ohm, controlled-impedance, microstrip-differential pair. Trace length mismatch within this pair is less than 0.005".

When using the optional on board clock generator R12 and R13 should be removed to ensure that the locally generated clock is not driven to the PCI Express edge connector (P1). In addition, R1 and R2 should be populated to route the on board clock to the PEX 8311.

The components for the on-board PCI Express clock circuitry are not assembled nor do they appear on the BOM. Customers who require this feature must source and assemble the components themselves. PLX takes no responsibility for boards damaged during this operation.

3.4.2 PERST#

PERST# is the fundamental Reset signal to the PEX 8311, from the PCI Express edge connector.

3.4.2.1 Reset Circuitry

The reset pushbutton (SW1) allows the user to force the PEX 8311 PERST# signal low. This causes a full reset of the device and the local bus logic. Pressing the reset button causes LRESET# to be asserted and will cause all EEPROM values to be re-loaded.

Pressing the pushbutton reset will also clear all configuration registers including the PCI Express configuration registers. The PEX 8311 will have to be re-enumerated by the host before it will respond to PCI Express memory transactions.

3.5 LED Indicators

The PEX 8311RDK provides several LED indicators, including power-on indication and programmable PEX 8311 GPIO lane status indication. Table 3-4 provides a quick explanation of each LED indicators.

By default GPIO[3:1] are configured as inputs and pulled high and GPIO0 shows the link status. By changing GPIOCTL[13:12] in the SPI EEPROM (U2) the GPIO lines can be reconfigured to reflect the lower four bits of the LTSSM state machine. See the PEX8311 data book for additional details.

Table 3-4. PEX 8311RDK LED Indicators

Indicator Type	Location	LED ON
Board Power Indication	LED5	PCI Express 12V power on
	LED6	3.3V power is on
	LED8	2.5V power is on
GPIO0	LED1	Output OFF (0) – Link Down ON (1) – Link Up
GPIO1	LED2	ON, GPIO1 = Input by default
GPIO2	LED3	ON, GPIO2 = Input by default
GPIO3	LED4	ON, GPIO3 = Input by default

3.6 PEX 8311RDK Power

The PEX 8311RDK has two sources for DC power. The first source is the card edge connector (P1). This x1 connector provides up to 500 mA at +12VDC, and 3.0A at +3.3VDC. Card edge power is intended to power only PEX 8311RDK components.

The second source, the ATX 4-pin connector (J4), provides +12VDC, and the +5VDC power supplied to the POM connector.

The electronic devices on the RDK require +1.5V, +2.5V, and +3.3V DC power. A 5A LDO regulator (U4) is used to convert the PCI Express +12 VDC to +3.3 VDC, a 2.5A LDO regulator (U9) is used to convert the PCI Express +3.3 VDC to +2.5 VDC and a 250mA regulator (U3) is used to convert the PCI Express +3.3 VDC to +1.5 VDC power for the on board devices. As long as the output current from the voltage converter remains less than the maximum current outputs from the LDOs, the RDK board will function correctly.

3.6.1 PEX 8311 Bridge Device Power

The PEX 8311 bridge device power requires the following:

- VDD Core +1.5 VDC ±10%
- +2.5 VDC ±10%
- VDD I/O +3.3 VDC ±10%

Care must be taken to ensure that the power sequencing requirements of the PEX 8311 are met – please refer to the PEX 8311 data book for further details.

As shipped the absolute maximum current required for the PEX 8311RDK supplies is detailed in Table 3-5.

Table 3-5. PEX 8311RDK Power supply currents

Power Supply	Maximum required by the RDK	Maximum available from the Regulator
+1.5 VDC	240mA	250mA
+2.5 VDC	220mA	2.5A
+3.3 VDC	450mA	5A[1]
Note 1: A maximum of 1.8A is available when U4 is fed from the 12V supply of a 10W PCI Express connector.		

When using the 1.5V supply to provide power to the uncommitted FPGA it may be necessary to change U3 to a larger regulator to ensure sufficient power supply current is available.

3.6.2 PEX 8311 Power Jumpers and Resistor options

Various power jumpers and resistor options are available on the PEX 8311 RDK to allow the power consumption of the PEX 8311 to be measured under different operating conditions.

Table 3-6 details the jumper and resistor settings for the main power options. For the uncommitted FPGA power options please see section 4.4.2.4 Uncommitted FPGA power supplies.

Table 3-6. PEX 8311RDK Power jumper and resistor options

Jumper	Factory Setting	Description
J7	CLOSED	+3.3V supply to PEX 8311
J8	CLOSED	+1.5V supply to PEX 8311
J9	CLOSED	+2.5V supply to PEX 8311
R21	ASSEMBLED	Link PCI Express 12V supply to U4 (+3.3V regulator)
R22	NOT ASSEMBLED	Link ATX (J4) 12V supply to U4 (+3.3V regulator)
R23	ASSEMBLED	U4 (3.3V Regulator) provides +3.3V supply to RDK
R27	NOT ASSEMBLED	PCI Express 3.3V supply (P1) provides +3.3V supply to RDK

3.7 Power Management Signaling

Local devices assert the PMEIN# pin to signal a Power Management event. The PEX 8311 converts the PMEIN# signal to PCI Express Power Management Event (PME) messages. There are no internal events that cause a PME message to be sent upstream.

When the PME message is sent to the host, the **PWRMNGCSR** register *PME Status* bit is set and a 100-ms timer is started. If the status bit is not cleared within 100 ms, another PME message is sent.

When the upstream device is powering down the downstream devices, it first places all devices into the $D3_{hot}$ state. It then sends a PCI Express PME_Turn_Off message. After the PEX 8311 receives this message, it stops sending PME messages upstream. The PEX 8311 then sends a PME_TO_Ack message to the upstream device and places its link into the L2/L3 Ready state. The downstream device is now ready to be powered down. If the upstream device changes the PEX 8311 power state back to D0, PME messages are re-enabled. The PCI Express PME_Turn_Off message terminates at the PEX 8311, and is not communicated to the PCI devices. The PEX 8311 does not issue a PM_PME message on behalf of a downstream PCI device while its upstream link is in the L2/L3 non-communicating state.

To avoid loss of PME# assertions in the conversion of the level-sensitive PMEIN# signal to the edge-triggered PCI Express PM_PME message, the PMEIN# signal is polled every 256 ms by the PEX 8311 and a PCI Express PM_PME message is generated if PME# is asserted.

The PMEIN# signal is used only when the PEX 8311 is in Endpoint Mode.

3.7.1 Wakeup

The PEX 8311 asserts the WAKEOUT# signal or sends a PCI Express beacon for the following:

- PMEIN# pin is asserted while link is in L2 state
- PCI Express beacon is received while link is in L2 state
- PCI Express PM_PME Message is received

A beacon is transmitted if the following are true:

- PMEIN# pin is asserted while link is in L2 state
- **DEVSPECCTL** register *Beacon Generate Enable* bit is set
- **PWRMNGCSR** register *PME Enable* bit is set

The WAKEOUT# signal is used only when the PEX 8311 is in Endpoint mode.

3.8 Endpoint/Root Complex operation

The PEX 8311 RDK has been designed to demonstrate the operation of the PEX 8311 in Endpoint Mode. While the PEX 8311 RDK has not been designed for Root Complex mode operation it is possible to achieve limited Root Complex mode functionality. The following notes indicate how this may be achieved. PLX has not tested operation of the board in Root Complex mode so customers who require this feature do so at their own risk and must source and assemble the components themselves. PLX takes no responsibility for boards damaged during this operation

To operate the PEX 8311 in Root Complex mode the PEX 8311 ROOT_COMPLEX# input should be pulled low by removing R6 and adding R7. In Root Complex mode the local bus of the PEX 8311 will be the upstream bus so some local intelligence will need to be added to act as the system host and enumerate any downstream device. Local intelligence may be added by attaching a suitable processor to either the POM (J3) connector, the test headers (LAH1-6) or by using the prototyping footprints.

When operating in Root Complex mode the internal clock (CLKIN) of the PEX 8311 must be supplied by an external clock source. To use the clock source on the RDK remove R53 and assemble R52, R150, C96, C97 and U13. The maximum operating frequency for U13 should be 66MHz.

As the PEX 8311 is now the upstream device it may be necessary for the PEX 8311 RDK to source the PCI Express clock. This can be achieved by populating the onboard PCI Express clock circuit – see sheet 7 of the schematics. To route the PCI Express clocks to the PEX 8311 remove R12 and R13 and insert R1 and R2.

When operating in Endpoint mode the power for the PEX 8311RDK is normally provided by the PCI Express edge connector. If power is unavailable from this connector other means must be used to provide the +12V and +3.3V required by the board. It is possible to use the ATX connector (J4) to provide +12V to the 3.3V regulator U4 by removing R21 and populating R22 with a 0 ohm jumper. The PCIE3.3VCC can then be provided by U4 by populating R27 with a 0 ohm jumper. Extreme care must be taken to ensure that the power sequencing requirements of the PEX 8311 are still met when using the supplies in this manner. If there is any doubt with regards to power sequencing use one or more of J7, J8 and J9 to provide the supplies to the PEX 8311 from properly sequenced external sources.

The PCI Express edge connector is obviously designed for use in Endpoint mode as an adapter card. A suitable converter will be required to allow other PCI Express devices/cards to be plugged into the RDK. In addition, it may be necessary to provide a downstream PCI Express clock. The spare REFCLK2 may be used for this function although care will be required with regards to the routing of this to the downstream device.

4. Mechanical Architecture

Figure 4-1 illustrates the PEX 8311RDK and component placement.

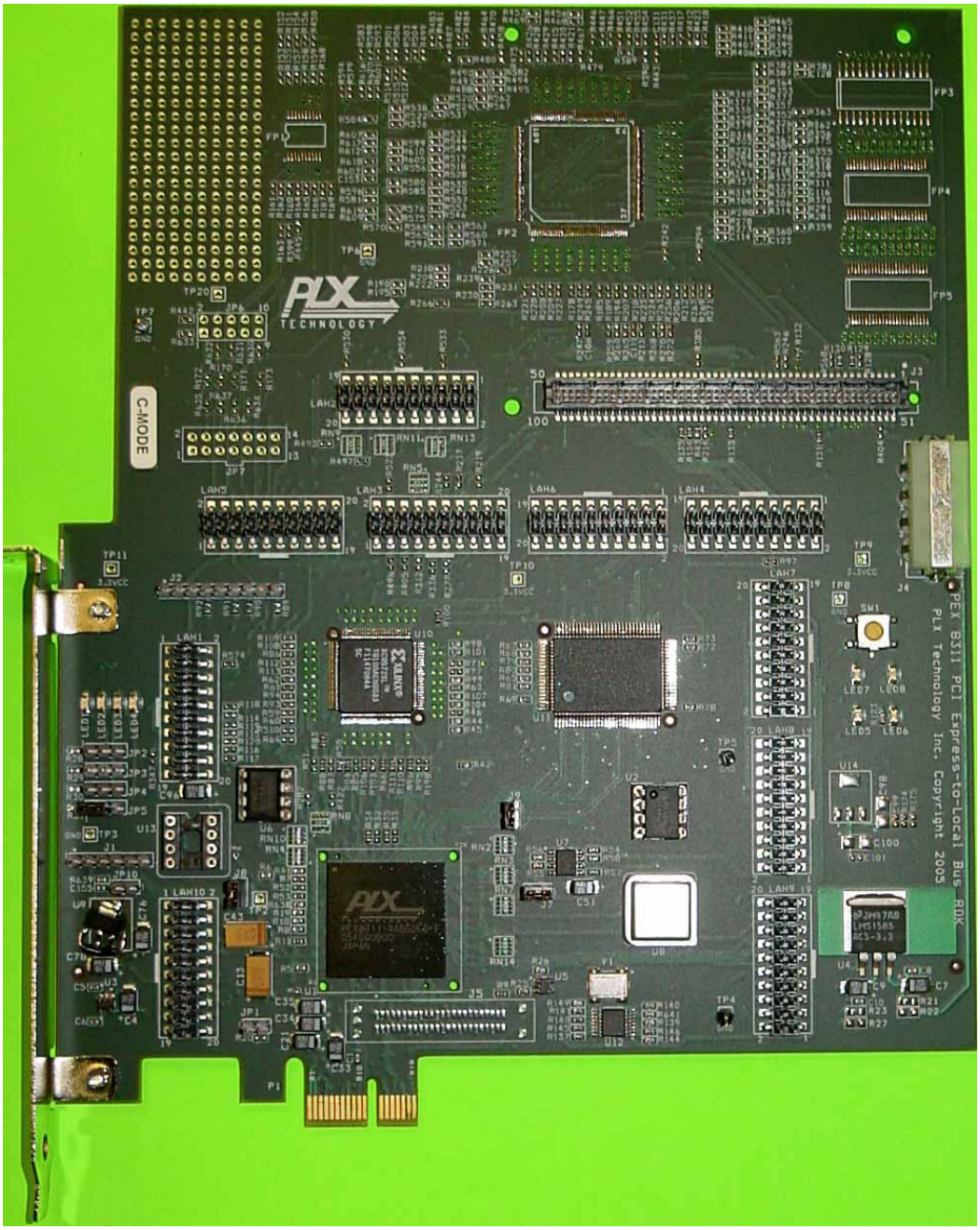


Figure 4-1. PEX 8311RDK Component Placement

The PEX 8311RDK's form factor is based on the PCI Express CEM specification. The board is an eight-layer 6.6"L x 8.15"W PC board. The board height is greater than that noted in the PCI Express CEM specification and care must be taken to ensure that the board will fit within the target PC. It may be necessary to leave the case of the PC open or use an open chassis PC when using the PEX 8311 RDK. If this is the case then appropriate heath and safety measures should be taken when using the system in this manner.

4.1 Monitoring Points, Test headers, Indicators, Control, and DIP Switch Summary

This section summarizes the interfaces available on the PEX 8311RDK for controlling and monitoring PEX 8311 performance.

4.1.1 Monitoring Points

- Six ground test points (TP3-8), are scattered across the PEX 8311RDK to provide probe reference points
- Voltages to the PEX 8311 can be monitored at the following locations:
  - J8 (1.5 VCC)
  - J9 (2.5 VCC)
  - J7 (3.3 VCC)
- Three 3.3 VCC test points (TP9-11), are scattered across the PEX 8311RDK to allow voltage monitoring.
- TP1 is connected to the PEX 8311 PWR_OK output
- TP2 can be used to monitor the PEX8311 internal clock
- External power can be monitored at the ATX connector (J4)
- J1 provides access to the PEX 8311 JTAG port; TCK, TDI, TDO, and TMS
- LAH 1-6 Logic analyzer test headers to connect to monitor local bus activity, see Section 4.1.2.1 Test Headers

4.1.2 Headers

4.1.2.1 Test Headers

The RDK board has six (6) 0.1”, 2x10 logic analyzer headers (LAH1-6) that follow the HP format and can be used for probing or prototype area extension. All PEX 8311 Local Bus signals, configuration and status signals are well arranged within these headers. Headers LAH2 and LAH3 contain Local Bus address signals. Headers LAH4 to LAH6 contain Local Bus data signals. Headers LAH1 and LAH5 contain Local Bus control and status signals. These headers do not provide any power source. Schematic page 5 provides the connector signal details.

4.1.2.2 JTAG Headers

There are two independent JTAG test ports on the PEX 8311 RDK. J1 is a 0.1”, 6 x 1 header which allows access to the PEX 8311 JTAG interface. This can be used to check connectivity of the device and to allow customers to develop their own test programs. With the exception of BSDL models PLX does not provide any additional boundary scan test software for the PEX 8311 or the PEX 8311 RDK.

J2 is a 0.1” 9 x 1 header which is connected directly to the Xilinx CPLD (U10). This header allows the CPLD to be re-programmed by the user at any time. PLX does not provide the programming software or the lead to allow re-programming of the CPLD.

By reprogramming the CPLD the user can change the functionality of the board. However, customers who re-program the CPLD do so at their own risk. PLX takes no responsibility for boards damaged or rendered inoperable while re-programming the CPLD.

4.1.3 Indicators

By default GPIO[3:1] are configured as inputs and pulled high. GPIO0 (and LED0) shows the link status. By changing GPIOCTL[13:12] in the SPI EEPROM (U2) the GPIO[3:0] lines and LED[3:0] can be reconfigured to reflect the lower four bits of the LTSSM state machine. See the PEX8311 data book for additional details.

The other LED's on the PEX 8311 indicate operation of the power supplies as detailed in Table 3-4. PEX 8311RDK LED Indicators

4.1.4 Controls

Table 4-1. PEX 8311RDK Default Jumper Settings

Jumper	Factory Setting	Description
JP1	OPEN	Pull down BAR0ENB# when closed
JP2	OPEN	GPIO0 drives LED1
JP3	1-2	Pull GPIO1 high
JP4	1-2	Pull GPIO2 high
JP5	1-2	Pull GPIO3 high
J7	CLOSED	+3.3V supply to PEX 8311
J8	CLOSED	+1.5V supply to PEX 8311
J9	CLOSED	+2.5V supply to PEX 8311

4.2 PEX 8311RDK Layout Information

4.2.1 Trace Routing Design Rules

The characteristic trace impedances are within the PCI Express specification (100 Ohm ±5%) for the differential, and within the PCI specification (55 Ohm ±10%) for the single-ended.

4.2.2 Power Decoupling

Power decoupling is provided by two means – plane capacitance (provided by the PCB stackup) and discrete decoupling capacitors. Plane capacitance filters noise above approximately 100 MHz. The footprints for the discrete decoupling capacitors are designed such that the inductance between the pad and plane is reduced by careful via placement. (Refer to Figure 4-2. PEX 8311RDK Decoupling Capacitor Footprints)

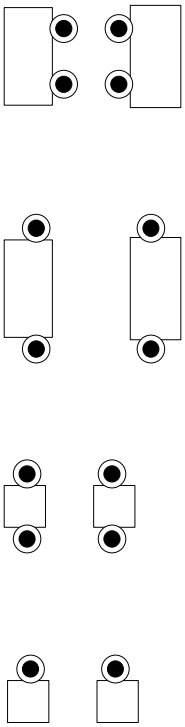


Figure 4-2. PEX 8311RDK Decoupling Capacitor Footprints

4.2.3 PCB Stackup

The PEX 8311RDK is an 8-layer, 60-mil thick PCB. The target signal impedance for all routing layers is 55 Ohms ±10% single-ended impedance and 100 Ohms ±5% differential. Figure 4-3 details the layers used in the PCB manufactuer. The thickness of the various layers is detailed in Table 4-2. Layer thickness.

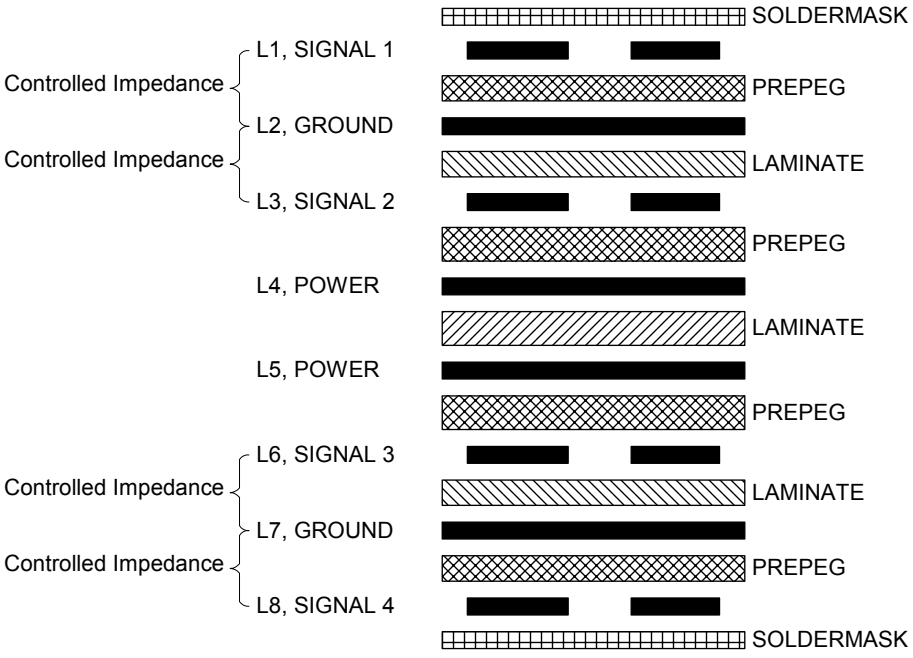


Figure 4-3. PEX 8311RDK Stackup

Table 4-2. Layer thickness

Layer	Type	Thickness (mils)
L1		0.60
	Prepeg	4.00
L2		1.20
	Core	5.00
L3		1.20
	Prepeg	10.00
L4		2.60
	Core	10.00
L5		2.60
	Prepeg	10.00
L6		1.20
	Core	5.00
L7		1.20
	Prepeg	4.00
L8		0.60

4.3 MidBus LAI Footprints

The PEX 8311RDK has one half-size MidBus LAI footprint site (J5), which can be used to probe the high-speed PCI Express serial lanes, or populated with a shroud to allow third-party PCI Express logic analyzers to view the serial data.

The board is not shipped with the shroud assembled nor does the shroud appear on the BOM. Customers who require this feature must source and assemble the shroud themselves. PLX takes no responsibility for boards damaged during this operation.

4.4 Prototyping Area

The RDK board contains a small prototyping area with various surface-mount footprints and a 20 x 10 0.1” pitch through-hole grid.

4.4.1 Surface Mount Footprints

The prototyping area of the PEX 8311 RDK has six (6) surface mount footprints; see Table 4-3 for details.

These footprints can accommodate a variety of devices. Although FP2 is deigned to accommodate FPGA’s other devices may be assembled on this footprint.

Table 4-3. Six (6) Surface Mount Footprints

Package	Qty	Pin Pitch	Schematic Reference	Example Applications
SOT-223	1	0.1”	U14	Voltage Regulator
20-pin SSOP	1	0.05"	FP1	Discrete Logic, Configuration Memory
28-pin SOIC	1	0.05"	FP3	Discrete Logic
48-pin SSOP	2	0.025"	FP4, FP5	Discrete Logic, data transceivers
144-pin PQFP	1	0.5mm	FP2	FPGA’s, CPLDs, TI C542/KC542/LC548/ LC549/VC549, SH7604, IDT RC32364

4.4.2 Uncommitted FPGA footprint

The footprint FP2 has been designed to accept either a 100 pin Altera Cyclone FPGA such as the EP1C3T144 or a 100 pin Xilinx Spartan-3E FPGA. Although care has been taken to ensure that the configurable resistor options and connections comply with these devices it is recommended that the user carefully checks the latest documentation from the FPGA manufacturer in case of product changes subsequent to the publication of this document.

In addition to the devices noted above other parts may also be assembled onto FP2. However, it is up to the user to determine the appropriate connections between the device and the PEX 8311 local bus.

It should be noted that PLX does not provide FPGA code examples. Section 7 - CPLD Verilog Code – details the code which is used in the on board CPLD and this may be used as a guide.

4.4.2.1 Uncommitted FPGA connections

The following modules can be used in conjunction with the uncommitted FPGA footprint:

- Unpopulated configuration Resistors
- Configuration PROM
- JTAG headers
- User VCC
- Through hole pads

Depending on the application one or more of these can be used to interconnect the FPGA to the existing circuitry on the PEX 8311 RDK, to set up FPGA configuration and/or to link to other uncommitted elements on the FPGA

4.4.2.2 Uncommitted FPGA to PEX 8311 local bus

The uncommitted FPGA can be connected to the PEX 8311 local bus in two ways:

a) Using the resistor options
b) Wiring between the through hole pads (PF1 to PF144) and the test headers (LAH1 to LAH6)

Any combination of the above can be used.

Table 4-4 shows the resistor options used to connect the Altera Cyclone or the Xilinx Spartan-3E arrays to the PEX 8311 local bus.

Table 4-4. Uncommitted FPGA resistor configuration

FPGA Pin No.	Xilinx Pin Name	Altera Pin Name	Local Signal	Bus No.	Xilinx link resistor	Xilinx Voltage R	Xilinx Capacitor	Altera link resistor	Altera Voltage R	Altera Capacitor
1	PROG_B	INIT_DON	Note 1	A1	180			User IO		
2	I/O	I/O	LD0	A2	182			182		
3	I/O	I/O	LD1	A3	186			186		
4	I/O	I/O	LD2	A4	191			191		
5	I/O	I/O	LD3	A5	196			196		
6	IP	I/O	LBG1	A6	198			198		
7	I/O	I/O	LD4	A7	200			200		
8	I/O	3.3V	LA2_X	A8	203			176		102
9	1.2V	GND		A9	209	190	103	209	195	
10	IP	I/O	BREQo	A10	214			214		
11	GND	I/O	LA2_A	A11	220	262		219		
12	IP	I/O (nCS0)	LA20	A12	225			225		
13	3.3V	DATA0	USERo	A13	231	201	104	Note 2		
14	I/O	nCONFIG	GPIO0	A14	User IO			234		
15	I/O	1.5V	LA4_X	A15	237			239	210	104
16	I/O	CLK0	LCLK_T	A16	User IO			241		
17	I/O	CLK1	LA5_X	A17	244			NC		
18	IP	GND		A18	User IP			249	235	
19	GND	GND		A19	178	235		178	235	
20	I/O	nCEO	USERi	A20	User IO			Note 2		
21	I/O	nCE	LA6_X	A21	183			Note 2		
22	I/O	MSEL0	LA7_X	A22	187			Note 2		
23	I/O	MSEL1	LA8_X	A23	192			Note 2		
24	IP	DCLK	GPIO1	A24	User IP			Note 2		
25	I/O	I/O	LD5	A25	199			199		
26	I/O	I/O	LD6	A26	202			202		
27	GND	I/O	LA4_A	A27	207	265		205		
28	3.3V	I/O	LA5_A	A28	212	267	112	211		
29	IP	3.3V	LA21_X	A29	216			218	251	107
30	2.5V	GND		A30	224	256	107	223	272	
31	I/O	I/O	LD7	A31	228			228		
32	I/O	I/O	LD8	A32	233			233		
33	I/O	I/O	LD9	A33	236			236		
34	I/O	I/O	LD10	A34	240			240		
35	I/O	I/O	LD11	A35	242			242		
36	IP	I/O	LINTo#	A36	246			246		
37	GND	I/O	LA6_A	B1	278	275		277		
38	IP	I/O	LSERR#	B2	282			282		
39	I/O	I/O	LD12	B3	287			287		
40	INIT_B	I/O	Note 1	B4	292			User IO		
41	IP	I/O	CS_3#	B5	294			294		
42	3.3V	I/O	LA7_A	B6	300	281	115	298		
43	I/O	GND	LA9_X	B7	305			307	291	
44	I/O	3.3V	LA10_X	B8	312			313	354	123
45	1.2V	GND		B9	320	311	116	320	318	
46	GND	1.5V		B10	323	380		323	374	124
47	IP	I/O	LA16	B11	328			328		
48	IP	I/O	LA17	B12	333			333		
49	3.3V	I/O	LA8_A	B13	327		117	336		
50	I/O	I/O	LD15	B14	338			338		

FPGA Pin No.	Xilinx Pin Name	Altera Pin Name	Local Signal	Bus No.	Xilinx link resistor	Xilinx Voltage R	Xilinx Capacitor	Altera link resistor	Altera Voltage R	Altera Capacitor
51	I/O	I/O	LD16	B15	340			340		
52	I/O	I/O	LD17	B16	343			343		
53	I/O	I/O	LD18	B17	346			346		
54	I/O	I/O	LD19	B18	349			349		
55	GND	I/O	LA9_A	B19	344			276		
56	IP	I/O	LA18	B20	279			279		
57	IP	I/O	LA19	B21	283			283		
58	I/O	I/O	LD22	B22	289			289		
59	I/O	I/O	LD23	B23	293			293		
60	I/O	I/O	LD24	B24	295			295		
61	GND	I/O	LA10_A	B25	303	366		301		
62	I/O	I/O	LD25	B26	308			308		
63	DIN	GND	Note 1	B27	315			317	366	
64	3.3V	1.5V		B28	321	368	126	321	376	126
65	2.5V	GND		B29	326	357	121	326	363	
66	I/O	3.3V	LA11_X	B30	329			330	369	127
67	I/O	I/O	LD26	B31	334			334		
68	I/O	I/O	LD27	B32	337			337		
69	IP	I/O	DACK0#	B33	339			339		
70	I/O	I/O	LD28	B34	342			342		
71	CCLK	I/O	Note 1	B35	345			User IO		
72	DONE	I/O	Note 1	B36	347			User IO		
73	GND	I/O	LA11_A	C1	387	384		386		
74	I/O	I/O	LD29	C2	391			391		
75	I/O	I/O	LD30	C3	394			394		
76	I/O	I/O	LD31	C4	397			397		
77	I/O	I/O	ADS#	C5	400			400		
78	IP	I/O	DACK1#	C6	403			403		
79	3.3V	I/O	LA12_A	C7	407	392	129	405		
80	1.2V	GND		C8	410	471	136	411	401	
81	I/O	3.3V	LA15_X	C9	416			417	408	130
82	I/O	I/O	BIGEND#	C10	422			422		
83	I/O	I/O	BLAST#	C11	427			427		
84	IP	I/O	LA31/DT/R#	C12	430			430		
85	I/O	I/O	LA29/ALE	C13	433			433		
86	I/O	CONF_DC	GPIO2	C14	User IO			Note 2		
87	I/O	nSTATUS	GPIO3	C15	User IO			Note 2		
88	I/O	TCK	F_TCK	C16	User IO			442		
89	IP	TMS	F_TMS	C17	User IP			445		
90	GND	TDO	F_TDO	C18	452	455		450		
91	I/O	I/O	BREQi	C19	385			385		
92	I/O	CLK3	LA12_X	C20	388			NC		
93	I/O	CLK2	PMEIN#_X	C21	393			NC		
94	I/O	I/O	BTERM#	C22	396			396		
95	IP	TDI	F_TDI	C23	User IP			399		
96	I/O	I/O	CCS#	C24	402			402		
97	I/O	I/O	DMPAF/EOT	C25	404			404		
98	I/O	I/O	DREQ0#	C26	409			409		
99	GND	I/O	LA13_A	C27	415	474		413		
100	3.3V	I/O	LA14_A	C28	420	480	139	419		

FPGA Pin No.	Xilinx Pin Name	Altera Pin Name	Local Signal	Bus No.	Xilinx link resistor	Xilinx Voltage R	Xilinx Capacitor	Altera link resistor	Altera Voltage R	Altera Capacitor
101	IP	GND	LA22_X	C29	424			426	475	
102	2.5V	3.3V		C30	429	463	134	428	481	140
103	I/O	I/O	DP0	C31	432			432		
104	I/O	I/O	DP1	C32	435			435		
105	I/O	I/O	DP2	C33	438			438		
106	I/O	I/O	DP3	C34	441			441		
107	IP	I/O	LA30/DEN#	C35	444			444		
108	TMS	I/O	LA3_A	C36	172			449		
109	TDO	I/O	LA15_A	D1	171			493		
110	TCK	I/O	LA21_A	D2	170			497		
111	IP	I/O	LA23	D3	502			502		
112	I/O	I/O	DREQ1#	D4	507			507		
113	I/O	I/O	LBR1	D5	510			510		
114	IP	I/O	LA24	D6	513			513		
115	1.2V	3.3V		D7	520	509	142	520	501	142
116	I/O	GND	LA13_X	D8	523			524	598	
117	I/O	1.5V	LA14_X	D9	530			532	536	143
118	GND	GND		D10	538	547		537	620	
119	IP	I/O	LA25	D11	542			542		
120	IP	I/O	LA26	D12	548			548		
121	3.3V	I/O	LA22_A	D13	562		144	554		
122	I/O	I/O	LD13	D14	558			558		
123	I/O	I/O	LINTi#	D15	563			563		
124	I/O	I/O	LRESET#	D16	568			568		
125	I/O	I/O	LBE0#	D17	573			573		
126	I/O	I/O	LBE1#	D18	578			578		
127	GND	I/O		D19	594			User IO		
128	GCLK8	I/O	LCLK_T	D20	496			User IO		
129	IP	I/O		D21	User IP			User IO		
130	I/O	I/O	LW/R#	D22	505			505		
131	I/O	I/O	LD14	D23	508			508		
132	I/O	I/O	READY#	D24	511			511		
133	GND	I/O	LA28_A	D25	518	615		516		
134	I/O	I/O	WAIT#	D26	521			521		
135	I/O	1.5V	LA3_X	D27	526			528	605	150
136	IP	GND	LA28_X	D28	533			534	621	
137	2.5V	3.3V		D29	540	585	146	540	580	146
138	3.3V	GND		D30	545	603	153	545	618	
139	I/O	I/O	LD20	D31	551			551		
140	I/O	I/O	LD21	D32	555			555		
141	IP	I/O	LA27	D33	559			559		
142	I/O	I/O	LBE2#	D34	564			564		
143	I/O	I/O	LBE3#	D35	569			569		
144	TDI	I/O	PMEIN#_A	D36	173			574		

Notes:

1) The resistors used for the Xilinx programming pins will depend on the programming method used. Refer to Table 4-6, Table 4-8 and Table 4-9 for further details.
2) The resistors used for the Altera programming pins will depend on the programming method used. Refer to Table 4-5, Table 4-7 for further details.

With the exception of the resistors noted in Table 4-5, Table 4-6, Table 4-7, Table 4-8 and Table 4-9 the resistor value will normally be 0 ohms.

Depending on the I/O of the FPGA some additional signal noise may be seen. If this is the case then the value of the resistors used to link to the local bus signals may be increased to form a series termination resistor. The value required will depend on the loading but will typically be in the range of 30 to 100 ohms.

The power supplies for the FPGA's normally require 2 resistors to be populated. One resistor is used to link the FPGA to a Vx bus (see the "…Link Resistor" column) and the second resistor is used to select the appropriate voltage (see the "…voltage R" column.

In addition to the resistors it is recommended that the appropriate decoupling capacitor noted in the "…Capacitor" column is also assembled. The value required will be FPGA specific but is typically 10nF.

4.4.2.3 Programming the uncommitted FPGA

There are three methods of programming or configuring the uncommitted FPGA:

a) Program through the JTAG interface
b) Program using the PEX 8311 GPIO
c) Program using the Configuration PROM

Of the above options (a) and (b) are available for both the Altera and Xilinx devices. Option (c) is only available for the Xilinx device.

4.4.2.3.1 Programming the FPGA through the JTAG interface

Table 4-5 shows the resistor options and jumpers used to connect the 0.1", 1 x 10 header JP6 to an Altera Cyclone array. JP6 can be used with programmers from Altera such as the ByteBlaster II, MasterBlaster etc.

Depending on the programmer used pins 4 and 10 of JP6 may need to be pulled to the appropriate voltage, see notes 1 and 2 below and the appropriate Altera documentation.

Table 4-5. Altera Uncommitted FPGA JTAG interconnections

FPGA JTAG program option	Connector [pin]	JTAG signal	Link Resistor (value)	FPGA signal [pin]	Pull-up resistor or jumper	Pull-down resistor or jumper
Altera FPGA using ByteBlaster II, MasterBlaster or ByteBlas 10 pin header.	JP6 [1]	F_TCK	R442 (0)	TCK [88]	-	R637 (10K)
	JP6 [2]	GND	-	-	-	-
	JP6 [3]	F_TDO	R450 (0)	TDO [90]	-	-
	JP6 [4]	VCC[1]	-	-	-	-
	JP6 [5]	F_TMS	R445 (0)	TMS [89]	R631 (10K)	-
	JP6 [6]	VIO (3.3V)	-	-	-	-
	JP6 [7]	NC	-	-	-	-
	JP6 [8]	NC	-	-	-	-
	JP6 [9]	F_TDI	R399 (0)	TDI [95]	R630 (10K)	-
	JP6 [10]	NC[2]	-	-	-	-
	-	-	R185 (0)	nCE [21]	-	R250 (0)
	-	-	R439 (0)	nSTATUS [87][3]	JP5 [1-2] or JP5 NC + R117 (10K)	-
	-	-	R436 (0)	CONF_DONE [86][4]	JP4 [1-2] or JP4 NC + R116 (10K)	-
	-	-	R234 (0)	nCONFIG [14][5,6]	JP2 [1-2] or JP2 NC + R114 (10K)	-
	-	-	R189 (0)	MSEL0 [22] [5]	-	R250 (0)
	-	-	R194 (0)	MSEL1 [23] [5]	-	R250 (0)
	-	-	R230 (0)	DATA0 [13] [5]	-	R266 (0)
	-	-	R197 (0)	DCLK [24] [5,7]	-	JP3 [2-3]

Notes:

1) This pin is connected to TP20. Connect this pin to the same supply voltage as the download cable.
2) For some programmers it may be necessary to tie this pin to GND.
3) nSTATUS is connected to GPIO3. During configuration ensure that GPIO3 is an input. This is the default condition for GPIO3.
4) CONF_DONE is connected to GPIO2. During configuration ensure that GPIO2 is an input. This is the default condition for GPIO2.
5) The connections for these pins assume only JTAG configuration is being used. When supporting non-JTAG configuration schemes see section 4.4.2.3.2.
6) nCONFIG is connected to GPIO0. The low to high transition begins configuration. If GPIO0 is programmed to be an output configuration can be enabled using this signal.
7) DCLK is connected to GPIO1. When JP3 is in position 2-3 GPIO1 is strapped to GND and must always be configured as an input.

In addition to the above resistors the appropriate power supply and ground resistors must also be populated.

Table 4-6 shows the resistor options and jumpers used to connect the 14 pin Target Interface connector (e.g. Molex part no. 87831-1420) JP7 to an Xilinx Spartan-3E array. JP7 can be used with appropriate programmers from Xilinx to configure the device using the JTAG interface.

Table 4-6 also assumes that JP7 is connected directly to the Xilinx FPGA. It is also possible to create a scan chain with the configuration PROM (FP1) if used. This is detailed further in section 4.4.2.3.3.

Depending upon the device, care should be taken with HSWAP_EN (pin 143). This pin configures the internal pull-up resistors. By default pin 143 will be connected to LBE3# (via R569) and is pulled high using RN2. This will disable the internal pull-ups. If the internal pull-ups are required this pin needs to be pulled low using R571 and R597.

Table 4-6. Xilinx Uncommitted FPGA JTAG interconnections

FPGA JTAG program option	Connector [pin]	JTAG signal	Link Resistor (value)	FPGA signal [pin]	Pull-up resistor or jumper	Pull-down resistor or jumper
Xilinx Spartan-3E array using 14 pin Target Interface Connector	JP7 [2]	Vref (2.5V)	-	-	-	-
	JP7 [4]	F_TMS	R172 (100Ω)[1]	TMS[108]	-	-
	JP7 [6]	F_TCK	R170 (100Ω)[1]	TCK [110]	-	-
	JP7 [8]	F_TDO	R171 (0)[1]	TDO [109]	-	-
	JP7 [10]	F_TDI	R173 (100Ω)[1]	TDI [144]	-	-
	JP7 [12,14]	NC	-	-	-	-
	JP7 [1,3,5,7,9, 11,13]	GND	-	-	-	-
	-	-	R180 (0 or 56 Ω)[1,2]	PROG_B [1]	JP5 [1-2] or JP5 NC	-
	-	-	R348 (0)	DONE [72]	R358 (330 Ω)[3]	-
	-	-	R292 (0)	INIT_B [40]	JP4 [1-2] or JP4 NC + R116 (4K7)[4]	R250 (0)
	-	-	R309 (0)	M0 [62]	R368 (10K)	-
	-	-	R297 (0)	M1 [60]	-	R361 (10K)
	-	-	R284 (0)	M2 [57][5]	-	R367 (10k)

Notes:

1) The value of the series current limiting resistor may vary depending on the programmer and the programming voltage used. If using 3.3V programming then 56Ω is typically used. Refer to the appropriate Xilinx application notes for further information.
2) PROG_B is connected to GPIO3. GPIO3 is an input by default.
3) The resistor options shown pull DONE to 3.3V. Depending on the programming option selected DONE can be pulled to 2.5V using R358.
4) INIT_B is connected to GPIO2. GPIO2 is an input by default.
5) If this pin is connected to LA19 through R283 then R284 and R367 are not required as this pin is pulled high using RN11.

In addition to the above resistors the appropriate power supply and ground resistors must also be populated.

4.4.2.3.2Programming the FPGA through the GPIO

Table 4-7 shows the resistor options and jumper configurations required to interface the Altera cyclone FPGA programming pins to the PEX 8311 GPIO pins. The FPGA may then be configured by sending appropriate commands and data through the PEX 8311 GPIO to the FPGA programming pins.

It should be noted that PLX does not provide software to program the FPGA. The SDK shipped with the PEX 8311 RDK provides .api calls to allow access to and changing of the GPIO pins. It is up to the user to develop software to program the FPGA used in their design.

Table 4-7 assumes that programming of the Altera FPGA uses the Passive Serial Configuration method.

Table 4-7. Programming the Altera Uncommitted FPGA through the GPIO

PEX 8311 signal	Link Resistor (value)	FPGA signal [pin]	Pull-up resistor or jumper	Pull-down resistor or jumper
USERo	R229 (0)	DATA0 [13]	-	-
GPIO0	R234 (0)	nCONFIG [14]	JP2 NC + R114[1]	-
GND	R185 (0)	nCE [21]	-	R250 (0)
VCC	R188 (0)	MSEL0 [22] [2]	R254 (0)	-
GND	R194 (0)	MSEL1 [23]	-	R250 (0)
GPIO1	R197 (0)	DCLK [24]	JP3 NC[3]	-
GPIO2	R436 (0)	CONF_DONE [86]	JP4 NC + R116 (10K)	-
GPIO3	R439 (0)	nSTATUS [87]	JP5 NC + R117 (10K)	-

Notes:

1) Depending on the device used, the pull-up R114 may not be required. GPIO0 should be configured to be an output.
2) For some devices MSEL0 should be pulled to ground. If this is required remove R254 and add R264
3) GPIO1 must be configured to be an output.

In addition to the above resistors the appropriate power supply and ground resistors must also be populated.

Table 4-8 shows the resistor options and jumper configurations required to interface the Xilinx Spartan-3E FPGA programming pins to the PEX 8311 GPIO pins. The FPGA may then be configured by sending appropriate commands and data through the PEX 8311 GPIO to the FPGA programming pins.

It should be noted that PLX does not provide software to program the FPGA. The SDK shipped with the PEX 8311 RDK provides .api calls to allow access to and changing of the GPIO pins. It is up to the user to develop software to program the FPGA used in their design.

Table 4-8 assumes that programming of the Xilinx FPGA uses the Slave Serial Configuration method.

Depending upon the device, care should be taken with HSWAP_EN (pin 143). This pin configures the internal pull-up resistors. By default pin 143 will be connected to LBE3# (via R569) and is pulled high using RN2. This will disable the internal pull-ups. If the internal pull-ups are required this pin needs to be pulled low using R571 and R597. If HSWAP_EN needs to be pulled low and LBE3# is required then connect R571 (0) and R597(4K7) and lift pin 4 or pin 5 of RN2.

Depending on the device and power supplies used it may be necessary to add a resistor from the 2.5V rail to ground to manage reverse current. Typically this resistor would be 118Ω or 110Ω and would only be required if the 2.5V supply for the FPGA was sourced from the USRVCC – see the Xilinx application notes for further details regarding reverse currents.

Table 4-8. Programming the Xilinx Uncommitted FPGA through the GPIO

PEX 8311 signal	Link Resistor (value)	FPGA signal [pin]	Pull-up resistor or jumper	Pull-down resistor or jumper
GPIO3	R180 (56 Ω)	PROG_B [1]	JP5 NC	-
USERi	R347 (0)	DONE [72]	R348 (0) + R358 (330 Ω) [1]	-
GPIO2	R292 (0)	INIT_B [40]	JP4 NC + R116 (4K7)	-
VCC	R309 (0)	M0 [62]	R368 (10K)	-
VCC	R297 (0)	M1 [60]	R350 (10K)	-
VCC	R284 (0)	M2 [57] [2]	R367 (10K)	-
GPIO1	R315 (0)	DIN [63]	JP3 NC	-
GPIO0	R345 (56 Ω)	CCLK [71]	JP2 NC	-

Notes:

1) R348 and R353 are only required if BitGen option DriveDONE = No – see the appropriate Xilinx data sheet for more details. Ideally pin 3 or pin 6 of RN10 should be lifted if R348 and R353 are used.
2) If LA19 is connected to this pin through R283 then R284 and R367 are not required as this pin is pulled high using RN11.

In addition to the above resistors the appropriate power supply and ground resistors must also be populated.

4.4.2.3.3 Programming the uncommitted FPGA from the configuration PROM

Xilinx FPGA's can be configured using Platform Flash In-System Programmable Configuration PROMs. FP1 is designed to accept the VO20/VOG20 packaged versions of the XCFxxS platform flash PROMs.

Table 4-9 details the resistor configurations required to interface a platform flash assembled on FP1 to a Xilinx Spartan-3E array assembled on FP2.

It also details the resistor options for connecting the platform flash JTAG interface to JP7 to allow the platform flash to be programmed using the JTAG interface. JP7 is the 14 pin Target Interface connector (e.g. Molex part no. 87831-1420) and can be used with appropriate programmers from Xilinx to configure the device using the JTAG interface.

The programming method detailed in Table 4-9 is master serial mode. Other programming modes may also be selected using the appropriate resistor options. The JTAG TDO output from the platform flash is routed to the TDI input of the Xilinx FPGA. If the JTAG interface is not required the resistors marked with a † in Table 4-9 may be removed.

Depending on the device and power supplies used it may be necessary to add a resistor from the 2.5V rail to ground to manage reverse current. Typically this resistor would be 118Ω or 110Ω and would only be required if the 2.5V supply for the FPGA was sourced from the USRVCC – see the Xilinx application notes for further details regarding reverse currents.

Table 4-9. Platform Flash to Xilinx interconnect

Connector [pin]	JTAG Signal	Plaftorm Flash Signal [pin]	Link Resistor (value)	FPGA signal [pin]	Pull-up resistor or jumper	Pull-down resistor or jumper
JP7 [2]	Vref (2.5V)	-	-	-	-	-
JP7 [4]	F_TMS	TMS [5]	R164 (0)	-	-	-
JP7 [6]	F_TCK	TCK [6]	R165 (0)	-	-	-
JP7 [8]	F_TDO	-	R171 (0) †	TDO [109]	-	-
JP7 [10]	F_TDI	TDI [4]	R163 (0)	-	-	-
JP7 [12,14]	NC	-	-	-	-	-
JP7 [1,3,5,7,9, 11,13]	GND	-	-	-	-	-
-	-	D0 [1]	R161 (0)	DIN [63]	-	-
-	-	CLK [3]	R162 (0)	CCLK [71]	-	-
-	-	CF# [7]	R166 (0)	PROG_B [1]	JP5 NC + R180 (0) +R117 (4K7) [1]	-
-	-	OE/RESET# [8]	R167 (0)	INIT_B [40]	JP4 NC + R292 (0) +R116 (4K7) [2]	
-	-	CE# [10]	R169 (0)	DONE [72]	R348 (0) + R358 (330 Ω) [3]	
-	-	GND [11]	R168 (0)	-	-	
-	-	TDO [17]	R159 (56 Ω) †,5	TDI [144]	-	-
-	-	VCCINT [18]	R157 (0)	-	-	-
-	-	VCCO [19]	R154 (0) [4]	-	-	-
-	-	VCCJ [20]	R151(0) [4]	-	-	-
JP7 [6]	F_TCK	TCK [6]	R170 (56 Ω) †	TCK [110]		
JP7 [4]	F_TMS	TMS [5]	R172 (56 Ω) †	TMS[108]		
			R309 (0)	M0 [62]	-	R379 (10K)
			R297 (0)	M1 [60]	-	R361 (10K)
			R284 (0)	M2 [57]	-	R375 (10K)

Notes:

1) If GPIO3 is to be used JP5 can be connected to position [1-2]. Care must be taken to avoid accidentally placing the FPGA into programming mode or resetting the device.
2) If GPIO2 is to be used JP4 can be connected to position [1-2]. Care must be taken to avoid accidentally placing the FPGA into programming mode or resetting the device.
3) R348 and R353 are only required if BitGen option DriveDONE = No – see the appropriate Xilinx data sheet for more details. Ideally pin 3 or pin 6 of RN10 should be lifted if R348 and R353 are used.
4) R154 and R151 are used when 3.3V programming is required. Other programming voltages are possible but will require pull's on the Xilinx array to be modified appropriately. See the Xilinx data sheets for further details.
5) If the Xilinx FPGA is not linked to the scan chain then remove R159 and add R158 (0). This will link the TDO of the Platform Flash to the JTAG connector TDO pin (F_TDO).

As noted above, in Table 4-9 the JTAG TDO output from the platform flash is routed to the TDI input of the Xilinx FPGA i.e. the Program Flash is the first device in the chain. The scan chain can also be configured so that Xilinx device is the first device in the chain by removing R159, R163 and R171 and populating R158 (0), R160 (0) and R173 (56 Ω).

4.4.2.4 Uncommitted FPGA power supplies

The device mounted onto FP2 may require a voltage level not provided by the voltage regulators assembled on the RDK. To accommodate this, the uncommitted USRVCC circuit can be populated with an appropriate voltage regulator.

Although the schematics show U14 to be a 2.5V regulator any comparable regulator which can fit the SOT-223 layout can be used.

The uncommitted regulator can be fed from either the PCIE3.3VCC rail (populate R175) or from the 5V supply provided by the ATX connector J4 (populate R174).

The uncommitted USRVCC could also be used to provide an additional 1.5VCC as there is relatively little spare current available from U3.

It should be noted that not all power rails are available for all the Vx bus resistor options associated with FP2 and it may be necessary to wire directly from the regulator to the appropriate PFx hole under some circumstances.

4.4.2.5 Uncommitted FPGA Pull-ups/downs

Many of the pins associated with the uncommitted FPGA footprint can be pulled high or low. These pulls are set up using the appropriate resistor to link to a Vx bus and then selecting the voltage the pin should be pulled to using a second resistor.

FPGA pins which are connected to LA or control pins of the PEX 8311 will not normally require additional pulls as these are already pulled to the correct value – see sheet 3 of the schematics.

4.4.2.6 Increasing the number of unused uncommitted FPGA I/O

The vast majority of the I/O of the FPGA's are used in connecting to the PEX 8311. The settings detailed in section 4.4.2.2 show the FPGA connected to the PEX 8311 in C mode using a 32 bit data bus. In addition every feature of the PEX 8311 is connected to the FPGA.

For some applications more FPGA I/O will be required for user circuitry attached to the FPGA. There are several ways in which additional I/O can be released:

1) C mode of J mode
   When operating in C mode both the address and data buses have to be routed to the FPGA. If the board is re-configured to operate in J mode (see section 5) those signals which were previously allocated to the LA bus are no longer required and can be used as additional I/O.

2) Data bus width
   The data bus is currently configured to be a 32 bit bus. The LBRDx registers can be reconfigured to allow operation in 8 or 16 bit mode, thereby releasing the I/O which are connected to the unused data lines.

   It may be useful to only change LDRD1 to a different bus width. This will allow 32 bit accesses to the SBSRAM using local address space 0.

   It should be noted that if the FPGA is to access any of the PEX 8311 registers that access must be a 32 bit wide access so reducing the bus width is really only a solution for slave designs.

3) Bus Mastering or Slave only designs
   If the FPGA is only going to be used as a slave device then it may not be necessary to link all of the local bus control signals to the FPGA.

4) Address bus subset
   CS3# is routed to the FPGA and can be used as a chip select for the device. If only a small number of addresses are going to be decoded by the FPGA the upper portion of the LA bus can be left unconnected releasing FPGA I/O.

5. RDK Mode Configuration

The RDK hardware's Processor/Local Bus is pre-configured for non-multiplexed data and address (C Mode) Processor/Local Bus operation. It can be reconfigured for multiplexed data and address Processor/Local Bus operation (J Mode). Several resistors configure the RDK hardware's Processor/Local Bus for C or J Mode. The specific resistors to install and remove for each mode are detailed in Table 5-1. ('X' means installed; no 'X' means removed.)

Table 5-1. RDK Board Mode Configuration

Resistors	Value	C Mode (Default)	J Mode
Mode Pins Configuration			
R32	1/10w, 10K ohm, 5%		X
R33	1/10w, 10K ohm, 5%		
R34	1/10w, 0 ohm, 5%	X	
R35	1/10w, 0 ohm, 5%	X	X
Data/Address Pins Configuration			
R74	1/10w, 0 ohm, 5%	X	
R75	1/10w, 0 ohm, 5%		X
R76	1/10w, 0 ohm, 5%	X	
R77	1/10w, 0 ohm, 5%		X
R84	1/10w, 0 ohm, 5%	X	
R85	1/10w, 0 ohm, 5%		X
R87	1/10w, 0 ohm, 5%		X
R88	1/10w, 0 ohm, 5%	X	
R93	1/10w, 0 ohm, 5%		X
R94	1/10w, 0 ohm, 5%	X	
R95	1/10w, 0 ohm, 5%		X
R96	1/10w, 0 ohm, 5%	X	
R97	1/10w, 0 ohm, 5%		X
R100	1/10w, 0 ohm, 5%	X	
R103	1/10w, 0 ohm, 5%		X
R106	1/10w, 0 ohm, 5%	X	
R108	1/10w, 0 ohm, 5%		X
R109	1/10w, 0 ohm, 5%	X	
R110	1/10w, 0 ohm, 5%		X
R111	1/10w, 0 ohm, 5%	X	
R112	1/10w, 0 ohm, 5%		X
R113	1/10w, 0 ohm, 5%	X	
LA29/ALE			
R50	1/10w, 10K, 5%	X	
R51	1/10w, 4.7K ohm, 5%		X

6. Examples of Testing the OnBoard 32Kx32 SBSRAM with PLXMon

1) Single read/write from/to on board SBSRAM

   a) At the lower command line window of PLXMon, type in the following commands to perform single 32bit, 16bit and 8bit memory read/write transfers from/to the on board SBSRAM.
   dl s0 1
   <= read one 32-bit long word from address s0
   el s0 88888888
   <= write 32-bit data, 88888888h, to address s0
   dw s0 1
   <= read one 16-bit word from address s0
   ew s0 8888
   <= write 16-bit data, 8888h, to address s0
   db s0 1
   <= read a byte from address s0
   eb s0 88
   <= write 8-bit data, 88h, to address s0

2) DMA burst read/write from/to on board SBSRAM:

   a) At the lower pane of the PLXMon, type **Vars** to obtain the addresses for HBuf, 60K-byte DMA scratch buffer located in the PC's main memory. For example, assume the HBuf has physical address starting at 01F80000h.

   b) Enter 8 long words of test data to the SBSRAM. For example,
   el s0 11111111
   el s0+4 22222222
   el s0+8 33333333
   el s0+c 44444444
   el s0+10 55555555
   el s0+14 66666666
   el s0+18 77777777
   el s0+1c 88888888

   c) Click the DMA button on PLXMon to open the DMA registers window.

   d) Configure DMA CH0 for burst transfer and the transfer direction is from Local-to-PCI. The settings on DMA channel 0 would be similar to the following
   Mode (80h): 143
   PCI address (84h):**01F80000**
   Local address (88h):00000000
   Transfer size (8ch):100
   Descriptor pointer (90h):8
   Check the box for data transfer enable

   e) Click on the [Start Transfer] button to transfer data from on Board SBSRAM to DMA scratch buffer.

   f) Compare the data from step 'b' by typing the **dl HBuf** commend.

   g) Change the contents of the DMA scratch buffer
   el HBuf99999999
   el HBuf+488888888
   el HBuf+877777777
   el HBuf+c66666666
   el HBuf+1055555555
   el HBuf+1444444444
   el HBuf +1833333333
   el HBuf+1c22222222

h) Change the direction of the DMA transfer to PCI-to-Local for DMA CH0, by modifying the Descriptor Pointer (90h) value from 8 to 0.

i) Click the [Start Transfer] button to perform a DMA transfer again

j) Type in **dl s0** to compare the data from step G.

7. CPLD Verilog Code

7.1 Verilog Code

```
//============================================================
//
//   8/8/2005
//
//   Synchronous SRAM controller for PLX PEX 8311 mode C and J.
//   128K byte (32K x 32 bit) synchronous SRAM is used.
//   The memory map for the sync. SRAM is 0000_0000 - 0001_FFFFh.
//   A partial memory decode is used. The decode is only involved
//   address lines A31 to A28 (or A31-A29 and LD28 in J mode)
//
//
//============================================================
`timescale 1ns/100ps

module sramctr82xx ( clk,adsn,blastn,lwdrdn,lhold,lbr,lben,adds_in,adds_4msb,
                     readyn,btermn,sramcsn,sramoen,lholda,lbg,sram_adds,
                     sram_bwn,csn);

    input    clk,adsn,blastn,lwdrdn,lhold;
    input   [1:0]    lbr;
    input   [3:0]    lben;
    input   [9:2]    adds_in;
    input   [31:28]  adds_4msb;

    output    readyn,btermn,sramcsn,sramoen,lholda;
    output [1:0]    lbg;
    output [9:2]    sram_adds;
    output [3:0]    sram_bwn;
    output [3:0]    csn;

    reg     [9:2]    sram_adds;
    reg     [1:0]    lbg;
    reg              sramcsn,sramoen,lholda;
    tri   readyn,btermn;

    // internal veriables

    reg    [3:0]    a31_28;
    reg[1:0]   state;
    reg   oer,oeb;

    BUFE tt1(.O(readyn),.E(!oer),.I(oer));
    BUFE tt2(.O(btermn),.E(!oeb),.I(oeb));

    // chip selects
    // Four uppermost address lines, A31-A28, are used to generate four
    // chip select signals for the board. They are CS[3:0] with addresses
    //
    //  csn_0: 1000_0000h
    //  csn_1: 2000_0000h
    //  csn_2: 3000_0000h
    //  csn_3: 4000_0000h


    wire [3:0] csn = (adds_4msb == 4'b0001) ? 4'b1110:
   (adds_4msb == 4'b0010) ? 4'b1101:
```

```
(adds_4msb == 4'b0011) ? 4'b1011:
(adds_4msb == 4'b0100) ? 4'b0111: 4'b1111;

// byte enable encode for SRAM write cycles

wire [3:0] sram_bwn =({lwdrdn,a31_28}=='b1_0000)
   ? lben[3:0] : 4'b1111;

// store the upper address LA31 - LA28

always @ (posedge clk)

   if (!adsn & (adds_4msb==4'b0000))
       a31_28[3:0] <= adds_4msb[31:28];


// SRAM control state machine
parameter s0=2'b00, s1=2'b01, s2=2'b10, s3=2'b11;

always @ (posedge clk)

    casex (state)
        s0: begin
                sramoen <=1;
    oeb <='b1;
                if (!adsn && !adds_4msb)
                    begin
            sram_adds[9:2] <= adds_in[9:2];
      sramcsn <= 0;
      if (lwdrdn)
          oer <= 'b0;
      else
     oer <= 'b1;
 state <= s1;
                    end
                else
                    begin
                        oer <= 'b1;
                        sramcsn <= 1;
                        state <= s0;
                    end

            end




        s1: if (lwdrdn && (!blastn))
                begin
        sram_adds[9:2] <=sram_adds[9:2]+1;
  sramoen <=1;
  sramcsn <=1;
  oer <='b1;
  oeb <='b1;
  state <= s0;
                end
            else    if (lwdrdn && blastn)
                        begin
      if (sram_adds[9:2]== 'hfe)
```

```
          begin
        oeb <='b0;
              sram_adds[9:2] <= sram_adds[9:2]+1;
              state <= s3;
                end
     else
           begin
        sram_adds[9:2] <= sram_adds[9:2]+1;
        sramoen <=1;
        sramcsn <=0;
        oer <='b0;
        oeb <='b1;
        state <=s1;
            end
                        end
                    else
       begin
     sram_adds[9:2] <=sram_adds[9:2]+1;
     sramoen <=0;
     sramcsn <=0;
     oer <='b0;
     oeb <='b1;
              state <= s2;
                        end



         s2: if ((!lwdrdn) && (!blastn))
     begin
         sramoen <=1;
   sramcsn <=1;
         oer <='b1;
         oeb <='b1;
         state <=s0;
     end
else
     begin
        if (sram_adds[9:2]=='hff)
            begin
    oeb <='b0;
    sram_adds[9:2] <= sram_adds[9:2]+1;
          state <=s3;
      end
 else
     begin
                             sram_adds[9:2] <= sram_adds[9:2]+1;
                             sramoen <=0;
    sramcsn <=0;
    oer <='b0;
          oeb <='b1;
          state <=s2;
      end
     end




          s3: begin
```

```
        sramcsn <=1;
  oer <='b1;
  oeb <='b1;
  state <=s0;
    end

            default: state <=s0;
        endcase

    always @(posedge clk)

        begin
if (lhold)
    lholda <= lhold;
else
    lholda <= 0;

if (!lhold && lbr[1])
    lbg[1] <= lbr[1];
else
    lbg[1] <= 0;

if (!lhold && !lbr[1] && lbr[0])
    lbg[0] <= lbr[0];
else
    lbg[0] <= 0;
        end

endmodule
```

8. References

The following is a list of documentation to provide further details.

- PLX Technology, Inc.
  870 Maude Ave.
  Sunnyvale, CA 94085 USA
  Tel: 408-774-9060
  Tel: 800-759-3735
  Fax: 408 774-2169
  http://www.plxtech.com
  - *PEX 8311 Data Book, Version xx or higher*
  - *PEX 8311RDK Hardware Reference Manual*

- PCI Special Interest Group (PCI-SIG)
  5440 SW Westgate Drive #217
  Portland, OR 97221 USA
  Tel: 503-291-2569
  Fax: 503-297-1090
  http://www.pcisig.com
  - *PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a*
  - *PCI Express-to-PCI Bridge Specification 1.0*

9. Bill of Materials / Schematics

The following pages contain the PEX 8311RDK bill of materials and schematics.

Table 9-1. PEX 8311RDK Bill Of Materials

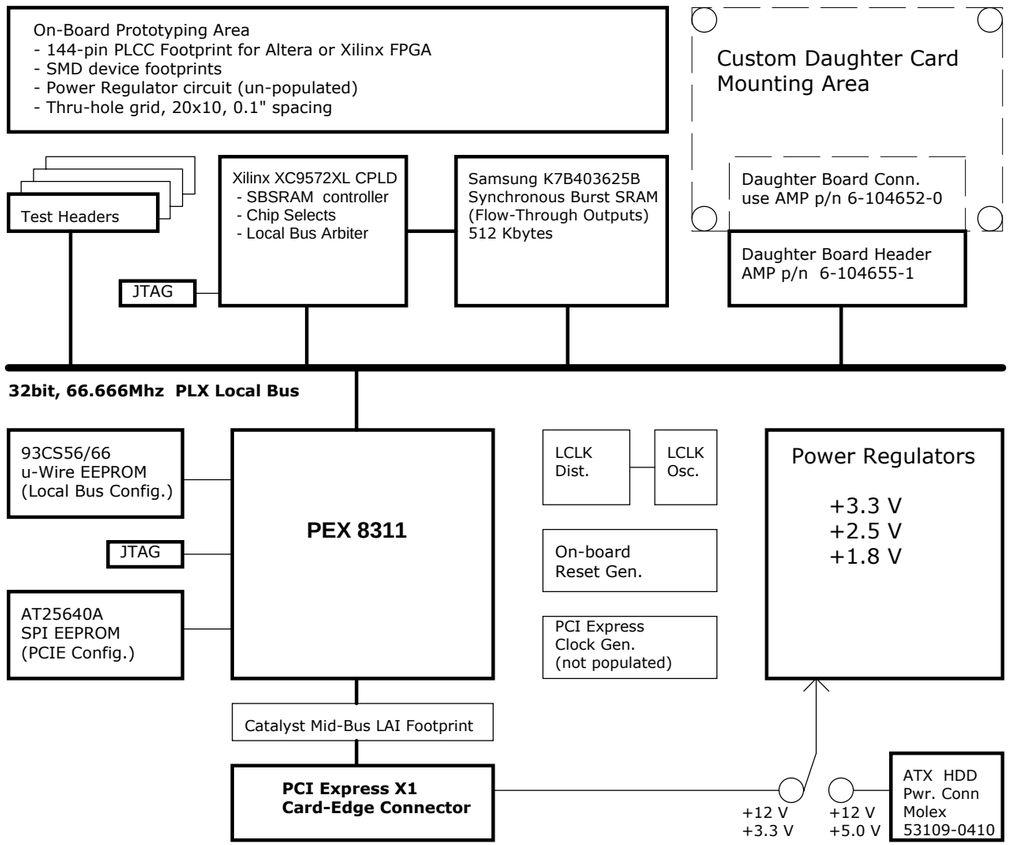
Item #	Qty	Man	Man's Part #	Des	Package Type	Schematic Reference	Subcon.	Subcon. Part #
SURFACE MOUNT COMPONENTS								
1	8	Panasonic	ECJ1VB1H102K	Cap, Ceramic, 0.001 uF, 10%, 50V, X7R	0603	C16, C18, C20, C26, C28, C30, C32, C200	Taiyo-Yuden	UMK107B102KZ-T
2	24	Kemet	C0603C103M5UAC	Cap, Ceramic, 0.01 uF, 50 V, 20%	0603	C6, C10, C46, C48, C52, C54, C56, C58, C60, C62, C64, C66, C68, C70, C72, C74, C79, C83, C84, C85, C89, C90, C91, C155		
3	47	Panasonic	ECJ1VB1E104K	Cap, Ceramic, 0.1 uF, 10%, 16V, X7R	0603	C1, C2, C3, C8, C12, C14, C15, C17, C19, C22, C23, C24, C25, C27, C29, C31, C36, C37, C38, C39, C40, C41, C42, C44, C45, C47, C49, C50, C53, C55, C57, C59, C61, C63, C65, C67, C69, C71, C73, C75, C77, C80, C81, C82, C86, C87, C88		
4	2	Panasonic	ECJ1VB1C105K, ECJ1VF105Z	Cap, Ceramic, 1.0 uF, 16 V	0603	C5, C11	Taiyo-Yuden	EMK107BJ105MA-B
5	10	Kemet	T494B106K016AT	Cap, Tantalum, 10 uF, 16V	CASE B	C4, C7, C9, C21, C33, C34, C35, C51, C76, C78	AVX	TAJ B 106M016R
6	2	Kemet	T491D474M016AT	Cap, Tantalum, 47uF,16V	CASE D	C13, C43	AVX	TAJ C476M020R
7	6	Samtec	TSM-110-01-T-DV	Header, 10 x 2 pins, 0.1", SMT	SMT	LAH1, LAH2, LAH3, LAH4, LAH5, LAH6		
8	1	AMP	6-104655-1	Header, 50 x 2 pins, .25mm, SMT, Shrouded	SMT	J3		
9	4	Chicago	CMD17-21VRC/TR8	LED, SMT, Red	0805	LED1, LED2, LED3, LED4		
10	3	Chicago	CMD17-21VGC/TR8	LED, SMT, Green	0805	LED5, LED6, LED8		
11	1	Steward	L10805E400R	Ferrite chip, 47 uH, 500mA	0805	L1		
12	1	CTS Corp	742C083271JTR	Resistor Array, x4, 270 Ohms, 5%, 0.1W	0603x4	RN1	NIC Compnents	NSRN06I4G271TRF
13	13	CTS Corp	742C083103JTR	Resistor Array, x4, 10K Ohms, 5%, 0.1W	0603x4	RN2, RN3, RN4, RN5, RN6, RN7, RN8, RN9, RN10, RN11, RN12, RN13, RN14	NIC Components	NSRN06I4J103TRF
14	30	Panasonic	ERJ3GEY0R00V	Resistor, 0 ohms (Jumper), 5%, 0.1 W	0603	R9, R10, R11, R12, R13, R34, R35, R53, R63, R66, R74, R76, R84, R88, R94, R96, R100, R106, R109, R111, R113, R122, R123, R129, R130, R131, R132, R133, R134, R135	NIC Components	NRC06Z0
15	2	Panasonic	ERJ6GEY0R00V	Resistor, 0 ohms (Jumper), 5%. 1/8W	0805	R21, R23	NIC Components	NRC10Z0
16	1	Panasonic	ERJ3RQF0r180V	Resistor, 0.18 ohms, 1%, 0.1W	0603	R24	NIC Components	NRC06F0R18TRF
17	5	Panasonic	ERJ3GEYJ330V	Resistor, 33 ohms , 5%, 0.1 W	0603	R54, R55, R56, R57, R58	NIC Components	NRC06J330TRF
18	5	Panasonic	ERJ3GEYJ101V	Resistor, 100 ohms , 5%, 0.1 W	0603	R28, R29, R30, R31, R127	NIC Components	NRC06J101TRF
19	2	Panasonic	ERJ3GEYJ331V	Resistor, 330 ohms, 5%, 0.1W	0603	R99, R125	NIC Components	NRC06J331TRF
20	22	Panasonic	ERJ3GEYJ102V	Resistor, 1K ohms , 5%, 0.1 W	0603	R5, R6, R8, R14, R15, R16, R17, R18, R19, R41, R65, R67, R68, R69, R72, R73, R78, R79, R80, R81, R82, R639	NIC Components	NRC06J102TRF
21	1	Panasonic	ERJ3GEYJ122V	Resistor, 1.2K ohms , 5%, 0.1 W	0603	R124	NIC Components	NRC06J122TRF
22	26	Panasonic	ERJ3GEYJ103V	Resistor, 10K ohms , 5%, 0.1 W	0603	R3, R4, R25, R26, R36, R37, R38, R42, R43, R44, R45,	NIC Components	NRC06J103TRF

Item #	Qty	Man	Man's Part #	Des	Package Type	Schematic Reference	Subcon.	Subcon. Part #
						R47, R48, R50, R89, R90, R91, R92, R98, R101, R102, R104, R105, R107, R638, R1147		
23	1	Omron	B3S1002	Switch, SPST, momentary, vertical	SMT	SW1		
24	1	PLX Technology, Inc.	PEX 8311	IC, PEX8311	BGA, 21x21 mm, 20x20 ball, 1.0mm pitch	U1		
25	1	National Semiconductor	LP2992IM5-1.5	IC, LDO Regulator, 1.5 V, 250 mA	NS Package Number MF05A	U3		
26	1	National Semiconductor	LMS1585ACS-3.3	IC, LDO Regulator, 3.3V, 3A		U4		
27	1	Semtech	LT1963AEXT-25	IC, LDO regulator, 2.5V, 1A	SOT-223	U9		
28	1	Maxim	MAX6306UK30D1-T	IC, Reset Controller, MAX6306UK30D1-T	SOT-23, 5 pin	U5		
29	1	Cypress Semiconductor	CY2305SC-1	IC, Clock Buffer, CY2305	SOIC, 8-pin	U7		
30	1	Xilinx	XC9572XL-5TQ100C	IC, CPLD Programmable Logic XC9572XL-5TQ100C	TQFP, 100 pins (square)	U10		
31	1	Samsung	K7B403625B	IC, Synchronous SRAM, 4 Mbit, 128Kx36, Flow-Through	TQFP, 100 pins, 14x20 mm	U11		
THROUGH-HOLE COMPONENTS								
32		4	Molex	22-28-4020	Header, 2 x 1 pins, 0.1", vert., no shroud	Thru-Hole	JP1, J7, J8, J9	AMP
33		4	Molex	22-28-4030	Header, 3 x 1 pins, 0.1", vert., no shroud	Thru-Hole	JP2, JP3, JP4, JP5	AMP
34		1	Molex	22-28-4060	Header, 6 x 1 pins, 0.1", vert., no shroud	Thru-Hole	J1	
35		1	Molex	22-28-4090	Header, 9 x 1 pins, 0.1", vert., no shroud	Thru-Hole	J2	
36		1	Molex	53109-0410	5.08mm (.200") Pitch Disk Drive Power Connection System Header, Right Angle, with Strap Standard Polarization, 4 Circuits	Thru-Hole	J4	
37		3	Mil-Max	110-93-308-41-001	Socket, 8-pin dip, 0.3", solder tail, low-profile	Thru-Hole	U2, U6, U8	
COMPONENTS THAT ARE HAND-ASSEMBLED								
38	1	CTS Corp	MXO45HS-3C-66M6666	OSC, 66.666 MHz clock oscillator, 3.3V, 50ppm, 40-60% duty cycle	Half-size DIP, 8-pin	U8	Ecliptek	EP1345HSPD-66.666M
39	1	Atmel	AT25640A-10PI-2.7	IC, Serial EEPROM, SPI, 64K, AT25640	DIP, 8-pin	U2		
40	1	Atmel	AT93C56A-10PU-2.7	IC, Serial EEPROM, 3-wire, AT93C56/66A	DIP, 8-pin	U6		
41	1	Keystone	9203	PCI Bracket, Blank		BRACKET1		

Item #	Qty	Man	Man's Part #	Des	Package Type	Schematic Reference	Subcon.	Subcon. Part #
42	2	Spaenaur	492-100	Phillips, 4-40, 1/4", PH screw (for PCB bracket)		SCREW1, SCREW2		
43	6			Jumper shunts, for 0.1" hdr.		J7, J8, J9, JP3(1-2), JP4(1-2), JP5(1-2)		
MISCELLANEOUS COMPONENTS								
44	1			PEX 8311RDK PCB, p/n 90-0058-000-A				
45	1	Velostat	2100R/8X10	8" x 10" anti-static bag		BAG1		FAI
PARTS THAT ARE NOT POPULATED (DO NOT KIT)								
46	1	Molex	10-88-1105	Header, 5 x 2 pins, 0.1", vert., no shroud	Thru-Hole	JP6		
47	1	Comm Con	2422-14G2	Header, 7 x 2 pins, 0.1", vert, keyed shrd.		JP7	OUPIIN	3112-14GSB
48	1	Semtech	EZ117-2.5	IC, LDO regulator, 2.5V, 1A	SOT-223	U14		
49	2	Panasonic	ERJ6GEY0R00V	Resistor, 0 ohms (Jumper), 5%. 1/8W	0805	R22, R27	NIC Components	NRC10Z0
50	3	Kemet	T494B106K016AS	Cap, Tantalum, 10 uF, 16V	CASE B	C96, C98, C100	AVX	TAJ B 106M016R
51	1	ICS Tech (www.icst.com)	ICS557G03	IC, PCI-Express Clock Source, ICS557-03	TSSOP-16 pins	U12		
52	1	CTS Corp	CB3LV-3C-25M0000	XTAL, 25 MHz, SMD	SMT, 3.2x2.5mm	Y1		
53	1	CTS Corp	MXO45HS-3C-66M6666	OSC, 66.666 MHz clock oscillator, 3.3V, 50ppm, 40-60% duty cycle	Half-size DIP, 8-pin	U13	Ecliptek	EP1345HSPD-66.666M
54	1	Mil-Max	110-93-308-41-001	Socket, 8-pin dip, 0.3", solder tail, low-profile	Thru-Hole	U13		
55	1	Panasonic	ERJ3GEYJ100V	Resistor, 10 ohms , 5%, 0.1 W	0603	R136	NIC Components	NRC06J100TRF
56	4	Panasonic	ERJ3GEYJ330V	Resistor, 33 ohms , 5%, 0.1 W	0603	R137, R141, R145, R148	NIC Components	NRC06J330TRF
57	4	Panasonic	ERJ3EKF49R9V	Resistor, 49.9 ohms, 1%, 0.1W	0603	R138, R142, R143, R147	NIC Components	NRC10F49R9TRF
58	1	Panasonic	ERJ3EKF4750V	Resistor, 475 Ohms, 1%, 0.1W	0603	R149	NIC Components	NRC10F4750TRF
59	8	Panasonic	ERJ3GEYJ103V	Resistor, 10K ohms , 5%, 0.1 W	0603	R32, R33, R139, R140, R144, R146, R147,R641	NIC Components	NRC06J103TRF
60	2	Panasonic	ECJ1VC1H100D	Cap, Ceramic, 10 pF, 50V, +/- 0.5 pF	0603	C94, C95		
61	2	Kemet	C0603C103M5UAC	Cap, Ceramic, 0.01 uF, 50 V, 20%	0603	C92, C93		
62	1	Panasonic	ECJ1VB1E104K	Cap, Ceramic, 0.1 uF, 10%, 16V, X7R	0603	C97		
63	18	Panasonic	ERJ3GEY0R00V	Resistor, 0 ohms (Jumper), 5%, 0.1 W	0603	R59, R60, R61, R62, R64, R83, R86, R75, R77, R85, R87, R93, R95, R97, R103, R108, R110, R112	NIC Components	NRC06Z0
64	3	Panasonic	ERJ3GEYJ472V	Resistor, 4.7K ohms , 5%, 0.1 W	0603	R39, R49, R51	NIC Components	NRC06J103TRF
NOTE: NOT POPULATED NO VALUE COMPONENTS FROM SHEETS 8 TO 12 OF THE SCHEMATICS ARE NOT LISTED. SEE SECTION 4.4.2 FOR COMPONENT VALUES								
NOTE: OTHER NOT POPULATED COMPONENTS ARE NOT LISTED AT THIS TIME								
Customer Name: PLX								
PLX Part #: 91-0058-000-A								
Product Name: PEX 8311RDK								

Table Of Contents

Block Diagram



This schematic includes minor board errata's which are not implemented in the PCB layout. See PEX8311RDK Errata Rev. 1.0, Dec. 2005 for details.

Revision History

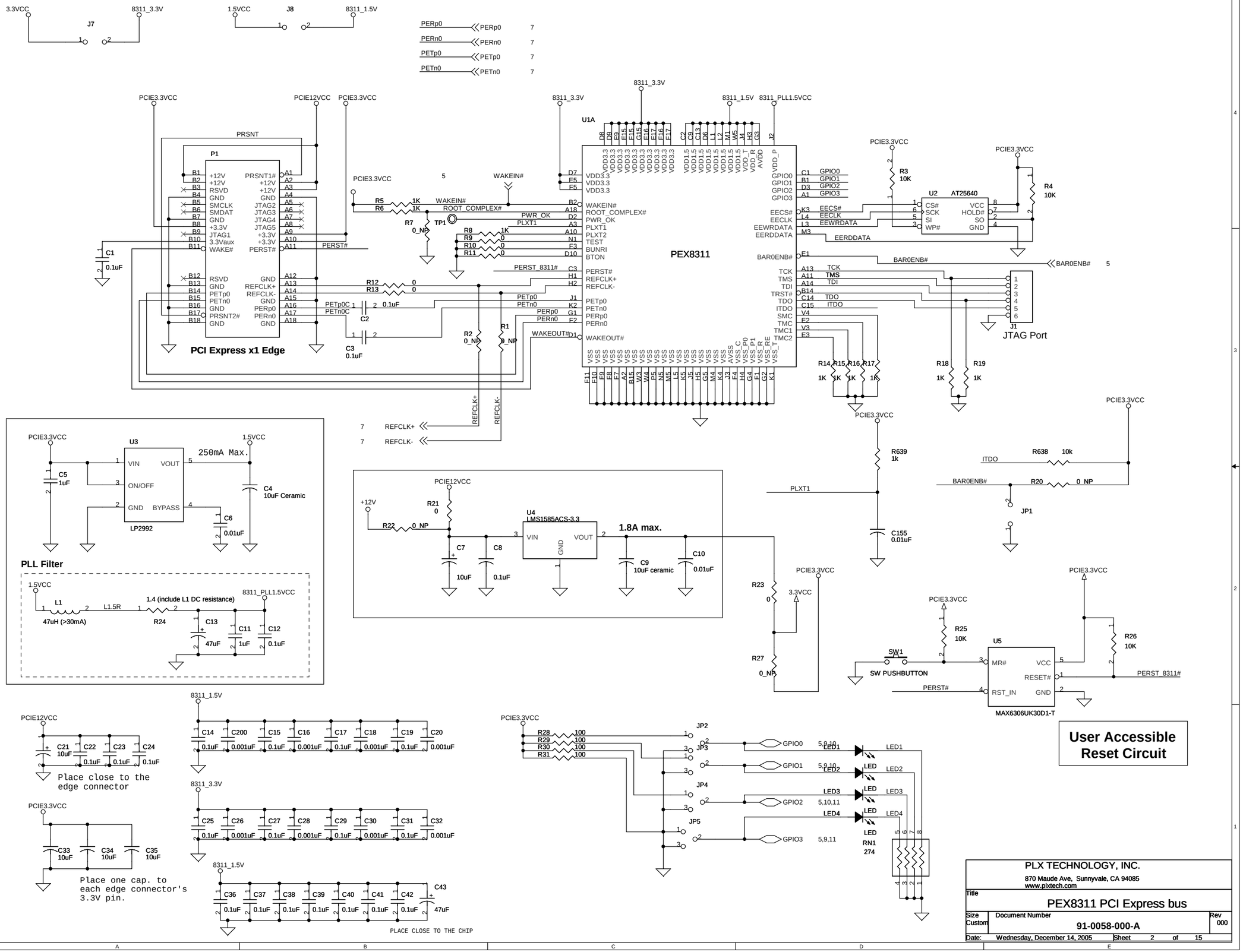
Date	Summary of Changes
12-08--05	Release 1.0

PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title: PEX8311RDK-Lite

Size: Custom | Document Number: 91-0058-000-A | Rev: 000

Date: Wednesday, December 14, 2005 | Sheet 1 of 15

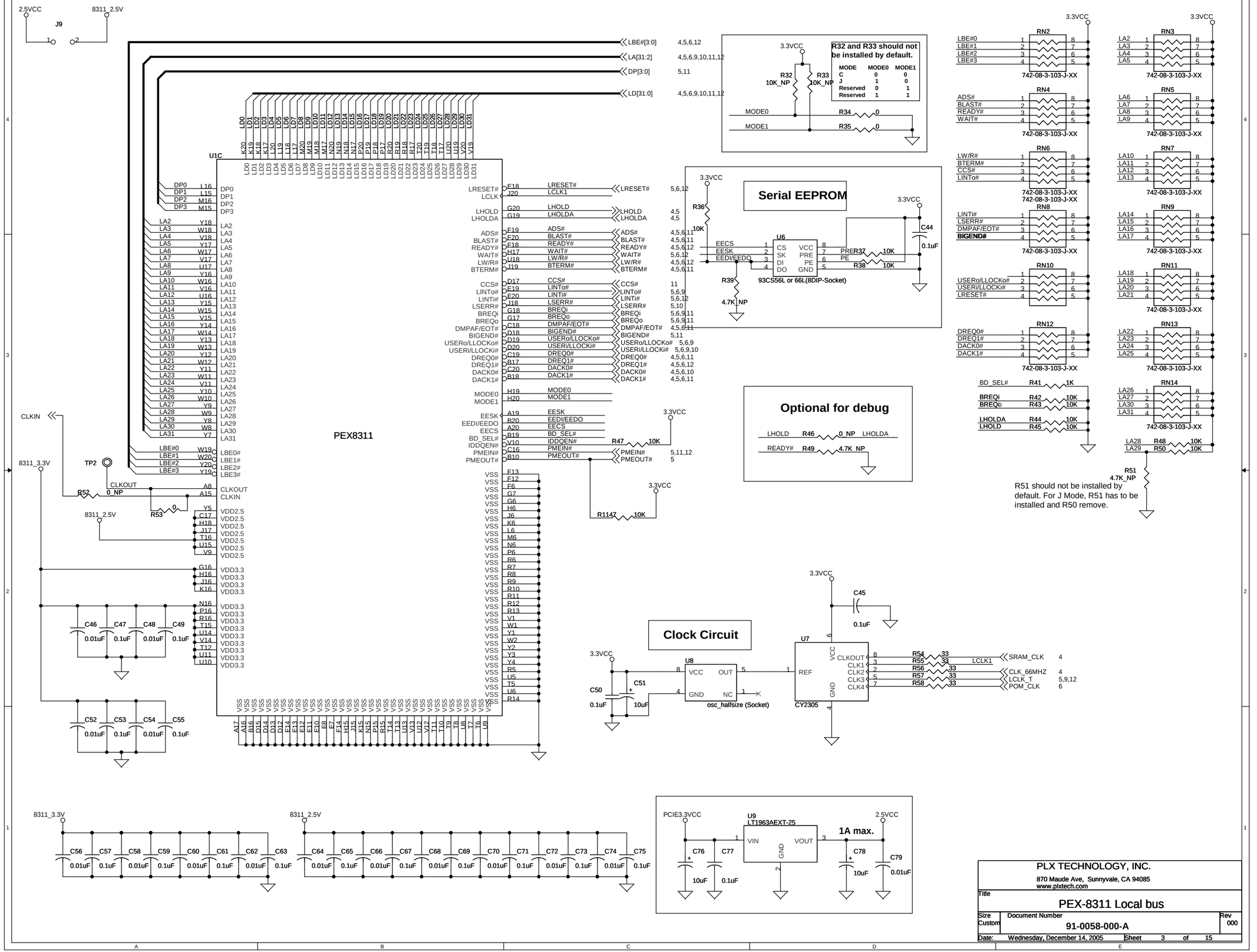


PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title: PEX8311 PCI Express bus

Size: Custom | Document Number: 91-0058-000-A | Rev: 000

Date: Wednesday, December 14, 2005 | Sheet 2 of 15


PEX8311
U1C
J9
2.5VCC
8311_2.5V
LBE#[3:0] 4,5,6,12
LA[31:2] 4,5,6,9,10,11,12
DP[3:0] 5,11
LD[31:0] 4,5,6,9,10,11,12
R32 and R33 should not be installed by default.
MODE MODE0 MODE1
C 0 0
J 1 0
Reserved 0 1
Reserved 1 1
R32 10K_NP
R33 10K_NP
R34 0
R35 0
Serial EEPROM
93CS56L or 66L(8DIP-Socket)
U6
R36 10K
R39 4.7K NP
R37 10K
R38 10K
C44 0.1uF
Optional for debug
R46 0_NP
R49 4.7K_NP
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
RN10
RN11
RN12
RN13
RN14
742-08-3-103-J-XX
R41 1K
R42 10K
R43 10K
R44 10K
R45 10K
R47 10K
R1147 10K
R48 10K
R50 10K
R51 4.7K_NP
R51 should not be installed by default. For J Mode, R51 has to be installed and R50 remove.
CLKIN
TP2
CLKOUT
R52 0_NP
R53 0
C46 C47 C48 C49 0.01uF 0.1uF 0.01uF 0.1uF
C52 C53 C54 C55 0.01uF 0.1uF 0.01uF 0.1uF
C56 C57 C58 C59 C60 C61 C62 C63 0.01uF 0.1uF
C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 0.01uF 0.1uF
Clock Circuit
U8 osc_halfsize (Socket)
U7 CY2305
C50 0.1uF
C51 10uF
C45 0.1uF
R54 R55 R56 R57 R58 33
SRAM_CLK 4
CLK_66MHZ 4
LCLK_T 5,9,12
POM_CLK 6
PCIE3.3VCC
U9 LT1963AEXT-25
1A max.
C76 10uF
C77 0.1uF
C78 10uF
C79 0.01uF
PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com
Title
PEX-8311 Local bus
Size Custom
Document Number 91-0058-000-A
Rev 000
Date: Wednesday, December 14, 2005
Sheet 3 of 15

Synchronous SRAM and Controller Circuit

R59-R62, and R64 should not be installed by default

3,5,6,11 DREQ0# — DREQ0# — R59 0
3,5,6,12 DREQ1# — DREQ1# — R60 0
3,5,6,10 DACK0# — DACK0# — R61 0
3,5,6,11 DACK1# — DACK1# — R62 0
3,5,6,11 DMPAF/EOT# — DMPAF/EOT# — R64 0

3.3VCC

U10

CPLD

PA8 AA3 16 IOA1
PA21 MA6 13 IOA2
PA2 LBR1 18 IOA3
PA11 20 IOA4
PA13 MA5 14 IOA5
PA4 15 IOA6
PA15 CS_0# 25 IOA7
PA17 17 IOA8
PA18 AA2 28 IOA9
PA22 AA31 23 IOA10/GCK2
PA24 CS_1# 33 IOA11
PA26 ADS# 36 IOA12
PA7 AA29 29 IOA13
PA28 CS_2# 39 IOA14
PA30 AA6 30 IOA15
PA32 CS_3# 40 IOA16

PA35 87 IOB1
PA36 94 IOB2
PA38 91 IOB3
PA40 MA3 93 IOB4
PA42 95 IOB5
PA44 96 IOB6
PA46 AA7 3 IOB7/GTS1
PA48 MA9 97 IOB8
PA50 LW/R# 99 IOB9/GSR
PA52 LBE#2 1 IOB10
PA54 MA7 6 IOB11
PA56 8 IOB12
PA58 LBE#3 9 IOB13
PA60 AA9 11 IOB14
PA62 10 IOB15
PA64 MA8 12 IOB16
PA66 92 IOB17

PA70 R83 0 27 IO/GCK1
PA71 4 IO/GCK3
R86 IO/GTS2

GND GND GND GND GND GND GND NC NC NC NC NC NC NC NC NC
21 31 44 62 69 75 84 100 2 7 19 24 34 42 46 73 80

XC9572XL-5TQ100C
or XC95144XL-5TQ100C
100-pin TQFP

IOC1 LBG0 41 PA20
IOC2 AA4 49 PA9
IOC3 LBG1 32 PA1
IOC4 LHOLD 50 PA10
IOC5 LHOLDA 35 PA12
IOC6 BLAST# 53 PA3
IOC7 BTERM 54 PA14
IOC8 AA8 37 PA16
IOC9 READYN 42 PA5
IOC10 60 PA19
IOC11 SRAM_BW_0 52 PA23
IOC12 LBR0 61 PA25
IOC13 SRAM_BW_1 63 PA6
IOC14 55 PA27
IOC15 SRAM_BW_2 56 PA29
IOC16 64 PA31
IOC17 SRAM_BW_3 58 PA33
IOC18 59 PA34

IOD1 AA30 65 PA37
IOD2 67 PA39
IOD3 SRAMCS 71 PA41
IOD4 72
IOD5 68
IOD6 76 PA47
IOD7 AA28 77 PA49
IOD8 SRAMOE_ 70 PA51
IOD9 66 PA53
IOD10 81 PA55
IOD11 74 PA57
IOD12 LBE#1 82 PA59
IOD13 MA2 85 PA61
IOD14 78 PA63
IOD15 LBE#0 89 PA65
IOD16 86 PA67
IOD17 MA4 90 PA68
IOD18 AA5 79 PA69

TCK 48
TDI 45
TDO 83
TMS 47

R63 0 READY#
R66 0 BTERM#

LBR0 LBG0 LBG0
LBR1 LBG1 LBR1
LBG1

R70 0 NP SA15 PA43
R71 0_NP SA16 PA45

3.3VCC

J2
1 2 3 4 5 6 7 8 9
CPLD_TCK
CPLD_TDO
CPLD_TDI
CPLD_TMS
1x9 HDR, 0.1"oc

R89 R90 R91 R92 10K 10K 10K 10K 3.3VCC

3,5,6,9,10,11,12 LA[31:2]

3.3VCC

R68 R67 R69 R65 1K 1K 1K 1K

R72 1K R73 1K

3 SRAM_CLK — SRAM_CLK
SRAMCS
SRAMOE
SRAM_BW_0
SRAM_BW_1
SRAM_BW_2
SRAM_BW_3

R78 R79 R80 R81 R82 1K 1K 1K 1K 1K

U11

SYNC_SRAM

128Kx36

MA2 37 SA0
MA3 36 SA1
MA4 35 SA2
MA5 34 SA3
MA6 33 SA4
MA7 32 SA5
MA8 100 SA6
MA9 99 SA7
LA10 82 SA8
LA11 81 SA9
LA12 44 SA10
LA13 45 SA11
LA14 46 SA12
LA15 47 SA13
LA16 48 SA14
SA15 49 SA15
SA16 50 SA16

88 GW#
97 CE2
83 ADV#
84 ADSP#
89 CLK
98 CE#
86 OE#
93 BWa#
94 BWb#
95 BWc#
96 BWd#
31 MODE
85 ADSC#
87 BWE#
92 CE2#
64 ZZ

DQa0 52 LD0
DQa1 53 LD1
DQa2 56 LD2
DQa3 57 LD3
DQa4 58 LD4
DQa5 59 LD5
DQa6 62 LD6
DQa7 63 LD7
DQb0 68 LD8
DQb1 69 LD9
DQb2 72 LD10
DQb3 73 LD11
DQb4 74 LD12
DQb5 75 LD13
DQb6 78 LD14
DQb7 79 LD15
DQc0 2 LD16
DQc1 3 LD17
DQc2 6 LD18
DQc3 7 LD19
DQc4 8 LD20
DQc5 9 LD21
DQc6 12 LD22
DQc7 13 LD23
DQd0 18 LD24
DQd1 19 LD25
DQd2 22 LD26
DQd3 23 LD27
DQd4 24 LD28
DQd5 25 LD29
DQd6 28 LD30
DQd7 29 LD31

VSS 5 10 17 28 40 55 60 67 71 76 90
NC 14 38 39 42 43

K7B403625B

LD[31:0] — LD[31:0] — 3,5,6,9,10,11,12

LA[31:2]

R74 0 LA31 LD31 AA31
R75 0
R76 0 LA30 LD30 AA30
R77 0 R84 0 LA29 LD29 AA29
R85 0 LA28 AA28

LD2 R87 0 AA2 LA2 R88 0
LD3 R93 0 AA3 LA3 R94 0
LD4 R95 0 AA4 LA4 R96 0
LD5 R97 0 AA5 LA5 R100 0
LD6 R103 0 AA6 LA6 R106 0
LD7 R108 0 AA7 LA7 R109 0
LD8 R110 0 AA8 LA8 R111 0
LD9 R112 0 AA9 LA9 R113 0

LD[31:0] 3,5,6,9,10,11,12

R83 and R86 should not be installed by default

For C mode (default), install R74,R76,R84,R88 , R94,R96,R100,R106,R109,R111 and R113, remove R75, R77 and R85,R87,R93,R95,R97, R103,R108,R110,and R112
For J mode, it is vice versa.

CS_0# — CS_0# 6

3.3VCC

SRAMCS R98 10K
SRAMOE R101 10K
SRAM_BW_0 R102 10K
SRAM_BW_1 R104 10K
SRAM_BW_2 R105 10K
SRAM_BW_3 R107 10K

LBR0 R99 330

3.3VCC

C80 C81 C82 C83 C84 C85
0.1uF 0.1uF 0.1uF 0.01uF 0.01uF 0.01uF

3.3VCC

C86 C87 C88 C89 C90 C91
0.1uF 0.1uF 0.1uF 0.01uF 0.01uF 0.01uF

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www.plxtech.com

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Date: Wednesday, December 14, 2005 | Sheet 4 of 15

3,4,6,12 LBE#[3:0]

LBE#0
LBE#1
LBE#2
LBE#3

3,11 DP[3:0]

DP0
DP1
DP2
DP3

3,4,6,9,10,11,12 LA[31:2]

LA2 LA3 LA4 LA5 LA6 LA7 LA8 LA9 LA10 LA11 LA12 LA13 LA14 LA15 LA16 LA17 LA18 LA19 LA20 LA21 LA22 LA23 LA24 LA25 LA26 LA27 LA28 LA29 LA30 LA31

3,4,6,9,10,11,12 LD[31:0]

LD0 LD1 LD2 LD3 LD4 LD5 LD6 LD7 LD8 LD9 LD10 LD11 LD12 LD13 LD14 LD15 LD16 LD17 LD18 LD19 LD20 LD21 LD22 LD23 LD24 LD25 LD26 LD27 LD28 LD29 LD30 LD31

TP3 TP4 TP5 TP6 TP7 TP8

PCIE3.3VCC

LAH1

3,6,9,11 BREQo
3,6,9,11 BREQi
3,4,6,10 DACK0#
3,4,6,11 DREQ0#
3,4,6,11 DACK1#
3,4,6,12 DREQ1#
3,4,6,11 DMPAF/EOT#
3,6,9,10 USERi/LLOCKi#
3,6,9 USERo/LLOCKo#

BREQo BREQi DACK0# DREQ0# DACK1# DREQ1# DMPAF/EOT# USERi/LLOCKi# USERo/LLOCKo#

+5V D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 GND

BIGENDE# PMEIN# PMEOUT# WAKEIN# BAR0ENB# GPIO0 GPIO1 GPIO2 GPIO3

BIGEND# PMEIN# PMEOUT# WAKEIN# BAR0ENB# GPIO0 GPIO1 GPIO2 GPIO3

Logic Analyzer Header

0_NP R114 R115 R116 R117 R118 R119 R120 R121

LAH2

2,9,10 GPIO0
2,9,10 GPIO1
2,10,11 GPIO2
2,9,11 GPIO3

LA28 LA26 LA24 LA22 LA20 LA18 LA16 LA14 LA29 LA27 LA25 LA23 LA21 LA19 LA17 LA15

Logic Analyzer Header

LAH3

3,9,12 LCLK_T

LA12 LA10 LA8 LA6 LA4 LA2 LBE#2 LBE#0 LA13 LA11 LA9 LA7 LA5 LA3 LBE#3 LBE#1

Logic Analyzer Header

LAH4

LD8 LD6 LD4 LD2 LD0 DP2 DP0 LA30 LD9 LD7 LD5 LD3 LD1 DP3 DP1 LA31

Logic Analyzer Header

LAH5

3,6,9 LINTo#
3,6,12 LINTi#
3,4,6,12 LW/R#
3,4,6,12 READY#
3,4,6,11 ADS#
3,4 LHOLD

LINTo# LINTi# LW/R# READY# ADS# LHOLD LD30 LD28 LD26

LRESET# LSERR# BTERM# WAIT# BLAST# LHOLDA LD31 LD29 LD27

LRESET# LSERR# BTERM# WAIT# BLAST# LHOLDA

3,6,12 3,10 3,4,6,11 3,6,12 3,4,6,11 3,4

Logic Analyzer Header

LAH6

LD24 LD22 LD20 LD18 LD16 LD14 LD12 LD10 LD25 LD23 LD21 LD19 LD17 LD15 LD13 LD11

Logic Analyzer Header

2.5VCC

LED8
LED
R127
100

PCIE12VCC 0 R122

LED5
LED
R124
1.2K

TP9 TP10 TP11

3.3VCC 0 R123

LED6
LED
R125
330

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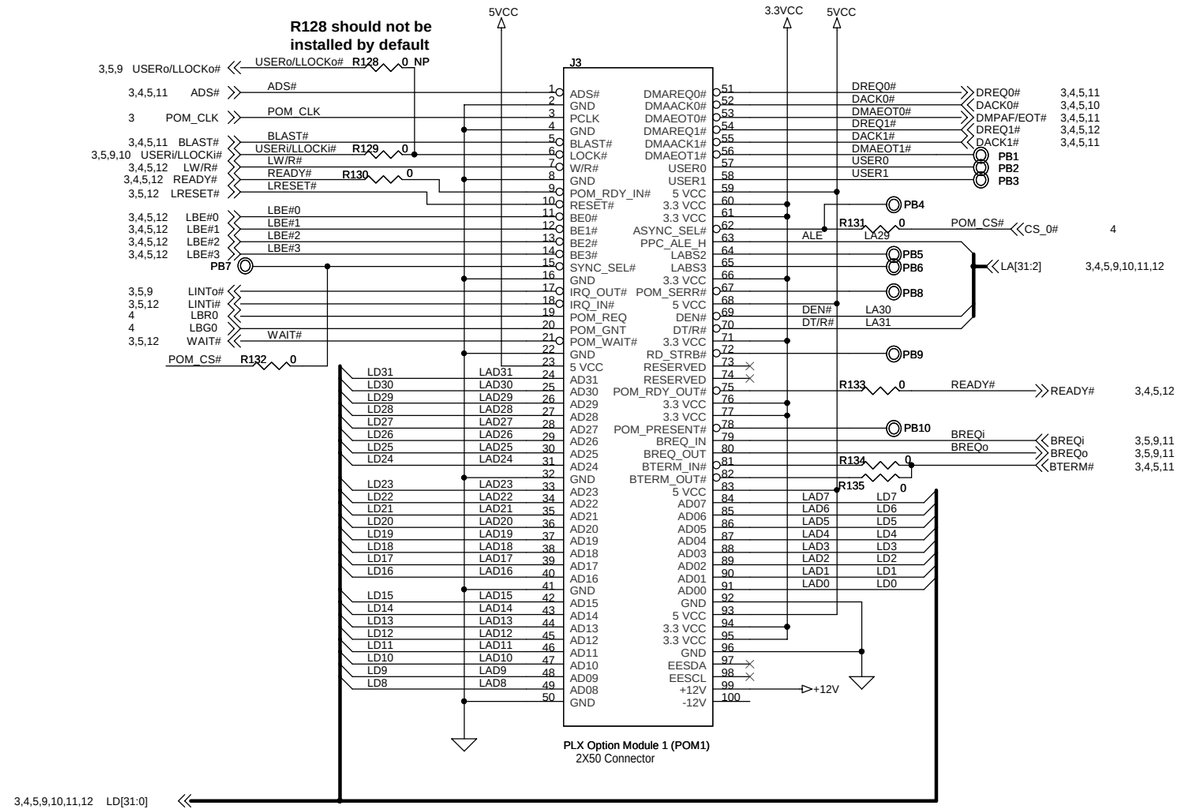
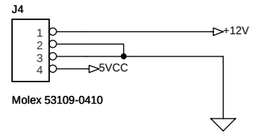
PLX Option Module Connector





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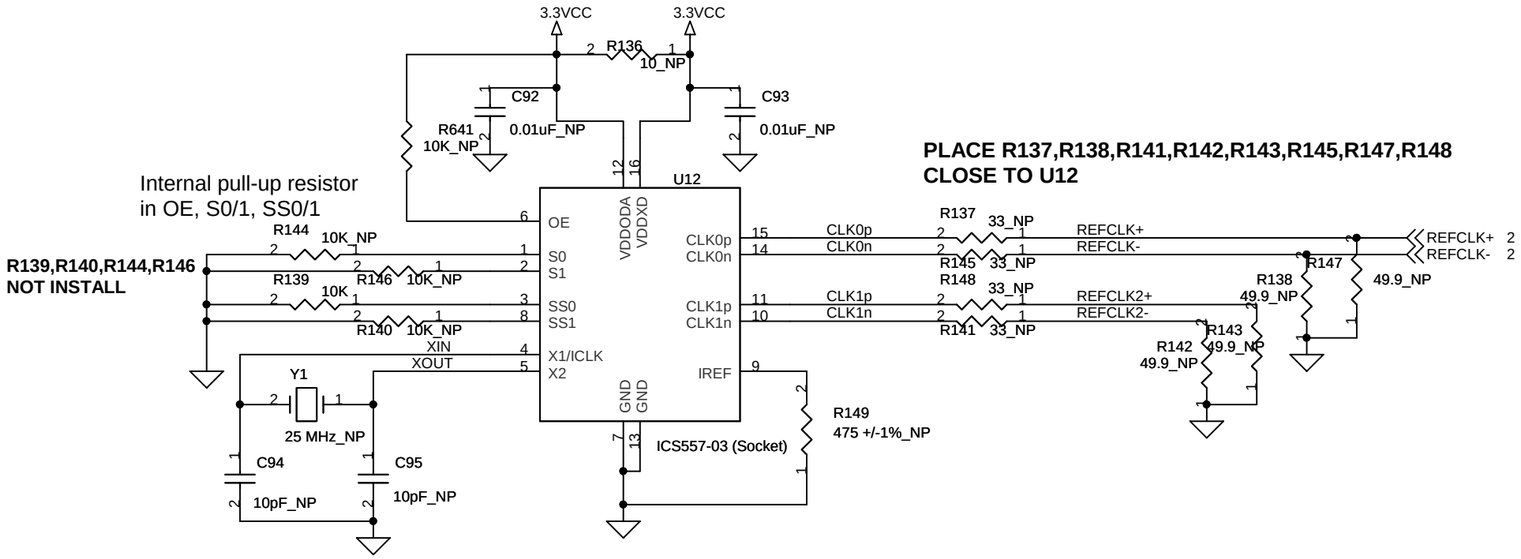
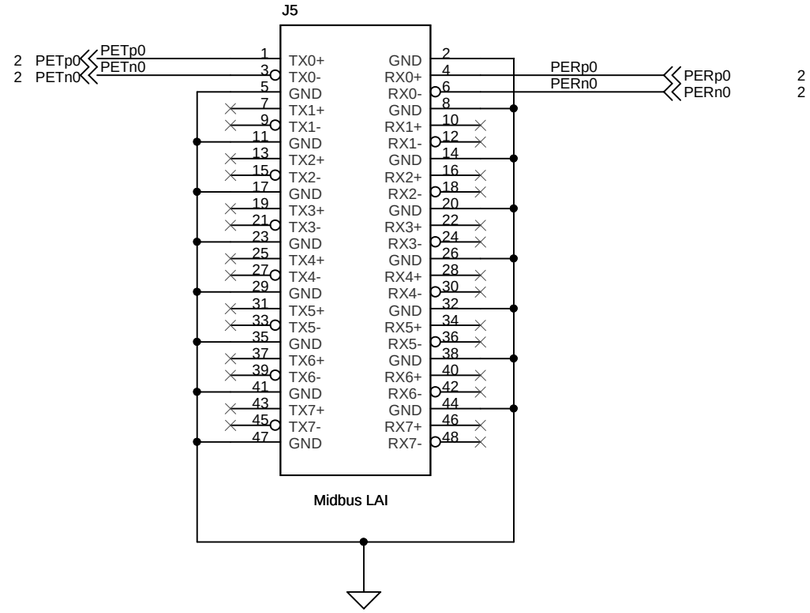
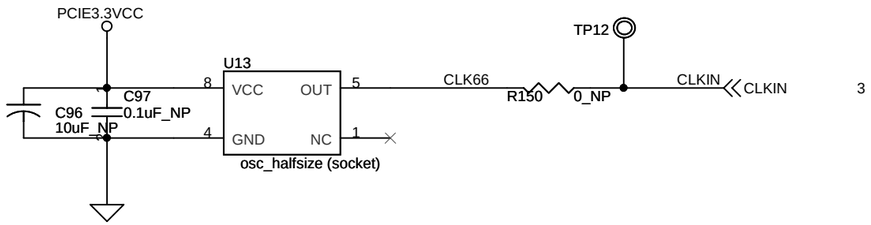
870 Maude Ave, Sunnyvale, CA 94085 www.plxtech.com			
Title: PLX Option Module Connector			
Size: Custom	Document Number: 91-0058-000-A		Rev: 000
Date: Wednesday, December 14, 2005	Sheet 6 of 15		

Clock Circuit

The components on this sheet are not installed by default.



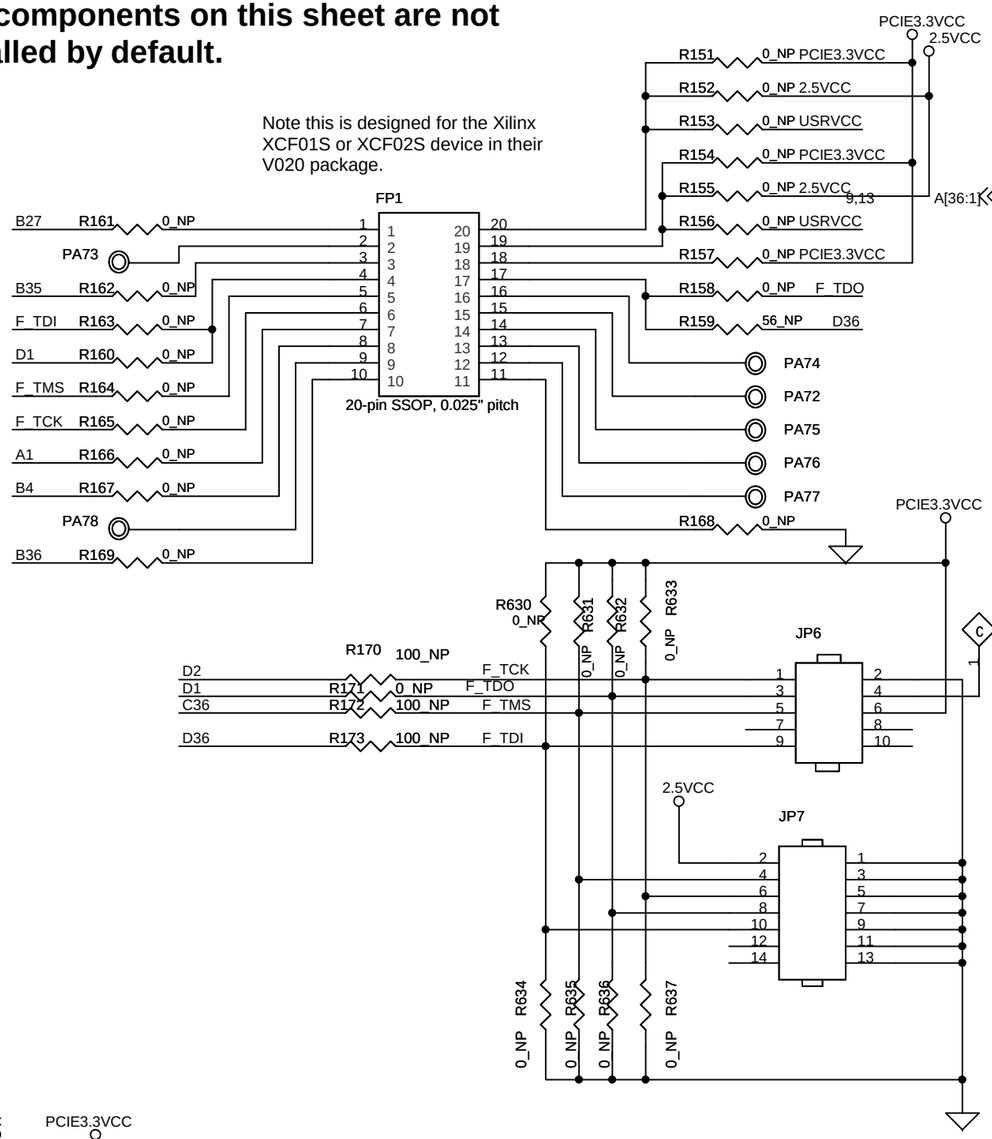


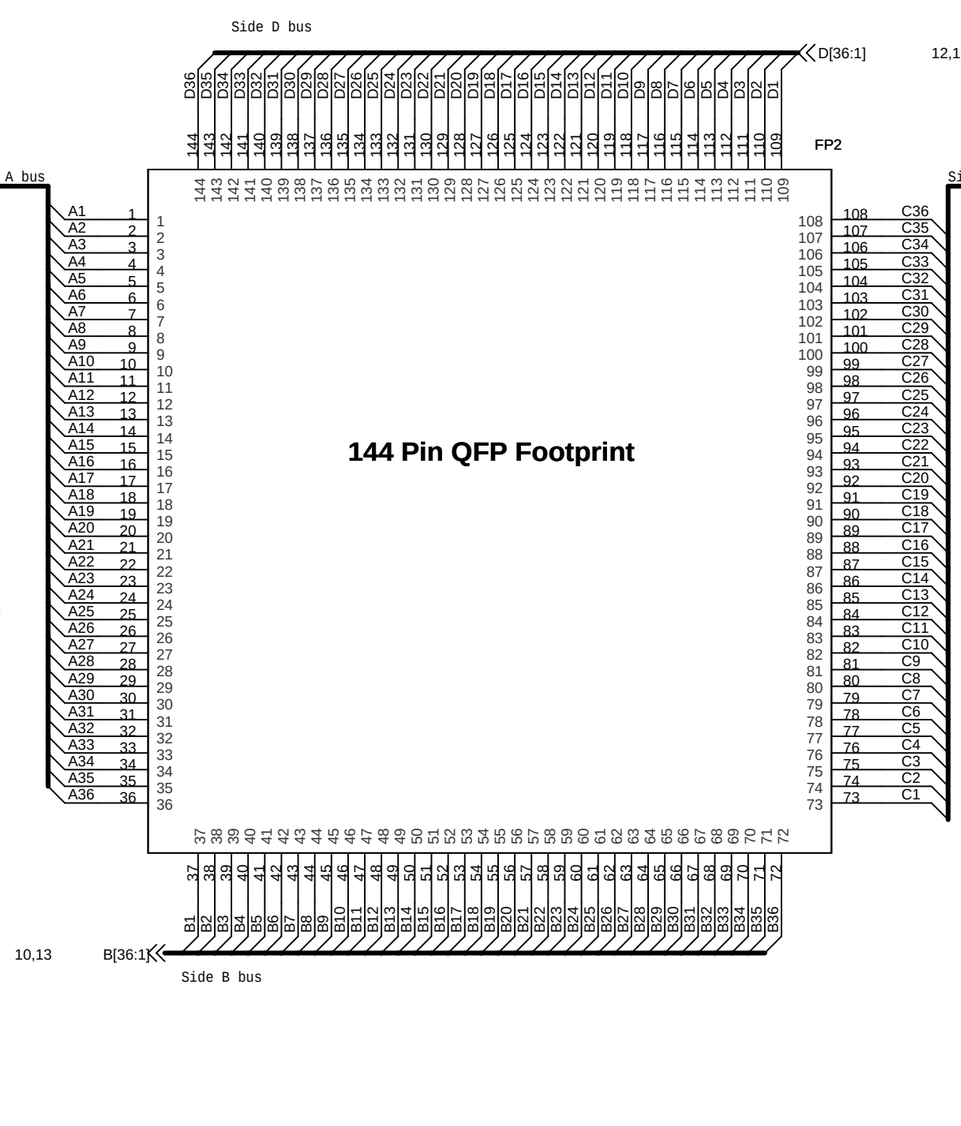


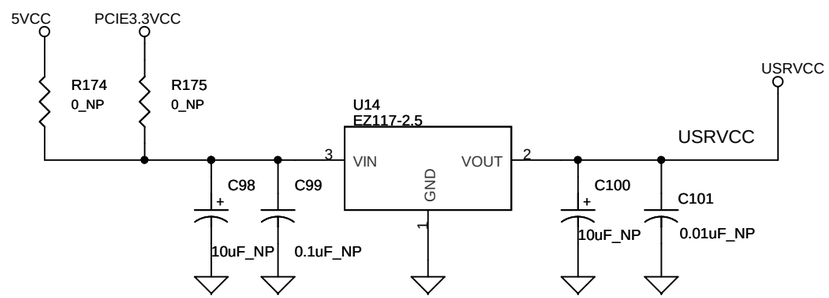
Title	PCI Express Midbus & Clock	
Size B	Document Number 91-0058-000-A	Rev 000
Date: Wednesday, December 14, 2005	Sheet 7 of 15	

The components on this sheet are not installed by default.

Note this is designed for the Xilinx XCF01S or XCF02S device in their V020 package.



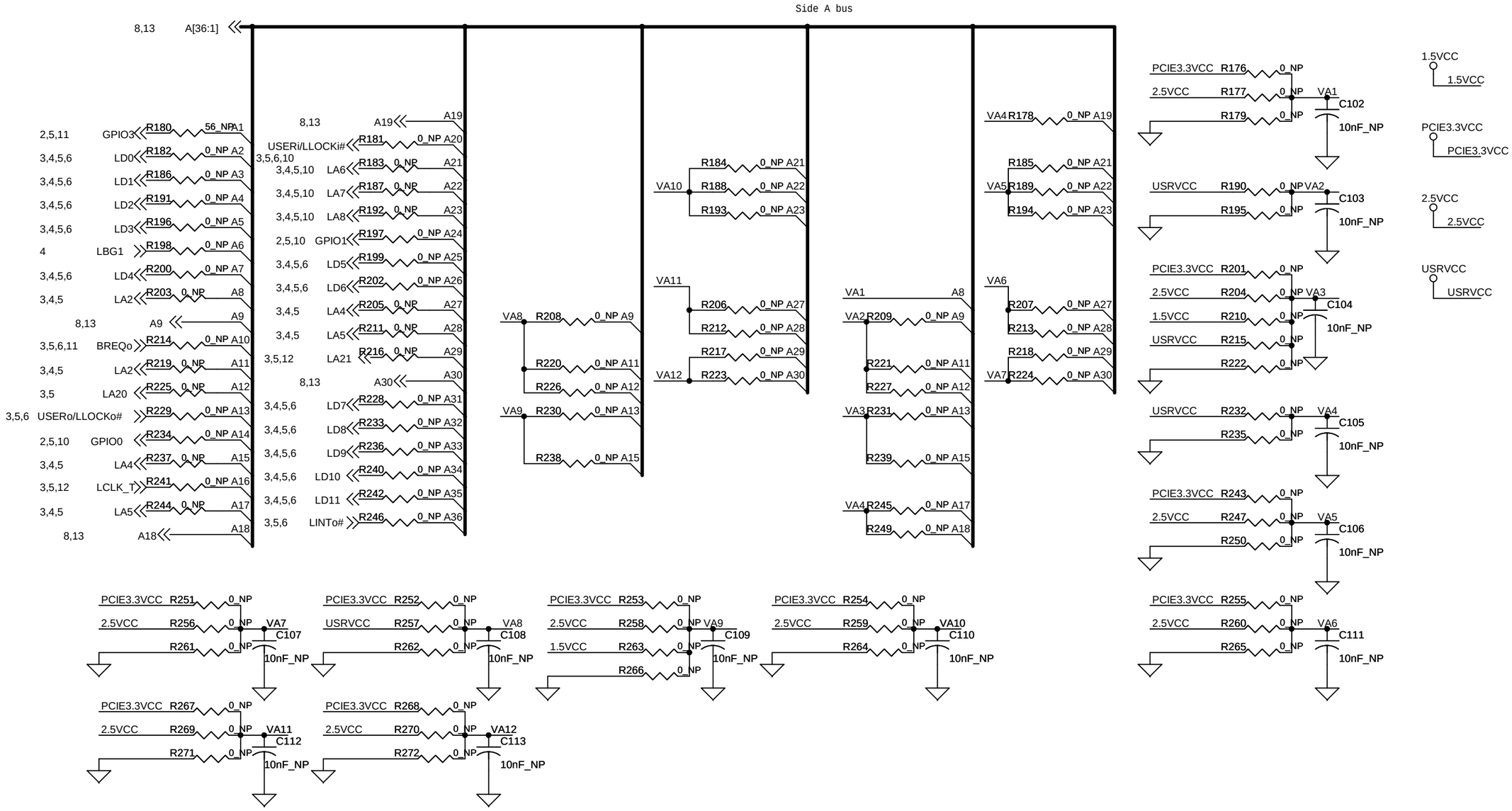




F_TDO — F_TDO 11
F_TDI — F_TDI 11
F_TMS — F_TMS 11
F_TCK — F_TCK 11

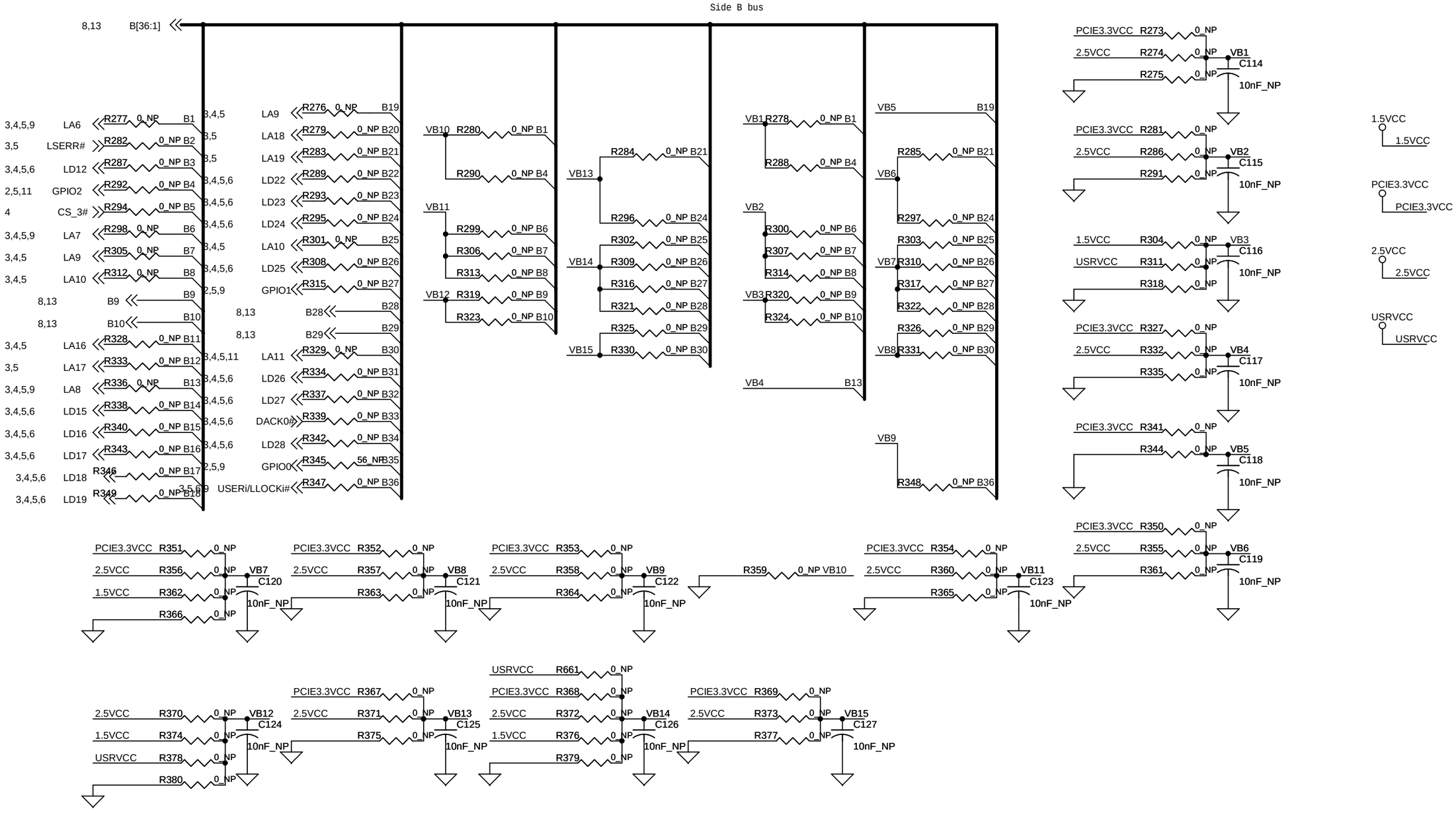
Title	FPGA Footprint	
Size: B	Document Number: <Doc> 91-0058-000-A	Rev: 000
Date: Wednesday, December 14, 2005	Sheet 8 of 15	

The components on this sheet are not installed by default.



Title	FPGA Side A resistor options	
Size B	Document Number <Doc> 91-0058-000-A	Rev 000
Date: Wednesday, December 14, 2005	Sheet 9 of 15	

The components on this sheet are not installed by default.



Title	FPGA Side B resistor options	
Size B	Document Number <Doc> 91-0058-000-A	Rev 000
Date: Wednesday, December 14, 2005	Sheet 10 of 15	

The components on this sheet are not installed by default.

Side C bus

8,13 C[36:1]

3,4,5,10	LA11	R386	0_NP	C1	3,5,6,9	BREQi	R385	0_NP	C19
3,4,5,6	LD29	R391	0_NP	C2	3,4,5	LA12	R388	0_NP	C20
3,4,5,6	LD30	R394	0_NP	C3	3,5,12	PMEIN#	R393	0_NP	C21
3,4,5,6	LD31	R397	0_NP	C4	3,4,5,6	BTERM#	R396	0_NP	C22
3,4,5,6	ADS#	R400	0_NP	C5	8	F_TDI	R399	0_NP	C23
3,4,5,6	DACK1#	R403	0_NP	C6	3	CCS#	R402	0_NP	C24
3,4,5	LA12	R405	0_NP	C7	3,4,5,6	DMPAF/EOT#	R404	0_NP	C25
8,13		C8			3,4,5,6	DREQ0#	R409	0_NP	C26
3,4,5,12	LA15	R416	0_NP	C9	3,4,5,12	LA13	R413	0_NP	C27
3,5	BIGEND#	R422	0_NP	C10	3,4,5,12	LA14	R419	0_NP	C28
3,4,5,6	BLAST#	R427	0_NP	C11	3,5,12	LA22	R424	0_NP	C29
3,4,5,6	LA31	R430	0_NP	C12	8,13		C30		
3,4,5,6	LA29	R433	0_NP	C13	3,5	DP0	R432	0_NP	C31
2,5,10	GPIO2	R436	0_NP	C14	3,5	DP1	R435	0_NP	C32
2,5,9	GPIO3	R439	0_NP	C15	3,5	DP2	R438	0_NP	C33
8	F_TCK	R442	0_NP	C16	3,5	DP3	R441	0_NP	C34
8	F_TMS	R445	0_NP	C17	3,4,5,6	LA30	R444	0_NP	C35
8	F_TDO	R450	0_NP	C18	3,4,5,12	LA3	R449	0_NP	C36

Note LA29=ALE (J Mode),
LA31= DT/R#(J Mode)

Note: LA30=DEN# (J Mode)

VC11 R389 0_NP C20

VC12 R414 0_NP C27
R420 0_NP C28
R425 0_NP C29
VC13 R428 0_NP C30

VC10 R406 0_NP C7
R410 0_NP C8
VC11 R446 0_NP C17
R451 0_NP C18

VC1 R387 0_NP C1

VC2 R407 0_NP C7
R411 0_NP C8
VC3 R417 0_NP C9

VC4 R443 0_NP C16
VC5 R447 0_NP C17
R452 0_NP C18

VC5 R390 0_NP C20

VC6 C23

VC7 R415 0_NP C27
R421 0_NP C28
R426 0_NP C29
VC8 R429 0_NP C30

VC9 C36

PCIE3.3VCC R381 0_NP
2.5VCC R382 0_NP VC1
USRVCC R383 0_NP C128
R384 0_NP 10nF_NP

PCIE3.3VCC R392 0_NP
2.5VCC R395 0_NP VC2
USRVCC R398 0_NP C129
R401 0_NP 10nF_NP

PCIE3.3VCC R408 0_NP
2.5VCC R412 0_NP VC3
USRVCC R418 0_NP C130
R423 0_NP 10nF_NP

PCIE3.3VCC R431 0_NP
2.5VCC R434 0_NP VC4
USRVCC R437 0_NP C131
R440 0_NP 10nF_NP

PCIE3.3VCC R448 0_NP
2.5VCC R453 0_NP VC5
USRVCC R454 0_NP C132
R455 0_NP 10nF_NP

1.5VCC
1.5VCC

PCIE3.3VCC
PCIE3.3VCC

2.5VCC
2.5VCC

USRVCC
USRVCC

PCIE3.3VCC R456 0_NP
2.5VCC R462 0_NP VC7
USRVCC R468 0_NP C133
R474 0_NP 10nF_NP

PCIE3.3VCC R457 0_NP
2.5VCC R463 0_NP VC8
USRVCC R469 0_NP C134
R475 0_NP 10nF_NP

PCIE3.3VCC R458 0_NP
2.5VCC R464 0_NP VC9
USRVCC R470 0_NP C135
R476 0_NP 10nF_NP

PCIE3.3VCC R459 0_NP
2.5VCC R465 0_NP VC10
USRVCC R471 0_NP C136
R477 0_NP 10nF_NP

PCIE3.3VCC R460 0_NP
2.5VCC R466 0_NP VC11
USRVCC R472 0_NP C137
R478 0_NP 10nF_NP

PCIE3.3VCC R461 0_NP
2.5VCC R467 0_NP VC6
USRVCC R473 0_NP C138
R479 0_NP 10nF_NP

PCIE3.3VCC R480 0_NP
2.5VCC R482 0_NP VC12
USRVCC R484 0_NP C139
R486 0_NP 10nF_NP

PCIE3.3VCC R481 0_NP
2.5VCC R483 0_NP VC13
USRVCC R485 0_NP C140
R487 0_NP 10nF_NP

Title
FPGA Side C resistor options

Size	Document Number	Rev
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The components on this sheet are not installed by default.

Side D bus

8,13 D[36:1]

3,4,5,11	LA15	R493	0_NP	D1	D19	R496	0_NP
3,5,9	LA21	R497	0_NP	D2	3,5,9	LCLK_T	
3,5	LA23	R502	0_NP	D3	D21	R505	0_NP
3,4,5,6	DREQ1#	R507	0_NP	D4	3,4,5,6	LW/R#	
4	LBR1	R510	0_NP	D5	3,4,5,6	LD14	R508	0_NP	D23
3,5	LA24	R513	0_NP	D6	3,4,5,6	READY#	R511	0_NP	D24
8,13	D7	D7			3,4,5	LA28	R516	0_NP	D25
3,4,5,11	LA13	R523	0_NP	D8	3,5,6	WAIT#	R521	0_NP	D26
3,4,5,11	LA14	R530	0_NP	D9	3,4,5,11	LA3	R526	0_NP	D27
8,13	D10	D10			3,4,5	LA28	R533	0_NP	D28
3,5	LA25	R542	0_NP	D11	8,13	D29	D29		
3,5	LA26	R548	0_NP	D12	8,13	D30	D30		
3,5,11	LA22	R554	0_NP	D13	3,4,5,6	LD20	R551	0_NP	D31
3,4,5,6	LD13	R558	0_NP	D14	3,4,5,6	LD21	R555	0_NP	D32
3,5,6	LINTi#	R563	0_NP	D15	3,5	LA27	R559	0_NP	D33
3,5,6	LRESET#	R568	0_NP	D16	3,4,5,6	LBE#2	R564	0_NP	D34
3,4,5,6	LBE#0	R573	0_NP	D17	3,4,5,6	LBE#3	R569	0_NP	D35
3,4,5,6	LBE#1	R578	0_NP	D18	3,5,11	PMEIN#	R574	0_NP	D36

VD9	R494	0_NP	D1	VD1	R495	0_NP	D1
	R498	0_NP	D2		R499	0_NP	D2
	R503	0_NP	D3		R504	0_NP	D3
VD10				VD2			
	R514	0_NP	D6		R515	0_NP	D6
	R519	0_NP	D7		R520	0_NP	D7
	R524	0_NP	D8		R525	0_NP	D8
VD11	R531	0_NP	D9	VD3	R532	0_NP	D9
	R537	0_NP	D10		R538	0_NP	D10
	R543	0_NP	D11		R544	0_NP	D11
	R549	0_NP	D12		R550	0_NP	D12
VD12	R517	0_NP	D25	VD4			D13
	R527	0_NP	D27	VD5			D19
	R534	0_NP	D28	VD6	R518	0_NP	D25
	R539	0_NP	D29		R528	0_NP	D27
VD13	R545	0_NP	D30		R535	0_NP	D28
	R552	0_NP	D31		R540	0_NP	D29
	R556	0_NP	D32	VD7	R546	0_NP	D30
	R560	0_NP	D33		R553	0_NP	D31
VD14	R565	0_NP	D34		R557	0_NP	D32
	R570	0_NP	D35		R561	0_NP	D33
	R575	0_NP	D36	VD8	R566	0_NP	D34
					R571	0_NP	D35
					R576	0_NP	D36

PCIE3.3VCC R488 0_NP
2.5VCC R489 0_NP VD1
USRVCC R490 0_NP C141
R491 0_NP 10nF_NP

PCIE3.3VCC R501 0_NP
2.5VCC R506 0_NP VD2
USRVCC R509 0_NP C142
R512 0_NP 10nF_NP

PCIE3.3VCC R522 0_NP
2.5VCC R529 0_NP VD3
1.5VCC R536 0_NP C143
USRVCC R541 0_NP 10nF_NP
R547 0_NP

PCIE3.3VCC R562 0_NP
2.5VCC R567 0_NP VD4
USRVCC R572 0_NP C144
R577 0_NP 10nF_NP

PCIE3.3VCC R579 0_NP
2.5VCC R584 0_NP VD5
USRVCC R589 0_NP C145
R594 0_NP 10nF_NP

PCIE3.3VCC R599 0_NP
2.5VCC R600 0_NP VD6
1.5VCC R605 0_NP C150
USRVCC R610 0_NP 10nF_NP
R615 0_NP

1.5VCC
1.5VCC

PCIE3.3VCC
PCIE3.3VCC

2.5VCC
2.5VCC

USRVCC
USRVCC

PCIE3.3VCC R580 0_NP
2.5VCC R585 0_NP VD7
USRVCC R590 0_NP C146
R595 0_NP 10nF_NP

PCIE3.3VCC R581 0_NP
2.5VCC R586 0_NP VD8
USRVCC R591 0_NP C147
R596 0_NP 10nF_NP

PCIE3.3VCC R582 0_NP
2.5VCC R587 0_NP VD9
USRVCC R592 0_NP C148
R597 0_NP 10nF_NP

PCIE3.3VCC R583 0_NP
2.5VCC R588 0_NP VD10
USRVCC R593 0_NP C149
R598 0_NP 10nF_NP

PCIE3.3VCC R601 0_NP
2.5VCC R606 0_NP VD11
1.5VCC R611 0_NP C151
USRVCC R616 0_NP 10nF_NP
R620 0_NP

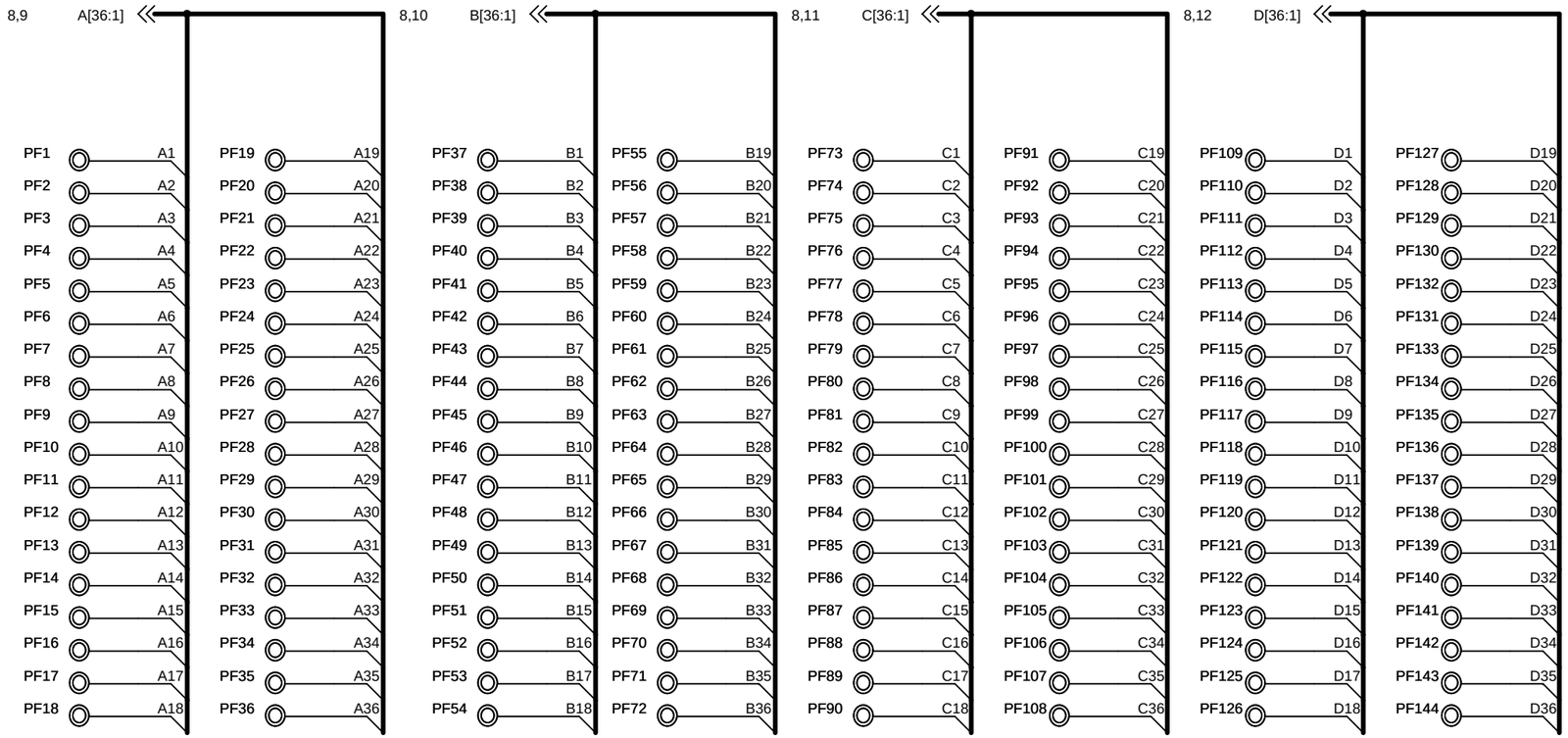
PCIE3.3VCC R602 0_NP
2.5VCC R607 0_NP VD12
1.5VCC R612 0_NP C152
USRVCC R617 0_NP 10nF_NP
R621 0_NP

PCIE3.3VCC R603 0_NP
2.5VCC R608 0_NP VD13
USRVCC R613 0_NP C153
R618 0_NP 10nF_NP

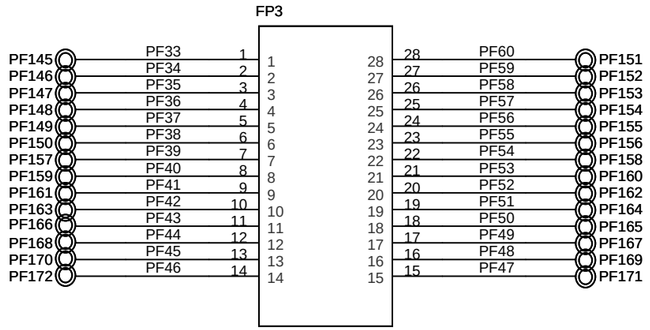
PCIE3.3VCC R604 0_NP
2.5VCC R609 0_NP VD14
USRVCC R614 0_NP C154
R619 0_NP 10nF_NP

Title	FPGA Side D resistor options		
Size B	Document Number <Doc> 91-0058-000-A		Rev 000
Date: Wednesday, December 14, 2005	Sheet 12 of 15		

The components on this sheet are not installed by default.

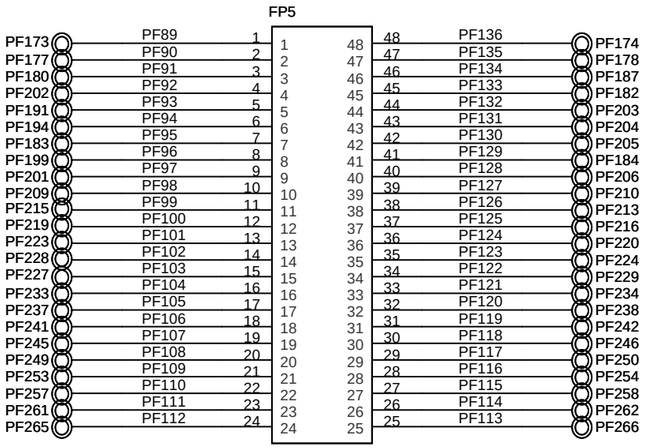


Title	PADS	
Size B	Document Number <Doc> 91-0058-000-A	Rev 000
Date: Wednesday, December 14, 2005	Sheet 13 of 15	

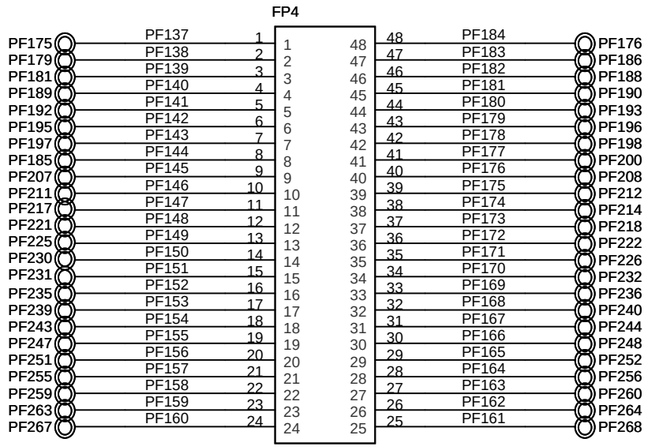


28-pin SOIC, 0.05" pitch

20X10 0.1" c-c Through hole Prototype Area



48-pin SSOP, 0.025" pitch



48-pin SSOP, 0.025" pitch

Title	Prototype Footprint	
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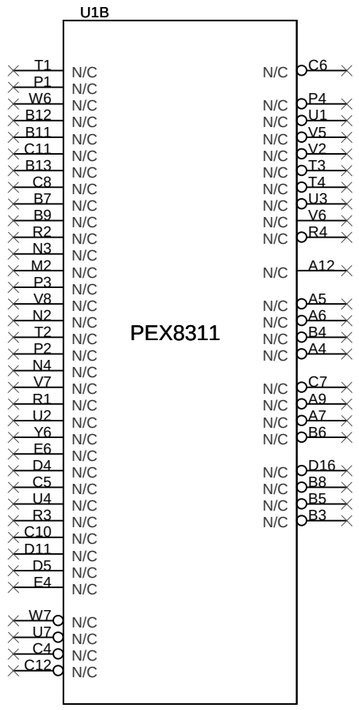

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