Design Notes Documentation

A. Product Status

Product	Revision	Description	Samples	Production
PCI9030	PCI9030-AA60PI	Released 176-pin PQFP Product	Mar 2000	April 2000
PCI9030	PCI9030-AA60BI	Released 180-pin μBGA Product	Mar 2000	April 2000

B. Documentation Status

Document	Revision	Description	Date
Data Book	1.4	PCI 9030 Data Book	May 2002

C. Design Notes Summary:

#	Description
1	Power Management Interface Specification version support
2	VPD Implementation (revised from Rev. 1.1)

D. Design Notes:

1. Power Management Interface Specification version support

Design Issue: The PCI 9030 Data Book indicates compliance with the PCI Power Management Interface Specification revision 1.1, however the PMC register description is compliant with revision 1.0. The PCI 9030 can support either revision. The only differences between these revisions, with respect to PCI 9030 support, are the Version bits [2:0] value (programmable by EEPROM), and the descriptions for bits [8:6, 4] for which the values are read-only and return a value of 0 regardless of revision. The Version bits value (001b or 010b), which has no effect on PCI 9030 operation, is used by software to determine PMC register format.

Recommendation: PMC register descriptions for revisions 1.0 and 1.1 are listed below. If revision 1.1 rather than revision 1.0 is to be supported, program the serial EEPROM with the Version value (010b) to overwrite the PMC register default value, by changing the 32-bit value at EEPROM offset 18h from 48014801h to 48024801h.

Register 10-27. (PMC; PCI:42h) Power Management Capabilities *(PCI Power Mgmt. r1.0)*

Bit	Description	Read	Write	Value after Reset
2:0	**Version.** The value 001 indicates compliance with *PCI Power Mgmt. r1.0*.	Yes	Serial EEPROM	001
3	**PCI Clock Required for PME# Signal.** When set to 1, indicates a function relies on PCI clock presence for PME# operation. The PCI 9030 does not require the PCI clock for PME#, so this bit should set to 0.	Yes	Serial EEPROM	0
4	**Auxiliary Power Source.** Because the PCI 9030 does not support PME# while in a D3cold state, this bit is always set to 0. ***Not Supported.***	Yes	No	0
5	**Device-Specific Initialization (DSI).** When set to 1, the PCI 9030 requires special initialization following a transition to a D0 uninitialized state before a generic class device driver is able to use it.	Yes	Serial EEPROM	0
8:6	***Reserved.***	Yes	No	000
9	**D1_Support.** When set to 1, the PCI 9030 supports the D1 power state. ***Not Supported.***	Yes	No	0
10	**D2_Support**. When set to 1, the PCI 9030 supports the D2 power state. ***Not Supported.***	Yes	No	0
15:11	**PME Support.** Indicates power states in which the PCI 9030 may assert PME#. Values: XXXX1 = PME# can be asserted from D0 XXXXX = The PCI 9030 does not support the D1 power state XXXXX = The PCI 9030 does not support the D2 power state X1XXX = PME# can be asserted from D3hot XXXXX = PME# cannot be asserted from D3cold	Yes	[14:11]: Serial EEPROM [15]: No	01001

Register 10-27. (PMC; PCI:42h) Power Management Capabilities *(PCI Power Mgmt. r1.1)*

Bit	Description	Read	Write	Value after Reset
2:0	**Version.** The default value 001 indicates compliance with *PCI Power Mgmt. r1.0*. To instead indicate PMC register format compliance with Revision 1.1, this value should be set to 010.	Yes	Serial EEPROM	001
3	**PCI Clock Required for PME# Signal.** When set to 1, indicates a function relies on PCI clock presence for PME# operation. The PCI 9030 does not require the PCI clock for PME#, so this bit should set to 0.	Yes	Serial EEPROM	0
4	***Reserved.***	Yes	No	0
5	**Device-Specific Initialization (DSI).** When set to 1, the PCI 9030 requires special initialization following a transition to a D0 uninitialized state before a generic class device driver is able to use it.	Yes	Serial EEPROM	0
8:6	**Aux_Current.** Supported by way of the PMDATA register per *PCI Power Mgmt. r1.1.*	Yes	No	000
9	**D1_Support.** When set to 1, the PCI 9030 supports the D1 power state. ***Not Supported.***	Yes	No	0
10	**D2_Support.** When set to 1, the PCI 9030 supports the D2 power state. ***Not Supported.***	Yes	No	0
15:11	**PME Support.** Indicates power states in which the PCI 9030 may assert PME#. Values: XXXX1 = PME# can be asserted from D0 XXXXX = The PCI 9030 does not support the D1 power state XXXXX = The PCI 9030 does not support the D2 power state X1XXX = PME# can be asserted from D3hot XXXXX = PME# cannot be asserted from D3cold	Yes	[14:11]: Serial EEPROM [15]: No	01001

2. VPD Implementation

Design Issue: The PCI 9030 supports the Vital Product Data (VPD) optional feature detailed in PCI Specification r2.2 Appendix I. The PCI 9030 VPD feature supports storage of a VPD data structure within a serial EEPROM (2k- or 4k-bit, 4-wire interface). The information contained in separate Read-Only and Writable sections of this data structure can include items such as Add-in Card Part Number, EC Level of the Add-in Card, Manufacture ID, Serial Number, Extended Capability, and Vendor Specific definitions. CompactPCI boards can additionally include Fabric Geography, PCI Geography, and Location information.

The PCI Specification requires that the VPD registers (PCI 9030 PVPDAD and PVPDATA address and data registers in PCI Configuration Space) be used only for VPD data. Any consequence in using the VPD feature for anything other than VPD data (such as PCI 9030 configuration data) is left to the silicon designer. PLX has no restriction in using the VPD mechanism to read/write PCI 9030 configuration data in the serial EEPROM. The PCI 9030 additionally provides CNTRL[27:24] register bits to allow programming of configuration data within the EEPROM, without using the VPD registers.

The PCI Specification also requires that the first element within the VPD data structure be the Identifier String (Product Name) at VPD address 0h. At power-up reset, the PCI 9030 reads 136 bytes of configuration data from a serial EEPROM, beginning with the PCI Device ID value stored at EEPROM address 0h. Although this address seemingly conflicts with VPD requirements, PLX choose to store configuration data beginning at address 0, in order to maintain compatibility with previous chips (such as PCI 9052).

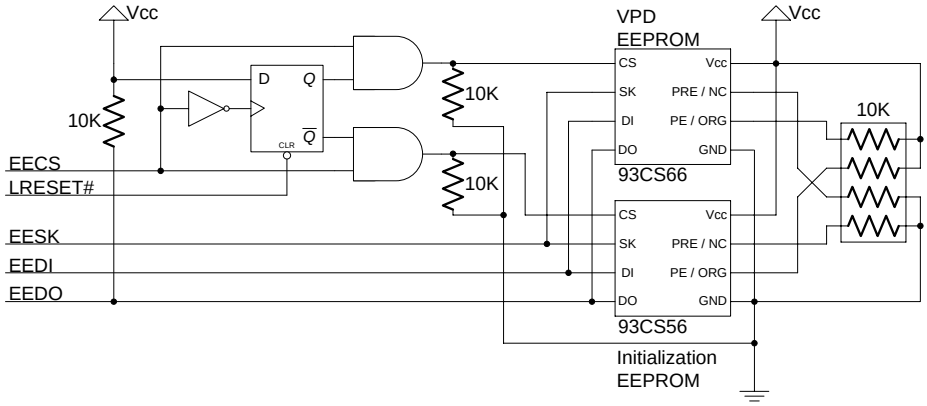
The issue is that if system software scans the PCI Capabilities linked list and sees the VPD Capability present, VPD software may try to access a VPD data structure at offset 0h. If no data structure is present, the read should return 0, but of course this read will return the Device/Vendor ID, assuming the EEPROM is programmed. If a valid VPD data structure were present, the value of the first byte (in byte 0 of PVPDATA, stored in byte 2 of the EEPROM where the lower byte of the Vendor ID resides), must be 82h. The VPD Read-Only section of data must terminate with a Checksum byte for which the sum of all byte values from VPD address 0 through the Checksum byte is zero.

Since the VPD data structure format is specifically defined, VPD software attempting to read VPD data will not successfully parse PCI 9030 configuration data.

Recommendation: VPD data storage can be implemented with a serial EEPROM used exclusively for VPD (and not containing PCI 9030 configuration data). Because the PCI 9030 will attempt to read configuration data through the serial EEPROM interface at power-up reset, the VPD EEPROM should not be enabled until PCI 9030 initialization completes (when EECS de-asserts).

The following sample circuit includes two serial EEPROMs, one for initialization and the other for VPD, with only one EEPROM enabled at any time. The circuit initially enables the optional Initialization EEPROM during power-up reset. After the first EECS de-assertion, the circuit enables access to the VPD EEPROM and disables access to the Initialization EEPROM. The D flip-flop and inverter can both be replaced by a negative edge-triggered J-K flip-flop such as the 74HCT107, with its J input tied high and its K input tied low.

Sample VPD implementation circuit



To allow programming of the Initialization EEPROM, the circuit can be modified such that the flip-flop CLR input is driven by the output of an AND gate instead of from LRESET# directly, with LRESET# connected to one of the AND gate inputs. If any AND gate input is low, the gate output is low, which will enable the Initialization EEPROM and disable the VPD EEPROM.

The PCI 9030 will reload its configuration registers from serial EEPROM if the Reload Configuration Registers register bit (CNTRL[29]) is transitioned from 0 to 1, or when its Power State (PMCSR[1:0]) is transitioned from D3hot to D0 state. Transitioning the Power State from D3hot to D0 state causes LRESET# assertion, and therefore the circuit will correctly access the Initialization EEPROM in such case. Prior to any setting of the Reload Configuration Registers bit, the designer should ensure that Initialization EEPROM access is enabled, since PCI 9030 registers must be reloaded with configuration data and not VPD data.