PEX 8112RDK-F

Hardware Reference Manual

For Board Revision 1.0

Version 1.1

March 2008

Website: www.plxtech.com
Technical Support: www.plxtech.com/support

Order Number: PEX 8112-RDK/F-HRM -1.1

Printed in the USA, March 2008

CONTENTS

FIGURES

TABLES

PREFACE

NOTICE

This document contains PLX Confidential and Proprietary information. The contents of this document may not be copied nor duplicated in any form, in whole or in part, without prior written consent from PLX Technology, Inc.

PLX provides the information and data included in this document for your benefit, but it is not possible to entirely verify and test all the information, in all circumstances, particularly information relating to non-PLX manufactured products. PLX makes neither warranty nor representation relating to the quality, content, or adequacy of this information. The information in this document is subject to change without notice. Although every effort has been made to ensure the accuracy of this manual, PLX shall not be liable for any errors, incidental or consequential damages in connection with the furnishing, performance, or use of this manual or examples herein. PLX assumes no responsibility for damage or loss resulting from the use of this manual, for loss or claims by third parties, which may arise through the use of the PEX 8112RDK-F, or for any damage or loss caused by deletion of data as a result of malfunction or repair.

ABOUT THIS MANUAL

This document describes the PLX PEX 8112RDK-F, the PEX 8112 Forward Bridge RDK board Rapid Development Kit, from a hardware perspective. It contains a description of all major functional circuit blocks on the board and also is a reference for the creation of software for this product. This manual also includes a complete bill of materials and schematics.

REVISION HISTORY

Date	Version	Comments
April 2007	0.5	Initial release. Supports Board Revision 1.0.
June 2007	1.0	Updated with feedbacks. Supports Board Revision 1.0
March 2006	1.1	Updated the Power Scheme in section 2 and Fixed an error in section 3.6.

1. General Information

The PLX PEX 8112RDK-F is a Rapid Development Kit based on the PEX 8112, a single-lane, PCI Express-to-PCI bridge device. The PEX 8112RDK-F provides a complete hardware and software development platform to facilitate getting designs up and running quickly, lowering risk and reducing time-to-market. The PEX 8112RDK-F allows the PEX 8112 bridge device upstream PCI Express port to be connected to a host system slot by way of a standard PCI Express edge connector (the PEX 8112RDK-F is designed to plug into a PCI Express motherboard slot). The PEX 8112RDK-F (shown in Figure 1) also allows for up to four PCI adapters to be plugged into the downstream bus, by way of four standard PCI slots residing on the PEX 8112RDK-F.

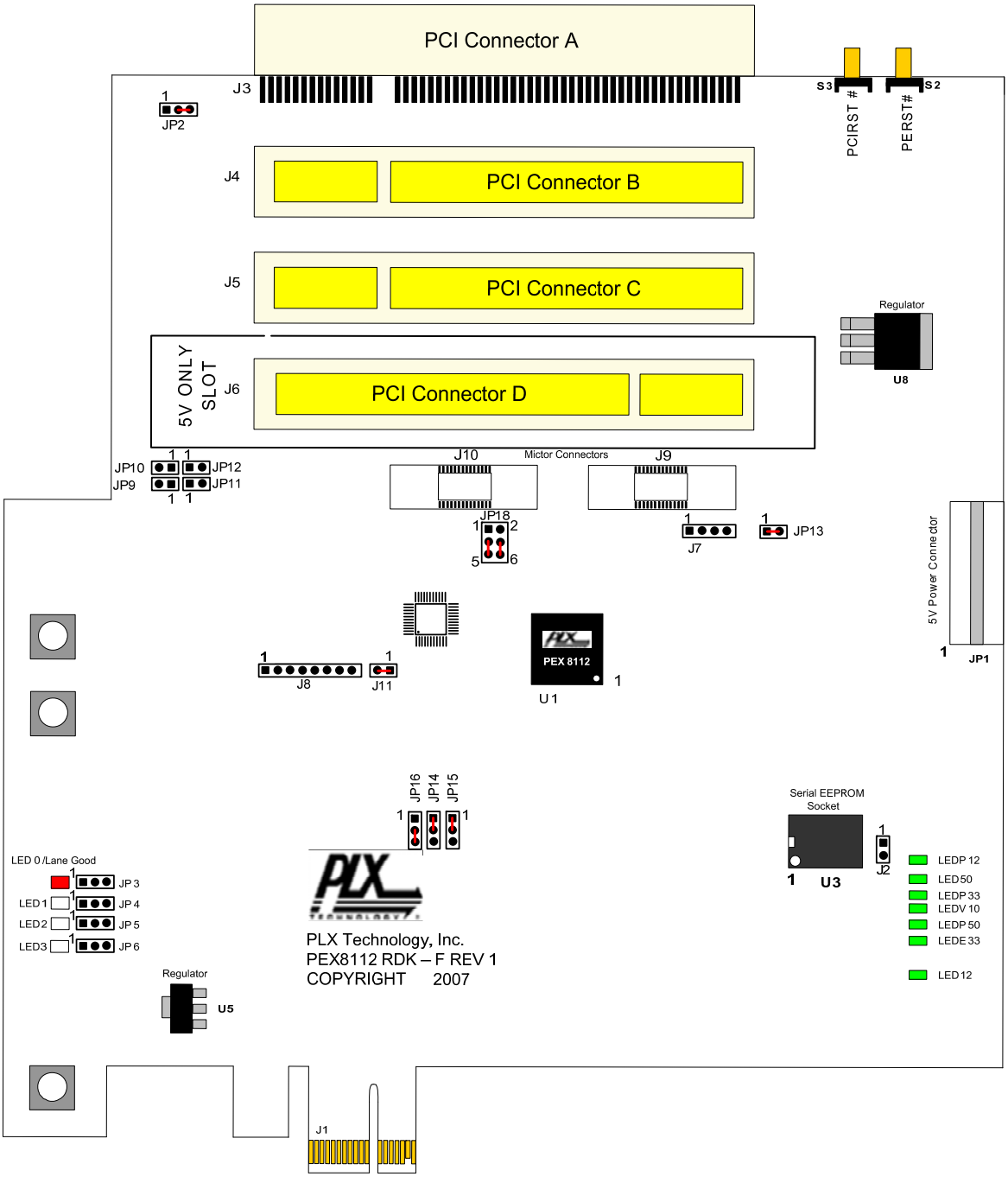


Figure 1. PEX 8112RDK-F – Component Side View

1.1 PEX 8112 Features

- Compliant to the following specifications:
  - *PCI Express Base Specification, Revision 1.0a*
  - *PCI Express to PCI Bridge Specification, Revision 1.0*
  - *PCI Local Bus Specification, Revision 3.0*
- Small package, enabling compact design
- Supports Forward and Reverse Bridging, allowing systems to migrate to PCI Express and leverage software compatibility

  Note: *The PEX 8112RDK-F is for Forward Mode designs. For Reverse Mode designs, refer to the PEX 8112RDK-R.*
- Integrated PCI Express interface with x1 link, dual-simplex 2.5 Gbps SerDes
- Single PCI Express port, capable of x1 link width
- Single PCI Bus segment supporting PCI protocol at 32-bit/66 MHz
- Low power consumption, meeting designers' demands for reduced power draws
- 3.3V I/O and 5V tolerant PCI
- Serial EEPROM configuration option with Serial Peripheral Interface (SPI)
- 8-KB general-purpose shared RAM

1.2 PEX 8112RDK-F Features

- PLX PCI Express-to-PCI bridge device in a 13 x 13 mm, 144-ball PBGA package
- Form factor based on the *PCI Local Bus Specification, Revision 3.0*
- Single x1 PCI Express Edge connector for insertion into standard PCI Express slot of x1 or greater link width
- Four downstream 32-bit PCI slots
- Socketable SPI serial EEPROM (3.3V devices supported)
- Onboard probing points and logic analyzer connections
- LEDs for link status visual inspection
- Auxiliary hard disk power connector for additional power requirement support

2. PEX 8112RDK-F System Architecture

The PEX 8112RDK-F assists customers in evaluating PLX Technology's PEX 8112 PCI Express-to-PCI bridge device, and to facilitate early development of customer designs with the PEX 8112. The usage configuration is forward bridging between a PCI Express base board and PCI add-in boards. The PEX 8112RDK-F is designed to showcase all PEX 8112 features when operating in Forward Bridge mode.

The PEX 8112RDK-F's form factor is based on the *PCI Local Bus Specification, Revision 3.0*. The PCI interface supports up to 32-bit transfers, at up to 66 MHz. The PEX 8112RDK-F has four PCI slot (female) connectors – one straddle mount, and three baseboard mount. Four INT# and four REQ#/GNT# pairs are supported, one for each slot. The PCI Express interface supports one lane operating at 2.5 Gbps.

The PEX 8112RDK-F +1.5VDC is generated from +3.3 VDC, provided through the PCI Express edge connector. Limited PCI +5 VDC power is generated from +12 VDC, provided through the PCI Express edge connector. Limited PCI -12 VDC power is generated from +5 VDC that was generated. PCI +3.3 VDC and +12 VDC are provided through the PCI Express edge connector. If PCI bus power demands are beyond the capability of onboard circuitry, PCI bus power can be supplied from a 4-pin hard disk power connector. When in default setting, plug in the 4-pin hard disk power connector (JP1). This provides the necessary voltages to power up the PEX 8112RDK-F.

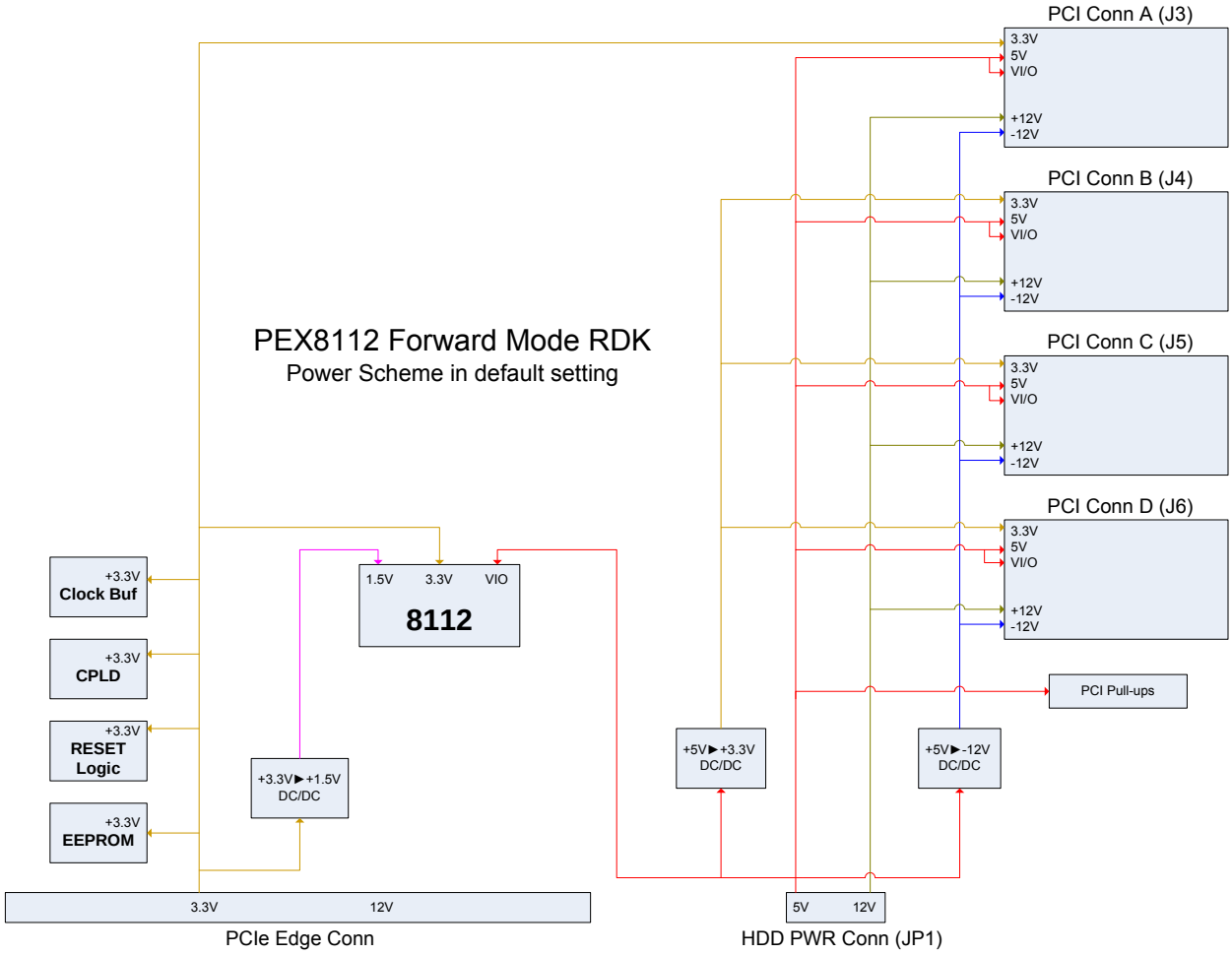


Figure 2. PEX 8112 Forward Mode RDK Power Scheme

3. PEX 8112RDK-F Hardware Architecture

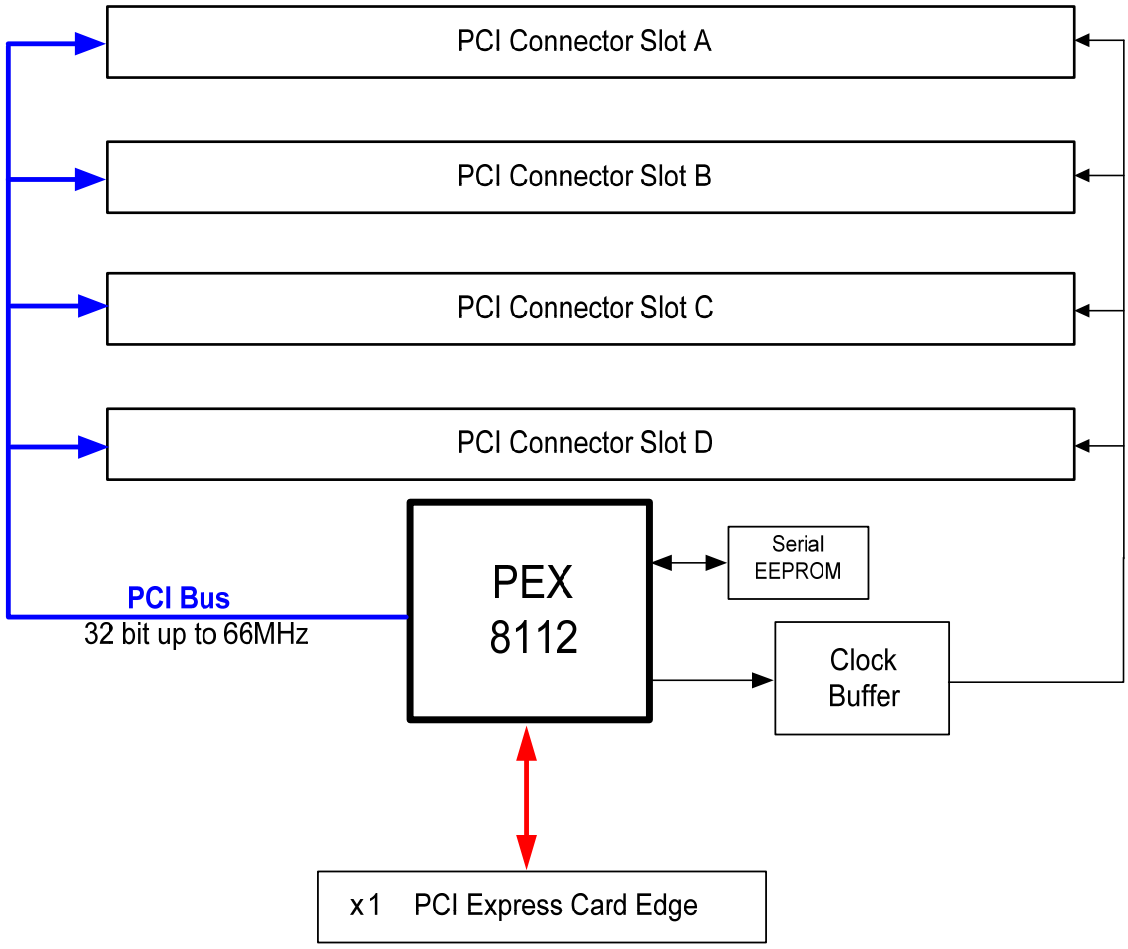


Figure 3. PEX 8112RDK-F Hardware Architecture

3.1 PEX 8112 PCI Express Bridge Device

The PEX 8112 is a high-performance bridge, designed to the *PCI Express-to-PCI Bridge Specification 1.0*, that enables designers to migrate legacy PCI Bus interfaces to the new, advanced serial PCI Express. This 2-port device is equipped with a single-lane PCI Express port and a parallel bus segment supporting Conventional PCI operation. The PEX 8112 is capable of operating in Forward and Reverse Bridging modes. The PEX 8112 bridge device is housed in a 13 x 13 mm, 144-ball PBGA package. Ball spacing is 1.0 mm. No additional cooling is required.

3.2 Serial EEPROM

The PEX 8112 bridge device has an SPI serial EEPROM, which can be used to load configuration data from a serial EEPROM on power-up. However, a serial EEPROM is not needed to bring up the PEX 8112. This interface is connected to an 8-pin DIP socket (U3), which houses the serial EEPROM. A pull-up resistor (R3) on the EERDDATA ball produces a value of FFh if there is no serial EEPROM installed.

The PEX 8112 supports up to 16-MB serial EEPROMs, utilizing 1, 2, or 3-byte addressing. The PEX 8112 automatically determines the appropriate addressing mode. The SPI operates at up to 25 MHz and can directly interface with the PEX 8112. The Atmel AT25640 device is recommended. Other compatible 128-byte serial EEPROMs include the Atmel AT25010A, Catalyst CAT25C01, and ST Microelectronics M95010W.

3.3 PCI Interface

The PCI interface is set up in a four-slot motherboard arrangement. Each slot has its own REQ#/GNT# pair, which can be arbitrated by the PEX 8112. The clock buffer drives individual PCI clocks to each slot.

3.3.1 Slot Connectors

This PEX 8112RDK-F has four female PCI slots, which connect to the PEX 8112 downstream port. (Refer to Figure 4.) Connector J3 is a straddle-mount (SMT) connector. Cards plugged into this slot are oriented parallel to the PEX 8112RDK-F. Connectors J4, J5, and J6 are vertical-mount (SMT) connectors. Cards plugged into these slots are oriented perpendicular to the RDK. All slots support up to 32-bit data transfers and use 5V-compatible PCI connectors. Connector J6 is strictly a 5V connector. All four slots support up to 66-MHz transfers. Power is provided to all connectors from the hard disk power connector, JP1.

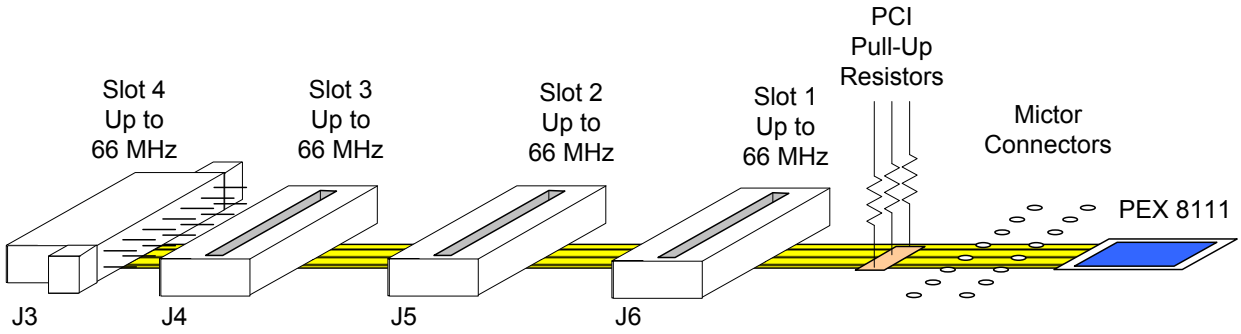


Figure 4. PEX 8112RDK-F Slots Diagram

3.3.2 PCI Terminations

The four PEX 8112 REQ# inputs are pulled up with 2.7K-Ohm resistors, to hold these lines for unpopulated slots.

3.3.3 PCI Clock

The PEX 8112 has only one output PCI clock, PCLKO. The Cypress Semiconductor CY2309 Zero Delay 1-to-9 clock buffer (U2) provides onboard PCI clock distribution to the PEX 8112, connectors J3, J4, J5, J6 and other circuits. The CY2309 input is sourced by PCLKO from the PEX 8112. Depending on the voltage level of M66EN input to PEX 8112, either 33 MHz or 66 MHz from the PCLKO of PEX 8112 is used as PCI clock source fan out from the CY2309 to connectors J3 to J6.

3.4 PCI Express Interface

The PCI Express interface is a male card edge connector, based on the *PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a* for an x1 interface. The card edge provides +12 VDC and +3.3 VDC, RefClk, and PERST#. The PCI Express lanes are laid out as 100-Ohm, controlled-impedance, microstrip-differential pairs. Trace length mismatch within signal pairs is not greater than 0.005".

3.4.1 RefClk

PCI Express RefClk enters the PEX 8112RDK-F through the PCI Express card edge (male) connector. RefClk is laid out as a 100-Ohm, controlled-impedance, microstrip-differential pair. Trace length mismatch is not greater than 0.005".

3.4.2 PERST#

PERST# is the fundamental Reset signal to the PEX 8112, from the PCI Express edge connector.

3.5 LED Indicators

The PEX 8112RDK-F provides several LED indicators, including power-on indication and programmable PEX 8112 GPIO lane status indication. Table 1 provides a quick explanation of each LED indicator.

Table 1. PEX 8112RDK-F LED Indicators

Indicator Type	Location	LED ON
Board Power Indication	LED12	12V power is on
	LED50	Optional PCI 5V power for J3 PCI slot
	LEDE33	PCI Express 3.3V power is on
	LEDP12	PCI 12V power on
	LEDP33	PCI 3.3V power is on
	LEDP50	PCI 5V power is on
	LEDVIO	VI/O power is on
GPIO	LED0	Output OFF (0) – Link Down ON (1) – Link Up
	LED1	Input
	LED2	Input
	LED3	Input

3.6 PEX 8112RDK-F Power

The PEX 8112RDK-F has two sources for DC power. The first source is the card edge connector (J1). This x1 connector provides up to 500 mA at +12V, and 3.0A at +3.3V. Card edge power is intended to power only PEX 8112RDK-F components, as well as optional PCI connector A (J3).

The second source, the 4-pin hard disk power connector, provides +12V, -12V, and +5V DC power. The +5V is converted down to +3.3V and -12V for slots J4, J5, and J6. The +12V power rail is used directly.

3.6.1 PEX 8112 Bridge Device Power

The PEX 8112 bridge device power consists of the following:

- VDD Core +1.5 VDC ±0.1V
- VDD I/O +3.3 VDC ±10%
- VIO Clamp +5 VDC for 5V PCI
  +3.3 VDC for 3.3V PCI

3.7 Power Management Signaling

PCI devices assert the PME# pin (connected to the PEX 8112 PMEIN# ball) to signal a Power Management event. The PEX 8112 converts the PME# signal to PCI Express Power Management Event (PME) messages. There are no internal events that cause a PME message to be sent upstream.

Power Management messages are used to support PMEs signaled by devices downstream of the PEX 8112. System software needs to identify the source of a PCI PME reported by a PM_PME message. When the PME comes from an agent on a PCI Bus, then the PM_PME Message Requester ID reports the Bus Number from which the PME was collected, and the Device Number and Function Number reported must both be zero (0).

When the PME message is sent to the host, the **PWRMNGCSR** register *PME Status* bit is set and a 100-ms timer is started. If the status bit is not cleared within 100 ms, another PME message is sent.

When the upstream device is powering down the downstream devices, it first places all devices into the $D3_{hot}$ state. It then sends a PCI Express PME_Turn_Off message. After the PEX 8112 receives this message, it stops sending PME messages upstream. The PEX 8112 then sends a PME_TO_Ack message to the upstream device and places its link into the L2/L3 Ready state. The downstream device is now ready to be powered down. If the upstream device changes the PEX 8112 power state back to D0, PME messages are re-enabled. The PCI Express PME_Turn_Off message terminates at the PEX 8112, and is not communicated to the PCI devices. The PEX 8112 does not issue a PM_PME message on behalf of a downstream PCI device while its upstream link is in the L2/L3 non-communicating state.

To avoid loss of PME# assertions in the conversion of the level-sensitive PME# signal to the edge- triggered PCI Express PM_PME message, the PCI PME# signal is polled every 256 ms by the PEX 8112 and a PCI Express PM_PME message is generated if PME# is asserted.

The PMEIN# ball is used only when the PEX 8112 is in Forward Bridge Mode.

3.7.1 Wakeup

The PEX 8112 asserts the WAKEOUT# signal or sends a PCI Express beacon for the following:

- PCI PME# pin is asserted while link is in L2 state
- PCI Express beacon is received while link is in L2 state
- PCI Express PM_PME Message is received

A beacon is transmitted if the following are true:

- PCI PME# pin is asserted while link is in L2 state
- **DEVSPECCTL** register *Beacon Generate Enable* bit is set
- **PWRMNGCSR** register *PME Enable* bit is set

The WAKEOUT# signal is used only when the PEX 8112 is in Forward Bridge mode.

4. MECHANICAL ARCHITECTURE

4.1 Monitoring Point, Indicator, Control, and DIP Switch Summary

This section summarizes the interfaces available on the PEX 8112RDK-F for controlling and monitoring PEX 8112 performance.

4.1.1 Monitoring Points

- Six ground post holes, scattered across the PEX 8112RDK-F to provide probe reference points
- Voltages to the PEX 8112 can be monitored at the following locations:
  - TP12 (1.5 VCC)
  - TP13 (PCI Express 3.3 VCC)
  - TP14 (PCI Express 5 VCC)
- PCI bus power can be monitored at the hard disk power connector (JP1)
- J7 – Test points for TCK, TDI, TDO, and TMS
- J9, J10 – footprints of mictor connectors, for PCI bus signal probing.

4.1.2 Indicators

- GPIO indicators – LED[3:0]

4.1.3 Controls

Table 2. PEX 8112RDK-F Default Jumper Settings

Jumper	Factory Setting	Description
J2	OPEN	Pull-up WP# on the serial EEPROM
JP2	2-3	Connect VI/O to 5V
JP3	OPEN	Pull-up (1-2) or pull-down (2-3) GPIO0
JP4	OPEN	Pull-up (1-2) or pull-down (2-3) GPIO1
JP5	OPEN	Pull-up (1-2) or pull-down (2-3) GPIO2
JP6	OPEN	Pull-up (1-2) or pull-down (2-3) GPIO3
JP9	OPEN	Do not ground INTC#
JP10	OPEN	Do not ground INTD#
JP11	OPEN	Do not ground INTB#
JP12	OPEN	Do not ground INTA#
JP13	1-2	Connect M66EN
JP14	1-2	Pull-up the buffer gate input connected to GPIO2
JP15	1-2	Pull-up the buffer gate input connected to GPIO3
JP16	2-3	FF-OE# drives the buffer OE#
JP17	OPEN	Do not ground BAR0ENB# ***Note:*** *BAR0ENB# can be set by connecting JP17, or programmed through the serial EEPROM.*
J11	Not installed	Hard wire jump 1-2 of J11 for enabling internal PCI arbiter of the PEX 8112
JP8	Not installed	JTAG port of U6
JP18	Not installed	Hard wire jump 3-5 and 4-6 of JP18 for use of the internal PCI arbiter of PEX 8112

4.1.4 Tact Switches

The PEX 8112RDK-F contains two user-controllable Tact switches (S2 and S3) for reset control. The S2 switch can be pressed to ground RSTB#. The S3 switch can be pressed to ground PCIRSTB#.

4.2 PEX 8112RDK-F Layout Information

4.2.1 Trace Routing Design Rules

The characteristic trace impedances are within the PCI Express specification (100 Ohm ±5%) for the differential, and within the PCI specification (57 Ohm ±5%) for the single-ended.

4.2.2 Power Decoupling

Power decoupling is provided by two means – plane capacitance (provided by the PCB stackup) and discrete decoupling capacitors. Plane capacitance filters noise above approximately 100 MHz. The footprints for the discrete decoupling capacitors are designed such that the inductance between the pad and plane is reduced by careful via placement. (Refer to Figure 5.)

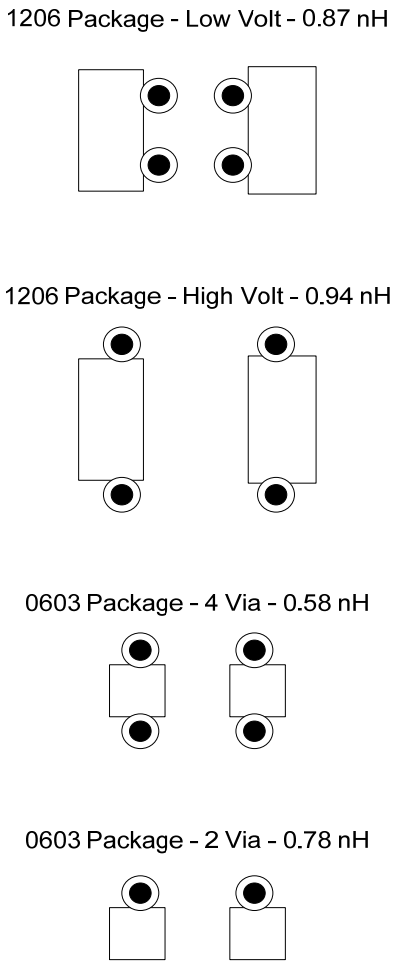


Figure 5. PEX 8112RDK-F Decoupling Capacitor Footprints

4.2.3 PCB Stackup

The PEX 8112RDK-F is a 6-layer, 62-mil thick PCB. The target signal impedance for all routing layers is 60 Ohms ±15% single-ended impedance and 100 Ohms ±5% differential. (Refer to Figure 6.)

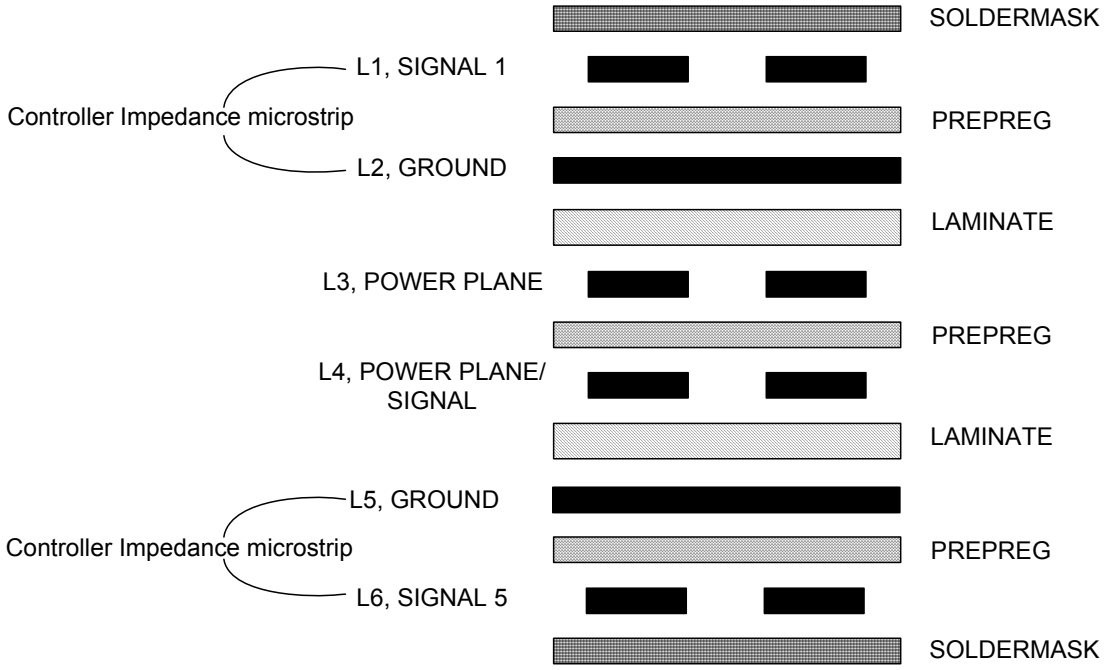


Figure 6. PEX 8112RDK-F Stackup

4.3 MidBus LAI Footprints

The PEX 8112RDK-F has one half-size MidBus LAI footprint sites (JP7), which can be used to probe the high-speed PCI Express serial lanes, or populated with a shroud that allows third-party PCI Express logic analyzers to view the serial data.

5. References

The following is a list of documentation to provide further details.

- PLX Technology, Inc.
  870 Maude Ave., Sunnyvale, CA 94085 USA
  Tel: 408 774-9060 or 800 759-3735, Fax: 408 774-2169, http://www.plxtech.com
  - *PEX 8112BB Data Book, Version 0.83 or higher*
  - *PEX 8112RDK-R Hardware Reference Manual*
- PCI Special Interest Group (PCI-SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 503 291-2569, Fax: 503 297-1090, http://www.pcisig.com
  - *PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a*
  - *PCI Express-to-PCI Bridge Specification 1.0*
  - *PCI Local Bus Specification, Revision 3.0*

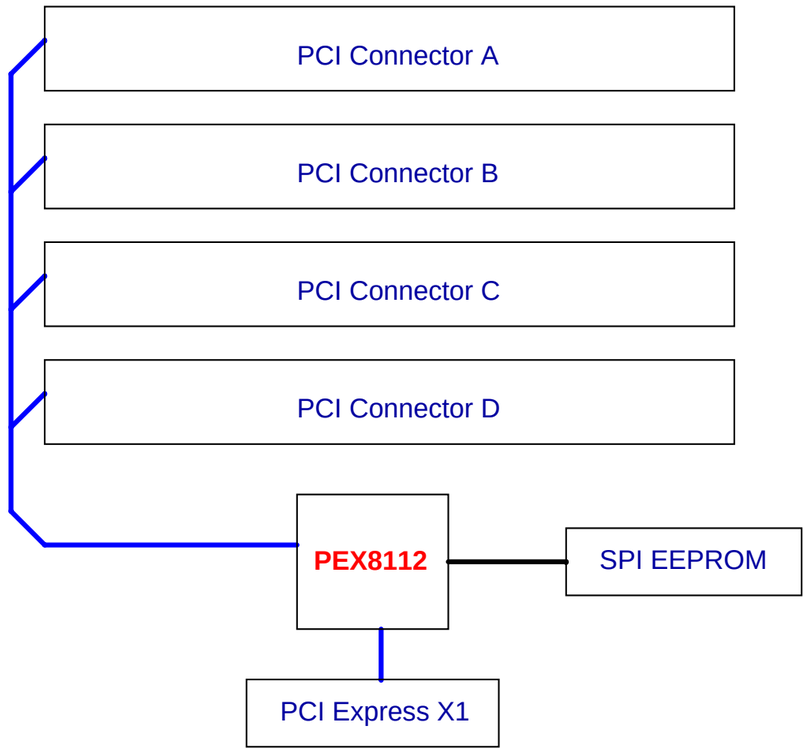
6. Bill of Materials and Schematics

The following pages contain the PEX 8112RDK-F bill of materials and schematics.

Item #	Qty	Man.	Man. Part number	Description	Package Type	Component Designator(s)
Surface Mount Components						
1	1	PLX Technology	PEX 8112-AA66BC	IC, 1-lane, 4-port, PCI Express bridge	SMT, 144-ball Standard BGA	U1
2	1	Cypress	CY2309SC-1	IC, Clock Buffer	SMT, 16-pin SOIC	U2
3	1	National	LP2992AIM5-1.5	IC, Regulator 1.5V	SMT, SOT235	U4
4	1	National	LM2937IMP-5.0	IC, Regulator 5V	SMT, SOT223	U5
5	1	TI	SN74LV08APWR	IC, Quad 2-IN AND GATE	SMT, 14-pin TSSOP	U7
6	1	National	LMS1587IS-3.3	IC, Regulator 3.3V	SMT, TO263	U8
7	1	TI	SN74AC74PWR	IC, Dual EDG-TRG D F-F	SMT, 14-pin TSSOP	U11
8	1	TI	SN74HC125DBR	IC, Quad BUS BUFF TRI-ST	SMT, 14-pin SSOP	U12
9	1	Raycon	RT-HD2-GT120ECN	PCI Connector, Dual Edge	SMD	J3
10	3	AMP/Tyco	145098-1	PCI Connector	SMD	J4, J5, J6
11	7	Chicago	CMD17-21VGC/TR8	LED, green	SMT, 0805	LEDV10, LEDP12, LED12, LEDP33, LEDE33, LEDP50, LED50
12	4	Chicago	CMD17-21VRC/TR8	LED, red	SMT, 0805	LED0, LED1, LED2, LED3
13	2	MuRata	LQH32CN470K53	Inductor, 47 µH, 10%	SMT, 1210	L1, L2
14	3	CTS	742C083272JTR	Resistor Network, 2.7K Ohms, 4R, isolated	SMT, 8-pin	RN3, RN4, RN5
15	1	CTS	742C083103J	Resistor Network, 10K Ohms, 4R, isolated	SMT, 8-pin	RN7
16	1	CTS	742C083512J	Resistor Network, 5.1K Ohms, 4R, isolated	SMT, 8-pin	RN10
17	1	CTS	742C083101JTR	Resistor Network, 100 Ohms, 4R, isolated	SMT, 8-pin	RN8
18	1	CTS	742C083271 JTR	Resistor Network, 270 Ohms, 4R, isolated	SMT, 8-pin	RN9
19	1	Panasonic	ERJ-6GEYJ512V	Resistor, 5.1K Ohms, 1/8W, 5%	SMT, 0805	R54
20	12	Panasonic	ERJ6GEYJ 272V	Resistor, 2.7K Ohms, 1/8W, 5%	SMT, 0805	R10, R17, R18, R19, R20, R21, R22, R23, R25, R26, R27, R55
21	2	Panasonic	ERJ-6GEYJ122V	Resistor, 1.2K Ohms, 1/8W, 5%	SMT, 0805	R43,R66,
22	3	Panasonic	ERJ-6GEYJ511V	Resistor, 510 Ohms, 1/8W, 5%	SMT, 0805	R44, R51, R52
23	2	Panasonic	ERJ-6GEYJ331V	Resistor, 330 Ohms, 1/8W, 5%	SMT, 0805	R41, R53,
24	4	Panasonic	ERJ6GEYJ 101V	Resistor, 100 Ohms, 1/8W, 5%	SMT, 0805	R13, R14, R15, R16
25	17	Panasonic	ERJ-6GEY0R00V	Resistor, Zero Ohms, 1/8W	SMT, 0805	R11, R12, R37, R45, R46, R47, R48, R49, R50, R58, R60, R62, R76, R78, R79, R82

Item #	Qty	Man.	Man. Part number	Description	Package Type	Component Designator(s)
26	1	Panasonic	ERJ6GEYJ105V	Resistor, 1M Ohms, 1/8W, 5%	SMT, 0805	R74
27	1	Panasonic	ERJ-6RSJR18V	Resistor, 0.18 Ohms, 1/8W, 5%	SMT, 0805	R2
28	15	Panasonic	ERJ6GEYJ103V	Resistor, 10K Ohms, 1/8W, 5%	SMT, 0805	R1, R3, R4, R7, R8, R9, R24, R34,R39, R67, R68, R71, R72, R73, R75
29	7	Panasonic	ERJ6GEYJ330V	Resistor, 33 Ohms, 1/8W, 5%	SMT, 0805	R28, R29, R30, R31, R32, R33, R38
30	4	IRC	LRC-LRF-1206-01 -R010-F	Resistor, current sense, 0.01 ohm 1/2W, 1%	SMT, 1206	R5,R35,R42,R64
31	27	Kemet	T494B226M0 16AS	Capacitor, 22 µF, tantalum, 16V	SMT, CASEB	CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14, CB15, CB17,CB18, CB19, CB20, CB21, CB22, CB23, CB24, CB25, CB26, CB27, C50
32	63	Panasonic	ECJ-GVB1C105K	Capacitor, Ceramic, 1.0 µF, 16V, 10%, X5R	SMT, 0805	CC1, CC2, CC3, CC4, CC5, C5, CC6, CC7, CC8, CC9, CC10, CC11, CC12, CC13, CC14, CC15, CC16, CC17, CC18, CC19, CC20, CC21, CC22, CC23, CC24, CC25, CC26, CC27, CC28, CC29, C33, CC35, CC36, CC37, CC38, CC39, CC40, CC41, CC42, CC43, CC44, CC45, CC46, CC47, CC48, CC49, CC50, CC51, CC52, CC53, CC54, CC55, CC56, CC57, CC58, CC59, CC60, CC61, CC62, CC63, CC64, CC65, CC66
33	13	Kemet	T491D476K016AS	Capacitor, 47 µF, tantalum, 20V, 10%	SMT, CASE D	CD2, CD3, CD4, C4, CD5, CD7, CD8, CD9, CD10, CD11, CD12, C15, C34
34	4	Kemet	T494B106K0 16AS	Capacitor, 10 µF, tantalum, 16V	SMT, CASE B	C32, C36, C37, C40
35	2	Panasonic	ECJ-0EB1A 104K	Capacitor, ceramic, 0.1 µF, 10V, 10%, X5R	SMT, 0402	C1, C2
36	27	Panasonic	ECJ-2VB1C 104K	Capacitor, ceramic, 0.1 µF, 16V, 10%, X7R	SMT, 0805	C3, C6, C7, C8, C9, C10, C11, C12, C13, C14, C16, C18, C20, C22, C24, C26, C28, C30, C35, C41, C42, C43, C49, C51, C52, C53, C54
37	8	Panasonic	ECJ-2VB1H 102K	Capacitor, ceramic, 0.001 µF, 50V, 10%, X7R	SMT, 0805	C17, C19, C21, C23, C25, C27, C29, C31
38	5	Panasonic	ECJ- 2VB1H 103K	Capacitor, ceramic, 0.01 µF, 50V, 10%, X7R	SMT, 0805	C38, C45, C46, C47,C48
39	2	AVX	TPSD476K025R0150	Capacitor, lo ESR tantalum, 47uF, 25V, 10%	SMT, Case D	CD1,CD6
40	2	Panasonic	ECS-T1EX475R	Capacitor, tantalum, 4.7uF, 25V, 20%	SMT, Case B	CB9, CB17
41	3	MuRata	GRM216R61E105KA1 2D	Capacitor, ceramic 1.0uF, 25V, 10%	SMT, 0805	CC32, CC33, CC34
42	3	Panasonic	ECJ-1VC1H220J	Capacitor, ceramic 22pF, 50V, 5%	SMT, 0603	C56, C57, C58

Item #	Qty	Man.	Man. Part number	Description	Package Type	Component Designator(s)
43	1	Panasonic	ECJ-1VC1H330J	Capacitor, ceramic, 33pF, 50V, 5%	SMR, 0603	C55
Through-Hole Components						
44	1	Mill-Max	110-93-308-41-001000	DIP socket	TH, 8-pin DIP	U3
45	1	Maxim	MAX765CPA	IC, INV -12V HI-EFF	TH, 8-pin DIP	U10
46	2	Omron	B3F-3152	Tact Switch	TH, 4-pin Rt Angle	S2, S3
47	8	AMP	640452-2	Header, 2 pin, single row, 0.1", unshrouded	TH, 2-pin	J2, JP9, JP10, JP11, JP12, JP13, JP17
48	8	AMP	640452-3	Header, 3 pin, single row, 0.1", unshrouded	TH, 3-pin	JP2, JP3, JP4, JP5, JP6, JP14, JP15, JP16
49	1	AMP	640452-4	Header, 4 pin, single row, 0.1", unshrouded	TH, 4-pin	J7
50	1	Molex	53109-0410	Power Connector	TH, 4-pin	JP1
51	1	Diodes	1N5817-T	Diode Schottky 20V 1A	TH, 2-pin	D12N
Manually Inserted Components						
52	1	Atmel	AT25640-10PC-2.7	SPI Serial EEPROM	DIP, 8-pin	U3
53	5	AMP/Tyco	382811-6	Shunt, 100mil pitch, 15u gold	2-pin	JP2(2-3),JP3(1-2), JP14(1-2), JP15(1-2), JP16(2-3)
Miscellaneous Components						
54	1	PLX Technology	PEX 8112 RDK-F	PCB, PEX 8111 RDK-F Bare Board Rev 4.0		
55	2	Building Fasterners	PMS 440 0025 PH	Screws, Philips, 4-40 3/16”		
56	1	Keystone	9203	PCI Bracket		
Parts that Should NOT Be Assembled						
57	0	Lattice	LC4032V-5T44C	IC, CPLD, 30 IOs, 5ns, 3.3V configurable for PCI signaling	SMT, 44 pin TQFP	U6
58	0	AMP/Tyco	2-767004-2	CONN., 38-pin Mictor connector, vertical	SMT, vertical	J9, J10
59	0			CONN, ½ size midbus connector	SMT	JP7
60	0	Panasonic	ERJ-6GEY0R00V	Resistor, zero ohm, 1/8W, 5%	SMT, 0805	R6, R36, R56, R57, R59, R61, R63, R65, R70, R77, R80, R81, R83
61	0	Panasonic	ECJ-GVB1C105K	Cap.ceramic, 1.0uF,16V 10%, X5R	SMT, 0805	CC30,CC31
62	0	Panasonic	ECJ-2VB1C104K	Cap. Ceramic, 0.1uF, 16V, 10%, X7R	SMT, 0805	C44,C59,C61
63	0	Panasonic	ECJ-2VB1H103K	Cap. Ceramic, 0.01uF, 50V 10%, X7R	SMT, 0805	C39,C60
64	0	AMP	103185-8	Header, 1x8 100mil	TH, 8-pin	JP8
65	0	AMP	103240-3	Header, 2x3 100mil	TH, 6-pin	JP18
Second Source Information						
52	1	Atmel	AT25640-10PU-2.7	SPI Serial EEPROM	DIP, 8-pin	U3
PLX Part # PEX 8112RDK-F						
Product Name: PEX 8112RDK-F						



ECN HISTORY

ECN NUMBER	DATE	NOTE
1.0	6/1/2007	Initial release

PEX8112RDK-Forward Bridge

PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title: PEX8112 RDK-F

Size	Document Number	Rev
B	91-0078-000-A	1.0

Date: Wednesday, April 11, 2007 Sheet 1 of 9

PEX8112 (PCI and PCI Express)

R77, R80 NOT INSTALL

R56 NOT INSTALL

JP8, C61, U6, C44,C39,C59,C60 and JP18 NOT INSTALL. JUMP WIRES TO 3-5 & 4-6 FOR INTERNAL PCI ARBITER

R81, R83 NOT INSTALL

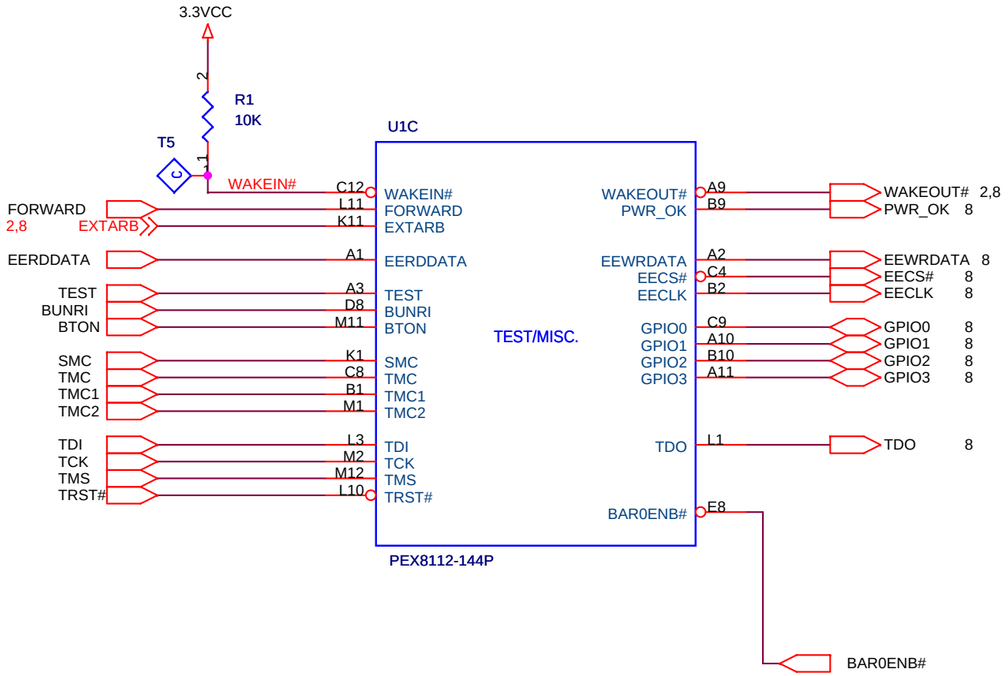
MATCH TRACES LENGTH ON PCI CLK

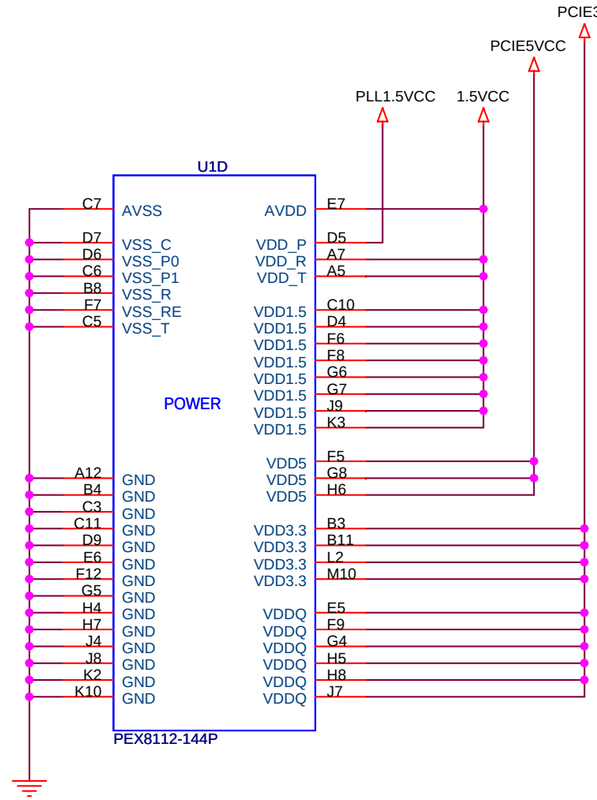
PLACE R33 CLOSE TO U1

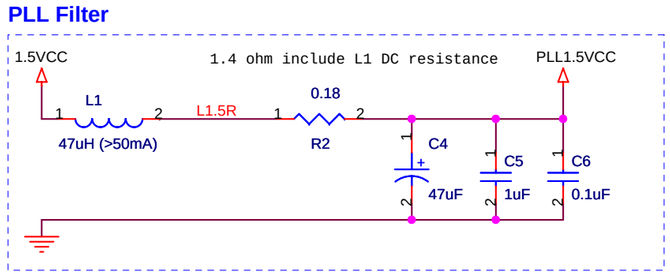
PLACE R28-R32 and R39 CLOSE TO U2

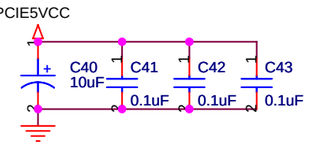
PLX TECHNOLOGY, INC.	
870 Maude Ave, Sunnyvale, CA 94085 www.plxtech.com	
Title	PEX8112 (PCI and PCI Express)
Size B	Document Number 91-0078-000-A
Rev	1.0
Date: Thursday, April 12, 2007	Sheet 2 of 9

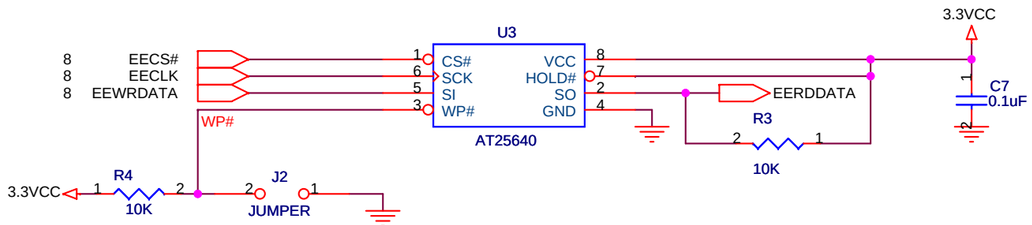
PEX8112 (Power and Misc.)

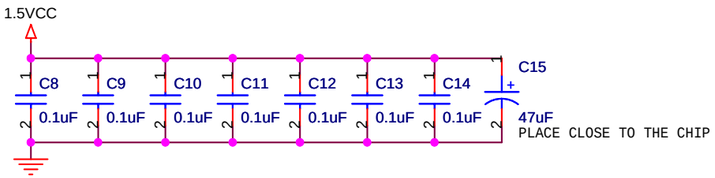


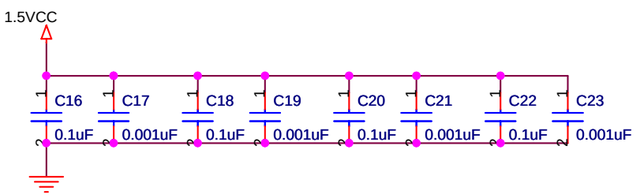


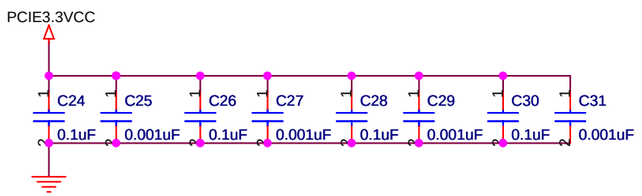






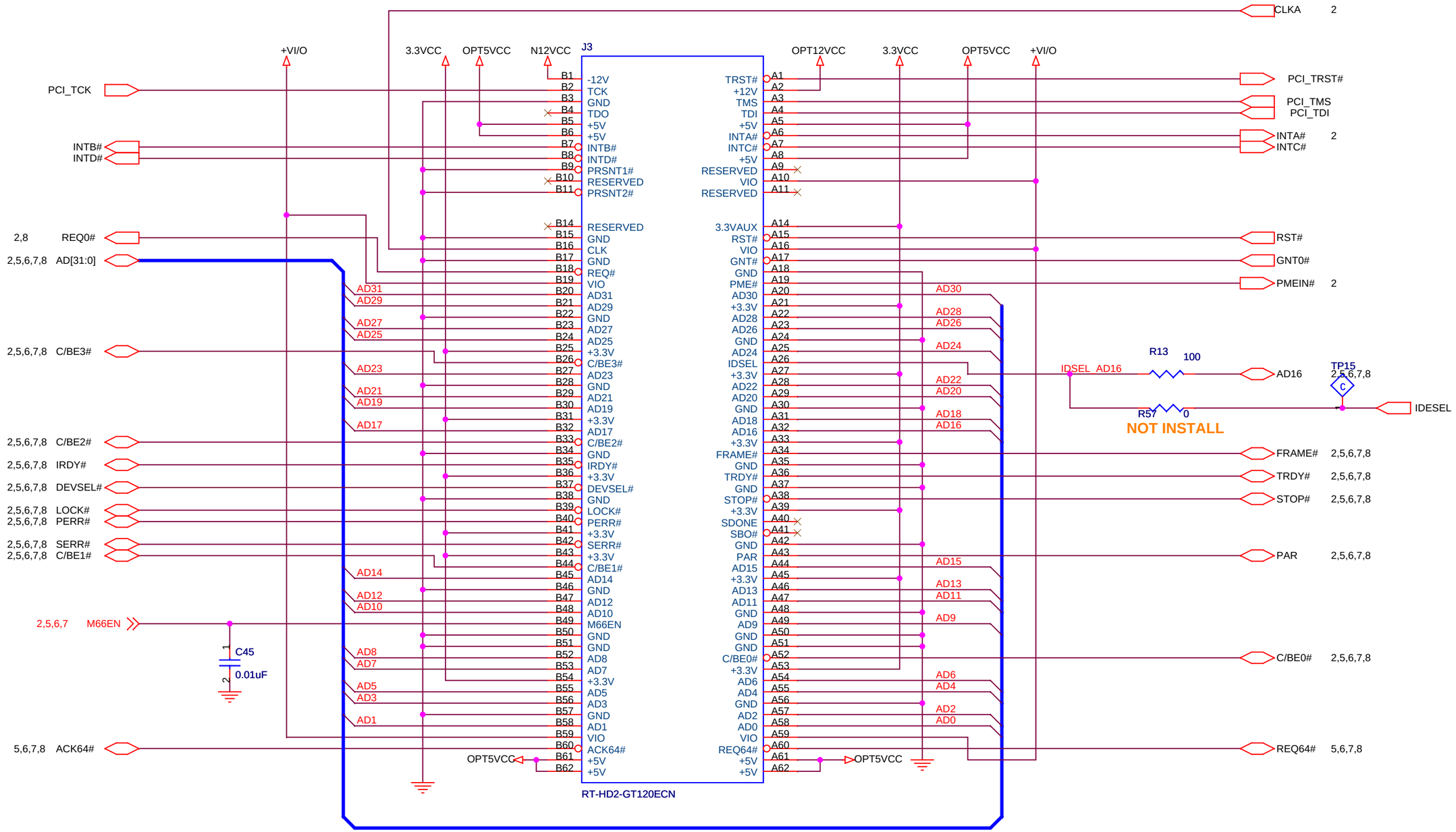






PLX TECHNOLOGY, INC.		
870 Maude Ave, Sunnyvale, CA 94085 www.plxtech.com		
Title: PEX8112 (POWER AND MISC.)		
Size: B	Document Number: 91-0078-000-A	Rev: 1.0
Date: Thursday, April 12, 2007	Sheet 3 of 9	

PCI Connector A

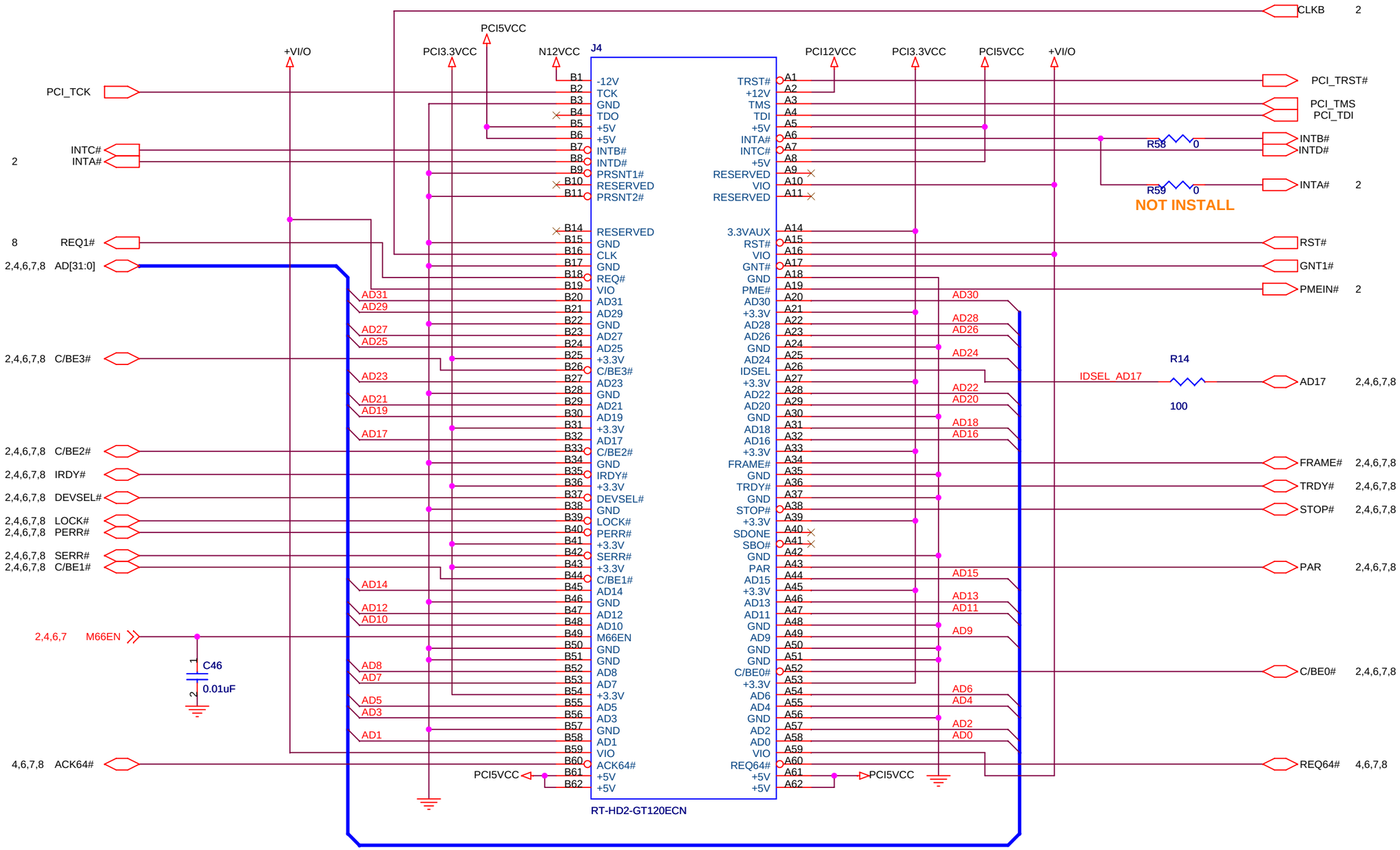


PLX TECHNOLOGY, INC.

870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

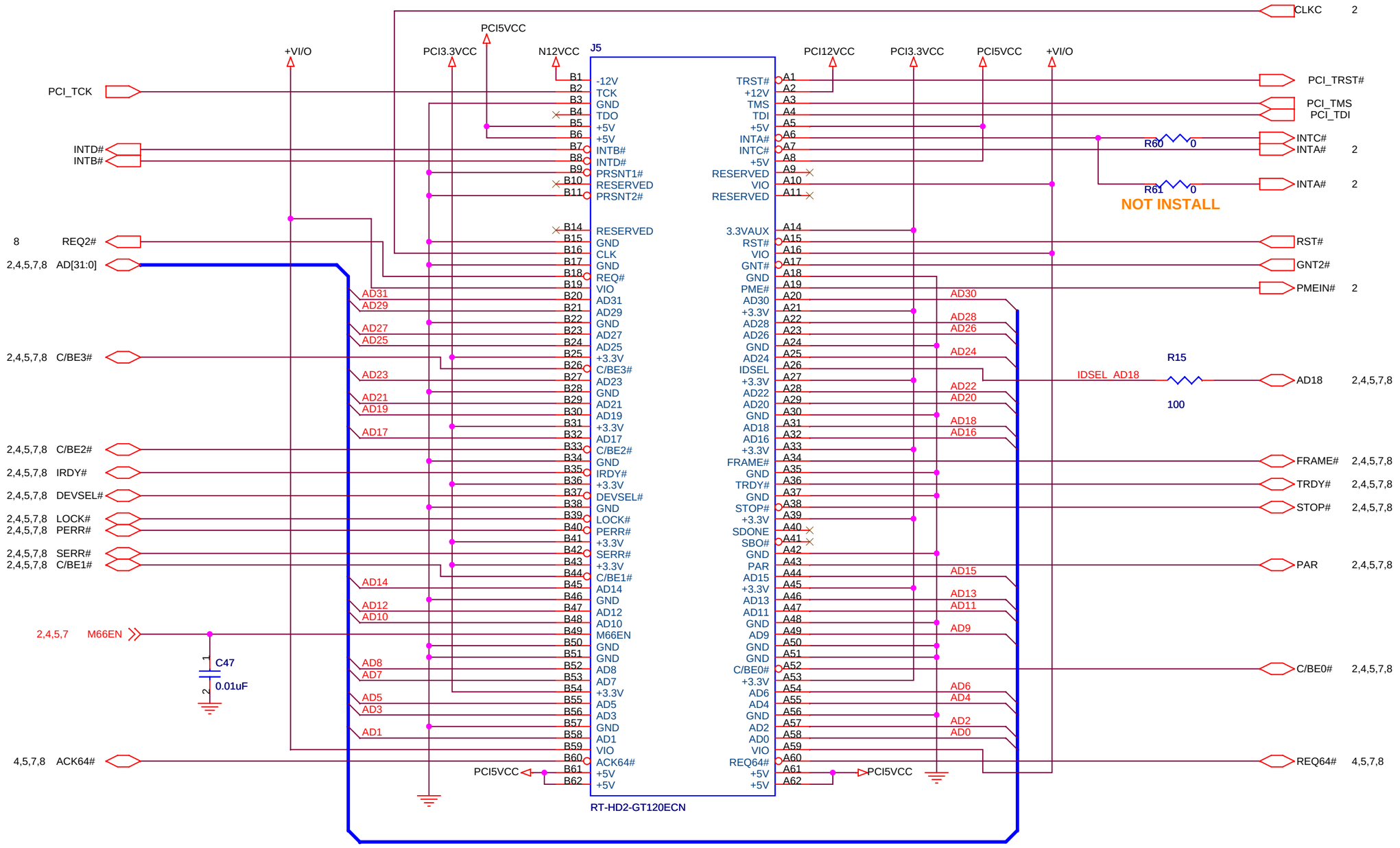
Title: PCI CONNECTOR A		
Size: B	Document Number: 91-0078-000-A	Rev: 1.0
Date: Friday, April 13, 2007	Sheet 4 of 9	

PCI Connector B



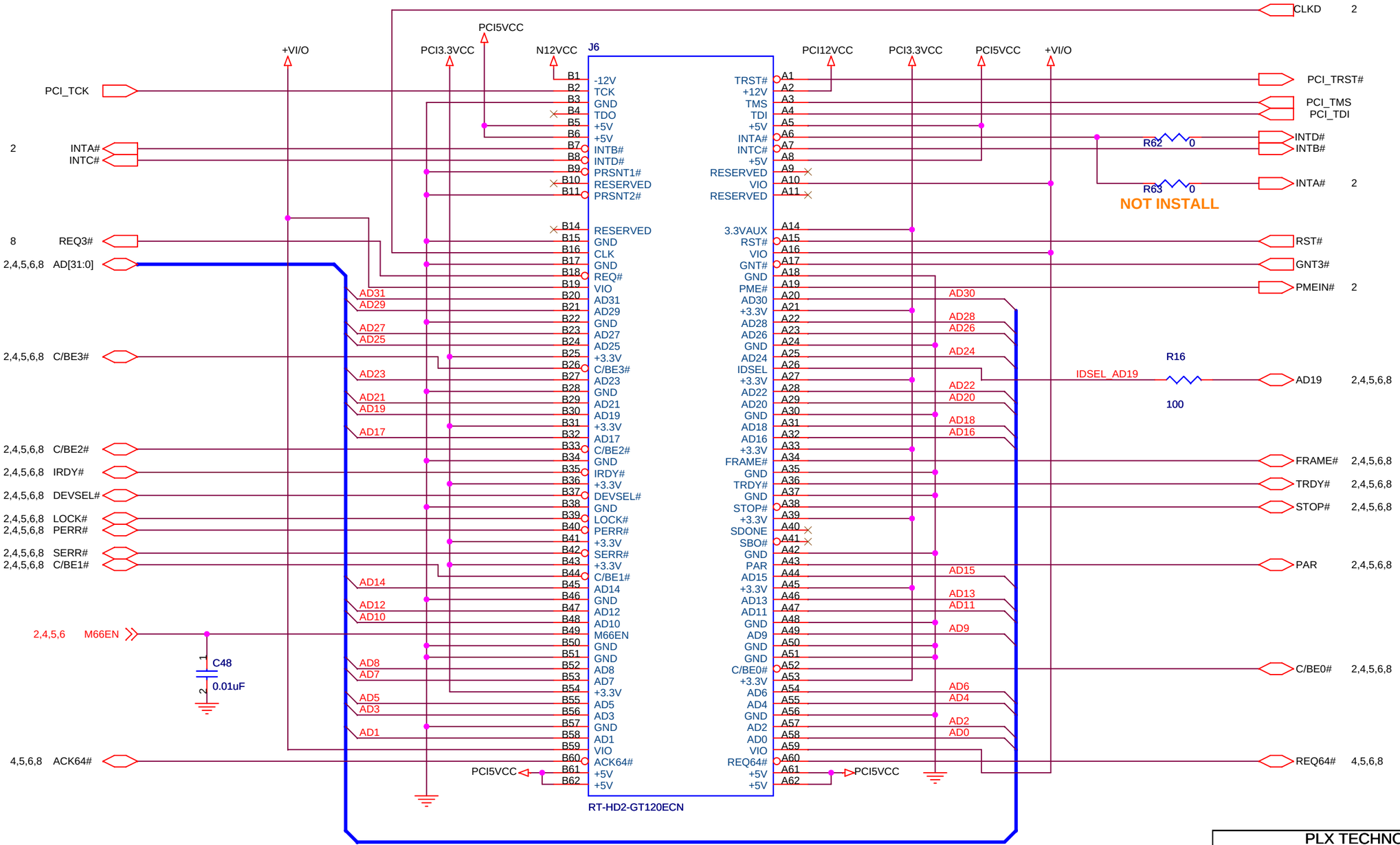
PLX TECHNOLOGY, INC.	
870 Maude Ave, Sunnyvale, CA 94085 www.plxtech.com	
Title	PCI CONNECTOR B
Size: B	Document Number: 91-0078-000-A
Rev: 1.0	
Date: Friday, April 13, 2007	Sheet 5 of 9

PCI Connector C

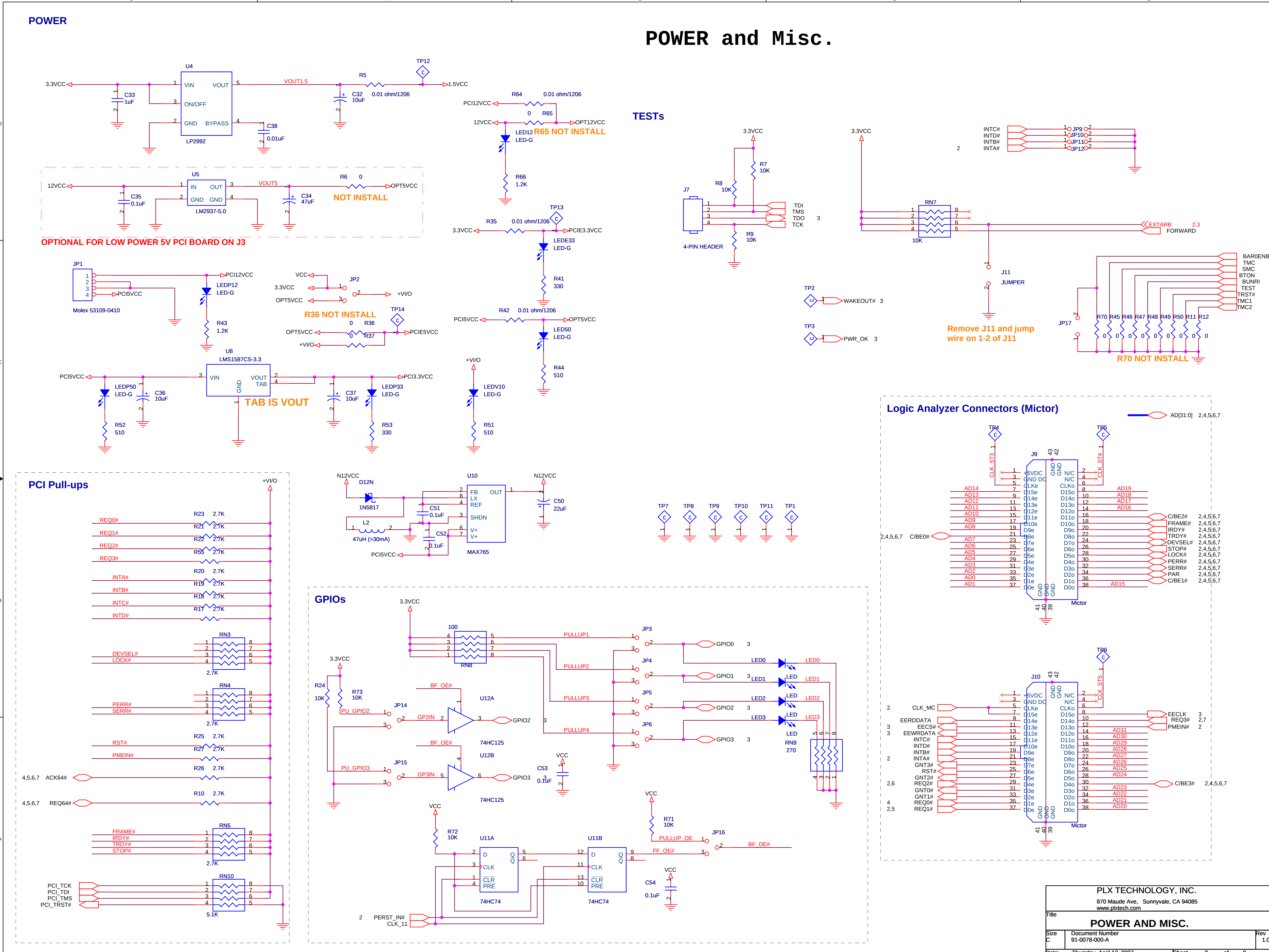


PLX TECHNOLOGY, INC.		
870 Maude Ave, Sunnyvale, CA 94085 www.plxtech.com		
Title: **PCI CONNECTOR C**		
Size: B	Document Number: 91-0078-000-A	Rev: 1.0
Date: Friday, April 13, 2007	Sheet 6 of 9	

PCI Connector D (5V Key)

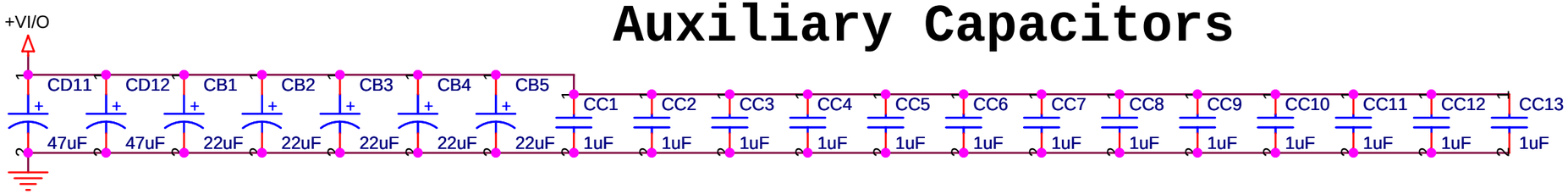


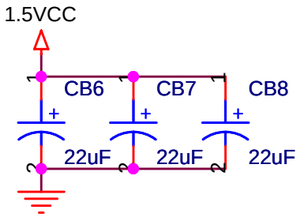
PLX TECHNOLOGY, INC.	
870 Maude Ave, Sunnyvale, CA 94085 www.plxtech.com	
Title: PCI CONNECTOR D	
Size: B	Document Number: 91-0078-000-A
Rev: 1.0	
Date: Friday, April 13, 2007	Sheet 7 of 9

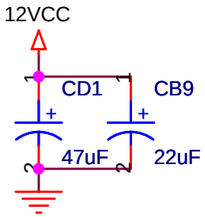


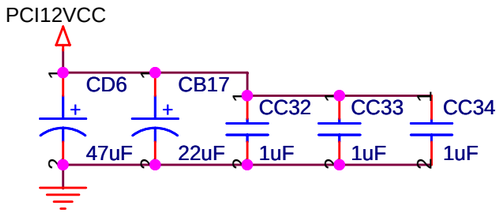
POWER
POWER and Misc.
U4
VIN
VOUT
ON/OFF
GND
BYPASS
LP2992
3.3VCC
C33 1uF
VOUT1.5
R5 0.01 ohm/1206
TP12
1.5VCC
C32 10uF
C38 0.01uF
PCI12VCC
R64 0.01 ohm/1206
12VCC
R65 0
OPT12VCC
LED12 LED-G
R65 NOT INSTALL
R66 1.2K
TESTs
U5
IN
OUT
GND
LM2937-5.0
C35 0.1uF
VOUT5
C34 47uF
R6 0
OPT5VCC
NOT INSTALL
OPTIONAL FOR LOW POWER 5V PCI BOARD ON J3
R35 0.01 ohm/1206
TP13
PCIE3.3VCC
LEDE33 LED-G
R41 330
J7
4-PIN HEADER
R7 10K
R8 10K
R9 10K
TDI
TMS
TDO
TCK
RN7 10K
EXTARB
FORWARD
J11 JUMPER
Remove J11 and jump wire on 1-2 of J11
INTC#
INTD#
INTB#
INTA#
JP9
JP10
JP11
JP12
JP1
Molex 53109-0410
PCI12VCC
PCI5VCC
LEDP12 LED-G
R43 1.2K
VCC
JP2
+VI/O
R36 NOT INSTALL
TP14
R36 0
R37 0
PCIE5VCC
R42 0.01 ohm/1206
LED50 LED-G
R44 510
TP2
WAKEOUT#
TP3
PWR_OK
BAR0ENB#
TMC
SMC
BTON
BUNRI
TEST
TRST#
TMC1
TMC2
JP17
R70 R45 R46 R47 R48 R49 R50 R11 R12
R70 NOT INSTALL
U8
LMS1587CS-3.3
VIN
VOUT
TAB
GND
TAB IS VOUT
LEDP50 LED-G
C36 10uF
R52 510
C37 10uF
LEDP33 LED-G
R53 330
PCI3.3VCC
LEDV10 LED-G
R51 510
Logic Analyzer Connectors (Mictor)
AD[31:0]
TP4
TP5
J9
Mictor
CLK_ST3
CLK_ST4
C/BE2#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
LOCK#
PERR#
SERR#
PAR
C/BE1#
C/BE0#
PCI Pull-ups
REQ0#
REQ1#
REQ2#
REQ3#
INTA#
INTB#
INTC#
INTD#
RN3
DEVSEL#
LOCK#
RN4
PERR#
SERR#
RST#
PMEIN#
ACK64#
REQ64#
RN5
FRAME#
IRDY#
TRDY#
STOP#
RN10 5.1K
PCI_TCK
PCI_TDI
PCI_TMS
PCI_TRST#
N12VCC
D12N 1N5817
L2 47uH (>30mA)
U10
FB
LX
REF
SHDN
V+
OUT
MAX765
C51 0.1uF
C52 0.1uF
C50 22uF
TP7 TP8 TP9 TP10 TP11 TP1
GPIOs
RN8 100
PULLUP1
PULLUP2
PULLUP3
PULLUP4
JP3
JP4
JP5
JP6
GPIO0
GPIO1
GPIO2
GPIO3
LED0
LED1
LED2
LED3
RN9 270
R24 10K
R73 10K
JP14
PU_GPIO2
BF_OE#
U12A
GP2IN
74HC125
JP15
PU_GPIO3
U12B
GP3IN
C53 0.1uF
R72 10K
U11A
74HC74
U11B
R71 10K
PULLUP_OE
JP16
FF_OE#
C54 0.1uF
PERST_IN#
CLK_11
J10
CLK_ST5
CLK_MC
EERDDATA
EECS#
EEWRDATA
EECLK
REQ3#
PMEIN#
C/BE3#
PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com
Title
POWER AND MISC.
Size C
Document Number 91-0078-000-A
Rev 1.0
Date: Thursday, April 12, 2007
Sheet 8 of 9

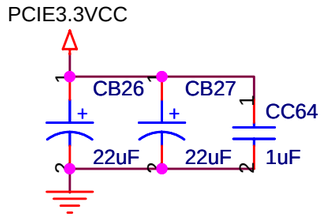
Auxiliary Capacitors

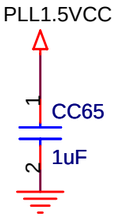


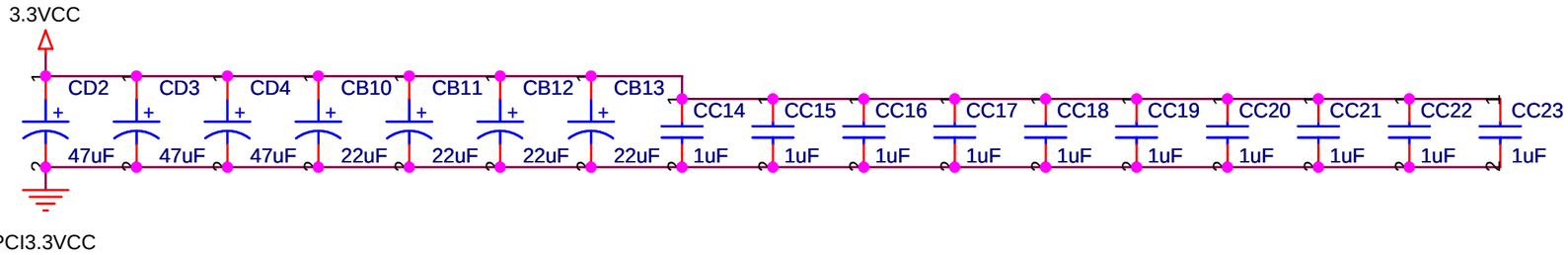


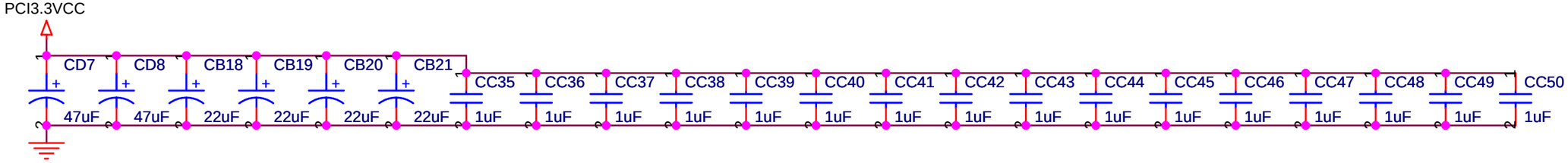


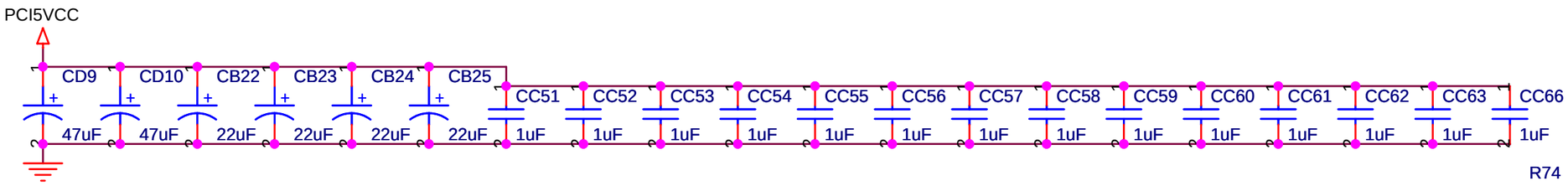


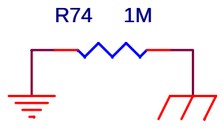


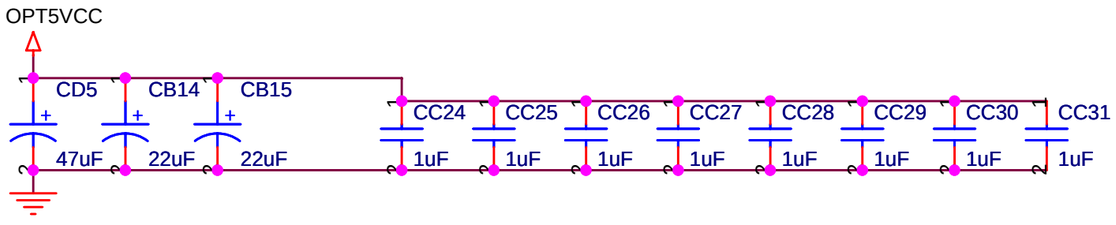












PLX TECHNOLOGY, INC.

870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title

AUXILIARY CAPACITORS

Size	Document Number	Rev
A	91-0078-000-A	1.0

Date: Wednesday, April 11, 2007 Sheet 9 of 9