PEX 8111BB ➔ PEX 8112AA
Conversion Documentation

The ExpressLane™ PEX 8112 and PEX 8111 are high performance bridges designed to the PCI Express-to-PCI Bridge Specification 1.0a, that enables designers to migrate legacy PCI bus interfaces to the new advanced serial PCI Express. These 2-port devices are equipped with a single lane PCI Express port and a parallel bus segment supporting the conventional PCI operation. The PEX 8112 and PEX 8111 are capable of operating in forward and reverse bridging modes. The PEX 8112 is fully compatible with the PEX 8111, allowing existing PEX 8111 customers to upgrade without making any hardware or software changes. The PEX 8112 is available in the Industrial Temperature range (-40 to +85 degC).

This document details changes that designers should be aware of as they convert PEX 8111BB silicon-based designs to use the latest generation PEX 8112AA. Technical assistance is available at the PLX Technical Support web page (www.plxtech.com/support/).

A. Silicon Documentation

Document	Version	Description	Publication Date
PEX 8111BB Data Book	1.2	Single Lane PCI Express-to-PCI Bridge	June, 2006
PEX 8112AA Data Book	1.0	Single Lane PCI Express-to-PCI Bridge	October, 2007

B. Conversion Documentation Revision History

Revision	Publication Date	Description
1.0	May 24, 2007	Baseline.
1.1	June 21, 2007	Added the GPIO description.
1.2	August 3, 2007	Updated Section 2: Errata Fixed in the PEX 8112.
1.3	November 13, 2007	PEX 8112 is now available in the Standard Pitch Leaded package.

C. Conversion Documentation Summary

#	Description
1	New Features of the PEX 8112
2	Errata Fixed in PEX 8112 Silicon
3	New PCLKO62SEL# ball in PEX 8112 Silicon
4	PEX 8112 Register Changes
5	PEX 8112 Package Information

1. New Features of the PEX 8112

- Industrial Temperature range -40 ºC to +85 ºC
- Capability to disable Power Management in Reverse Mode
- Permits Memory Reads to burst in Reverse Mode
- Strap option allows a 62.5MHz clock to be selected
- Prevents multi-master lockouts (Modified internal arbiter algorithm to address the bandwidth loss encountered when an even number of masters are used in hidden arbitration)
- Eliminates glitch sensitivity on the interrupt lines
- New JTAG, PCI, and PCIe revision IDs

2. Errata Fixed in PEX 8112 Silicon

The PEX 8112 fixes the following errata in the *PEX 8111BB Errata, Revision 1.8*

Refer to the Errata document for further details.

Errata

- Errata #1: Serial EEPROM Last Configuration Register Does Not Load
- Errata #3: Secondary 66MHz Capable Bit Default Value in Incorrect
- Errata #4: First Byte Enable Value Forwarded on the PCI Express Writes Greater than 1 DWord
- Errata #5: PCI-to-PCI Express Prefetchable Space Incorrectly Accepted
- Errata #6: Last Byte Enable Corruption on PCI Express-to-PCI Writes
- Errata #7: Link Up Fails when Link number Equals 00F7h (247d) in TS1
- Errata #8: External Reset for PCLKO Clock Generator Ensures Reliable PCLKO Output
- Errata #9: D3hot to D0 Reset
- Errata #10: L1 Exit Failure Causes System Hang on Transition to D3hot
- Errata #11: Unexpected PM_Active_State_NAK Message Incorrectly Handled
- Errata #12: PCI Bus Protocol Violation during PCI-to-PCI Express Burst Writes
- Errata #13: PCI-to-PCI Express MSI Problem
- Errata #14: Multi-Master PCI Read Arbitration
- Errata #15: Multi-Master PCI Write Arbitration
- Errata #16: Short PCI Interrupts
- Errata #18: PCI Express-to-PCI Read Performance
- Errata #19:Link Up Fails with Asynchronous Resets

3. New PCLKO62SEL# ball in PEX 8112 Silicon

The PEX 8112 has a PCI Clock Output 62.5 MHz Select ball, which is not present on the PEX 8111. When PCLKO62SEL# is pulled Low with M66EN High, the PCLKO clock is derived from an internal low-jitter PLL. PCLKO is 62.5 MHz, with a 50% Duty cycle. The jitter is caused by the circuit that divides 100 MHz by 2/3. It operates on both the rising and falling edges of the clock, so as the duty cycle deviates from 50%, the jitter increases.

PCLKO62SEL# is a 3.3V input ball that was previously a No Connect ball in the PEX 8111 silicon. The PEX 8112 has an internal 50K pull-up resistor on PCLKO62SEL#. Therefore, existing PEX 8111 designs which convert to PEX 8112 require no change in layout to continue using the 66MHz clock.

- For the Standard Pitch (144-Ball, 13 x 13mm^2) BGA package, ball C2 is now PCLKO62SEL# in the PEX 8112.
- For the Fine-Pitch (161-Ball, 10 x 10mm^2) BGA package, ball C3 is now PCLKO62SEL# in the PEX 8112.

4. PEX 8112 Register Changes

The following changes to the register configurations are required when migrating to the PEX 8112 from the PEX 8111.

1. The PCI Device ID default value, PCIDEVID register (offset 02h[15:0]), was changed from 8111h to 8112h. This reflects the new PEX 8112 part number.
2. The PCI Device Revision ID default value, PCIDEVREV register (offset 08h[7:0]), was changed from 21h to AAh. This corresponds to the AA revision of the PEX 8112.
3. The Chip Revision default value, CHIPREV register (offset 1040h[15:0]), was changed from 0202h to 0A0Ah. This corresponds to the AA revision of the PEX 8112.
4. The Delay Link Training default value, TLPCFG0 register (offset 1048h[18]), was changed from 0h to 1h. PEX 8112's link training, by default, is now delayed for 12 ms after PERST# is de-asserted. GPIO3 is no longer used to determine the value of Delay Link Training in the PEX 8112 and can only be cleared through EEPROM accesses. GPIO3 must be pulled high or low with a 10K resistor.
5. In Forward Mode, the Secondary 66-MHz Capable value, SECSTAT register (offset 1Eh[5]), was changed from 0h to 1h. This indicates that the PEX 8112's secondary bus is capable of operating at 66MHz.
6. In Reverse Mode, the PEX 8112 introduced two new bits in the PCICTL register (offset 100Ch). Short Discard Timer Timeout Select (PCICTL[30]) and PE2P Rdline Override, (PCICTL[31]). These bits are reserved in the PEX 8111. Their respective functions are detailed below:

- (PCICTL[30]) - Short Discard Timer Timeout Select (rw, Default = 0b)

  When clear (default), the length of time in which data is returned from the PCI Express device, in response to a PCI Read, are held before being discarded is specified by the Bridge Control register *Primary Discard Timer* bit (offset 3Eh [8])

as either 32,767 (2^{15}) or 1,024 (2^{10}) PCI Clock cycles. This function is consistent with the PEX 8111 devices.

When set, Read data returned for PCI reads are discarded after only 64 PCI clock cycles.

- (PCICTL[30]) - PCI Express-to-PCI Memory Read Line Override (rw, Default = 1b)

  A PCI Express-to-PCI Read request that is outside both Memory-Mapped I/O and Prefetchable space is forwarded upstream, to the PCI Bus:

  - Addresses below the 4-GB Address Boundary space usually result in PCI Memory Read commands
  - Addresses above the 4-GB Address Boundary space usually result in PCI Memory Read Line or Memory Read Multiple commands

  For certain applications, it might be necessary to issue PCI Memory Read Line or Memory Read Multiple commands for addresses below the 4-GB Address Boundary space. Although the address is below the 4-GB Address Boundary space, setting this bit enables these PCI Cache commands, as long as all other requirements are met. This bit is set by default.

7. In Reverse Mode, the Capabilities List access, PCISTAT register (offset 06h[4]), was changed from Read-Only (RO) to Read-Write (R/W) for Memory Mapped access and to Write-Only (WO) for EEPROM accesses. This allows Power Management Extended Capabilities to be disabled in Reverse Mode.
8. The JTAG Part Number changed from 81D2h to 81D3, and the JTAG version changed from 3 to 0.

5. PEX 8112 Package Information

The PEX 8112 is a pin for pin compatible drop in replacement for the PEX 8111 and is offered in the following two packages:

- Standard Pitch BGA package

Parameter	Specification
Package Type	Plastic Ball Grid Array (PBGA)
Number of Balls	144
Package Dimensions	13 x 13 mm^2 (approximately 1.83 mm high)
Ball matrix pattern	12 x 12 mm^2
Ball pitch	1.00 mm
Ball diameter	0.60 ± 0.15 mm
Ball Spacing	0.40 mm
Part number	PEX 8112-AA66BI (leaded version)
Part number	PEX 8112-AA66BI F (lead-free version)

- Fine-Pitch BGA package

Parameter	Specification
Package Type	Fine-Pitch Ball Grid Array (FBGA)
Number of Balls	161
Package Dimensions	10 x 10 mm^2 (approximately 1.43 mm high)
Ball matrix pattern	9 x 9 mm^2
Ball pitch	0.65 mm
Ball diameter	0.60 ± 0.15 mm
Ball Spacing	0.40 mm
Part Number	PEX 8112-AA66FBI F (lead-free version)

The PEX 8112 is not available in the fine pitch leaded package.