I²C Level Shifting and Voltage Management AN

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Version 1.0

PEX 8505/08/09/18/25/33/47/48
Application Note

Introduction

This application note, in addition to general use, is specifically applicable to PEX 8505, PEX 8508, PEX 8509, PEX 8518, PEX 8525, PEX 8533, PEX 8547 and PEX 8548 devices.

Problem Description

I^2C is a standardized, low pin count, parallel bus used to communicate between two silicon chips. Typical usage includes setup and control operation where by a device is configured and or interrogated outside of the main data path.

Often, several devices will be on the same I^2C chain. Because of the parallel connectivity, I^2C rules require that any un-powered device not load down the Address/Data or Clock lines. Additionally, the specification requires that devices connected to the bus be capable of operating with both +3.3V and +5V logic levels.

The enclosed note addresses a simple transistor means of ensuring the PLX family of switches is compliant to both possible conditions.

Making the PLX family of Switches Fully I^2C Voltage Level Compliant

Within the PEX 85XX family of switches that support I^2C, if the device is un-powered, it can load down the SDA and SCL lines of the I^2C. Normally this is not an issue because the I^2C bus is typically not exercised until all devices are powered. However a problem can occur if the user has an I^2C Hot-Plug application, or uses I^2C to initialize and control various system power supplies during system power-up.

There are several means to make the PEX 85XX family of switches compliant to the I^2C voltage specification in either of these events. Described below is a standard transistor level translation method to provide bi-directional operation and bus protection to the I^2C bus when low side power is not present or when +5V operation is required.

General Description of the PLX PEX 85XX I^2C Buffer

The basic structure of the PEX 85XX I^2C implementation is as shown in figure 1 below. The push-pull IO cell is configured for I^2C operation by physically disabling the upper FET and forcing the device to operate only as pull down. When no power is applied to the PLX device ($V_{DD}33$=0V), the primary and secondary ESD protection becomes the basic conduction path for any master exercising the I^2C bus. This conduction path loads down the bus.

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I²C Open Drain Buffer Schematic

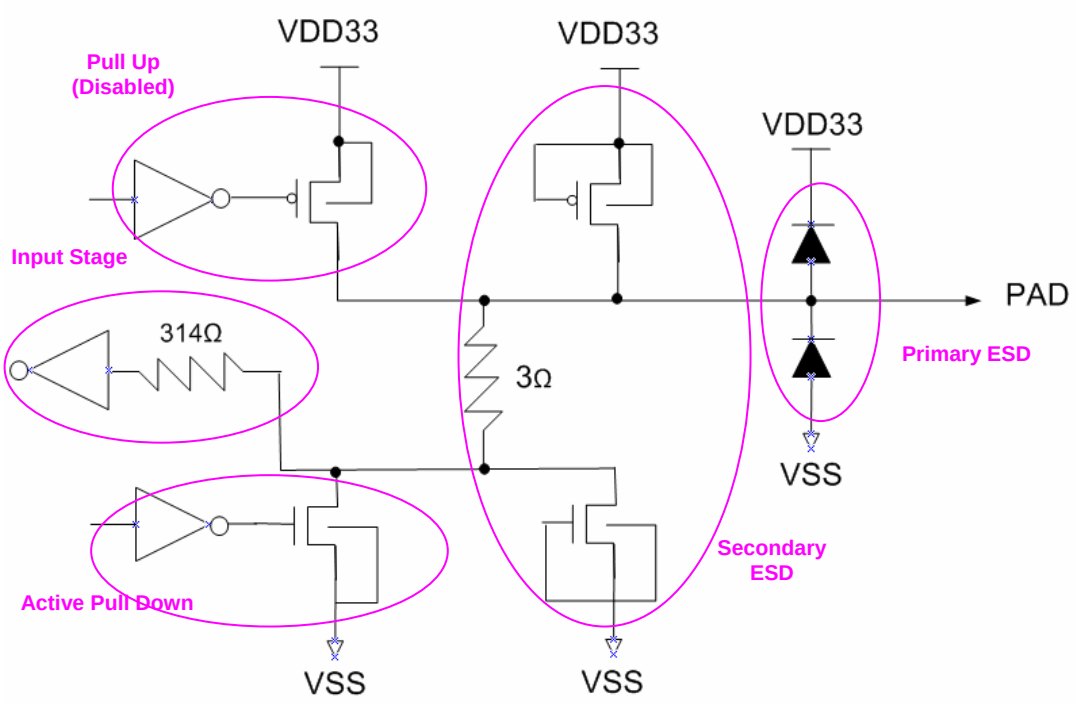

Figure 1. General Representation of PEX 85XX I²C Buffer Structure

Simple Transistor Method

This method uses a low V_{gs} transistor to isolate and/or shift the bus operating voltage. Circuit configuration requires the FET Source to be connected to the low-side bus and the FET Drain to be connected to the high-side bus. (See Figure 2) The FET gate is connected directly to the low-side power. Circuit operation is such that when the low side drives the bus to a logic low (active pull down), positive V_{gs} of the FET causes conduction, bringing the high-side bus lower also. To communicate a logic high, the low-side driver releases the line, causing V_{gs} → to zero and the FET to turn off.

To drive on the high-side bus, the high side master pulls the data bus low. This causes the FET bulk diode to conduct, resulting in a voltage drop along V_{source} of the FET. This in turn, re-establishes a positive V_{gs} of the device, further causing the FET to conduct and drive the low-side of the bus to a logic low.

When the PLX switch is powered off, V_{gs} is zero volts, and as such will isolate the powered portion of the bus from the unpowered PLX logic and prevent excessive bus loading. The circuit can be used for bi-directional data traffic, with the powered side (high-side) of the bus operating at +5V or +3.3V logic.

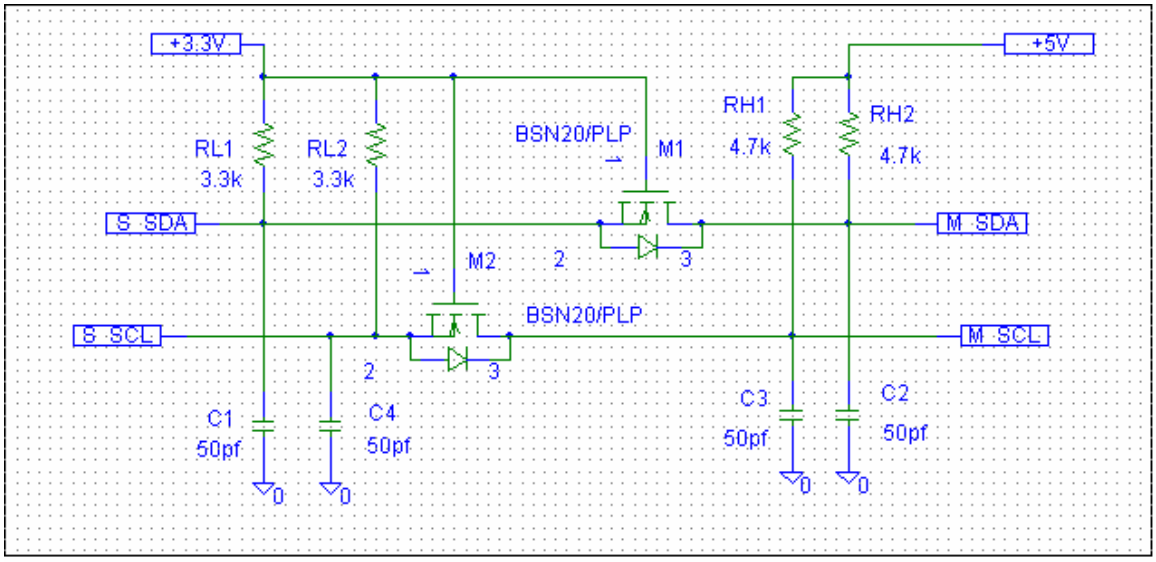

Figure 2. Simple Transistor Level Translation

The above circuit operates bi-directionally and will provide voltage translation and bus suppression. An ideal transistor to use is one with a low gate activation voltage. The Philips BSN20, N-Channel, enhancement mode MOS FET is an acceptable, low cost transistor for 3.3V operation. Transistors for even lower 'Low Side Bus' voltage operation might require a device such as the SuperTex TN2501. For the circuit to operate properly, the maximum V_{gs} threshold to activate the transistor must be minimally 1 Volt less than the low side bus voltage – hence for a 3.3V bus, V_{gs} < 2 Volts.

In this configuration, the PLX switch resides on the low side of the bus, receiving power from the +3.3V, with signal connections to the S_SDA and S_SCL bus lines. Rough cost estimates for the complete circuit (2 BSN20 FETs and two additional resistors) is ~ $0.25 in volume. Simulation examples are below.

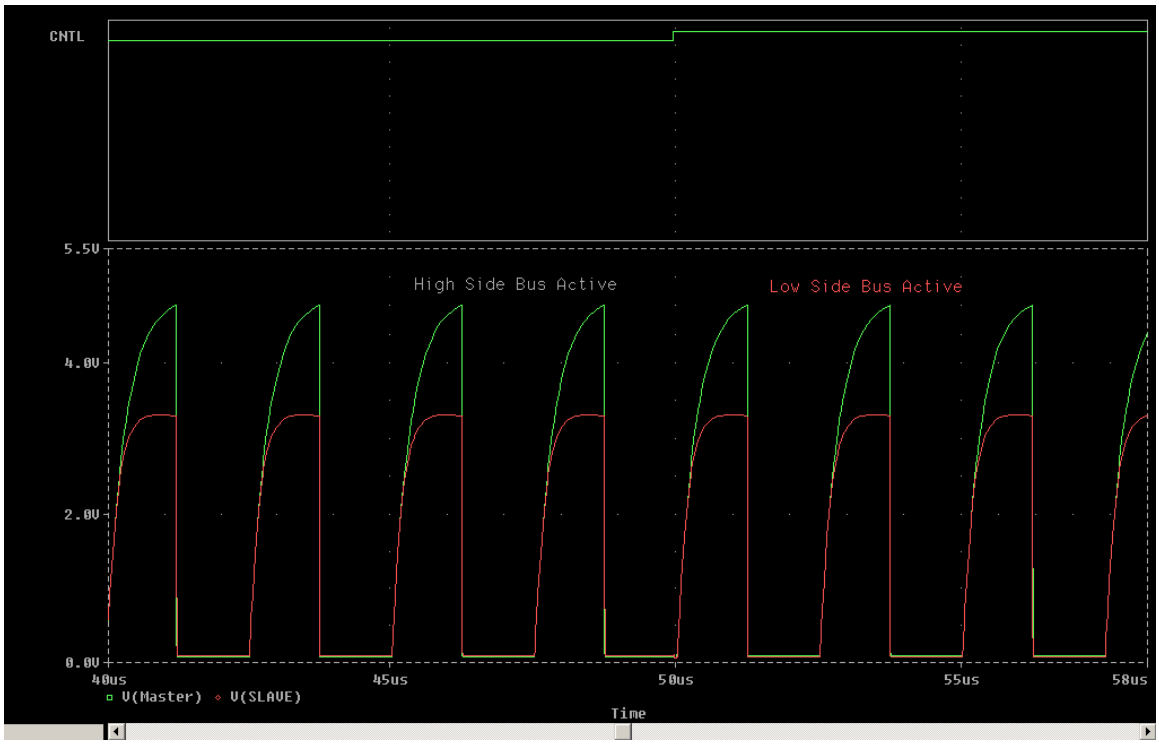

Figure 3. +5V High-side and +3.3V Low-side bus Active

A simulation CNTL signal was created to indicate when the bus is being driven by the slave or the master. With the CNTL signal low, the I^2C master (high-side) is exercising the bus. As can be seen with the change before and after the change in the CNTL signal, the bus is stimulated bi-directionally with appropriate signal levels for +5V high-side and +3.3V low-side operation on each side of the bus.

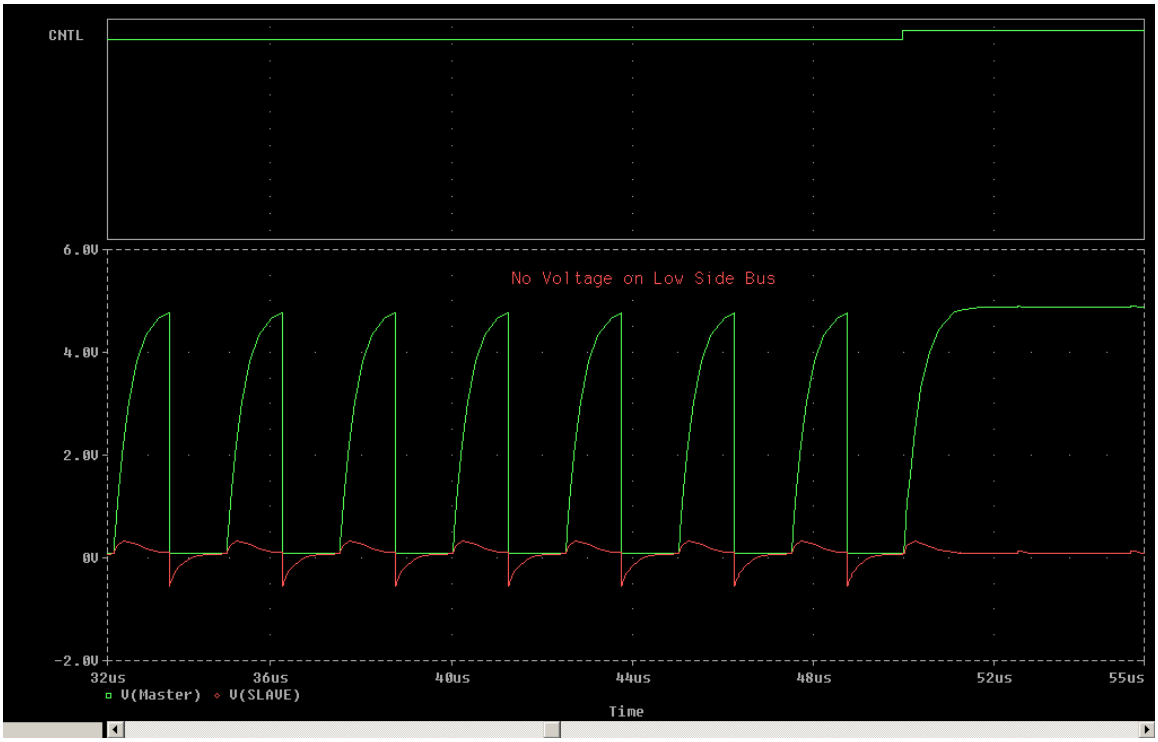

Figure 4. No power applied to Low Side Bus

With no 3.3V power applied, as can be seen above, the high-side bus continues to operate without loading.

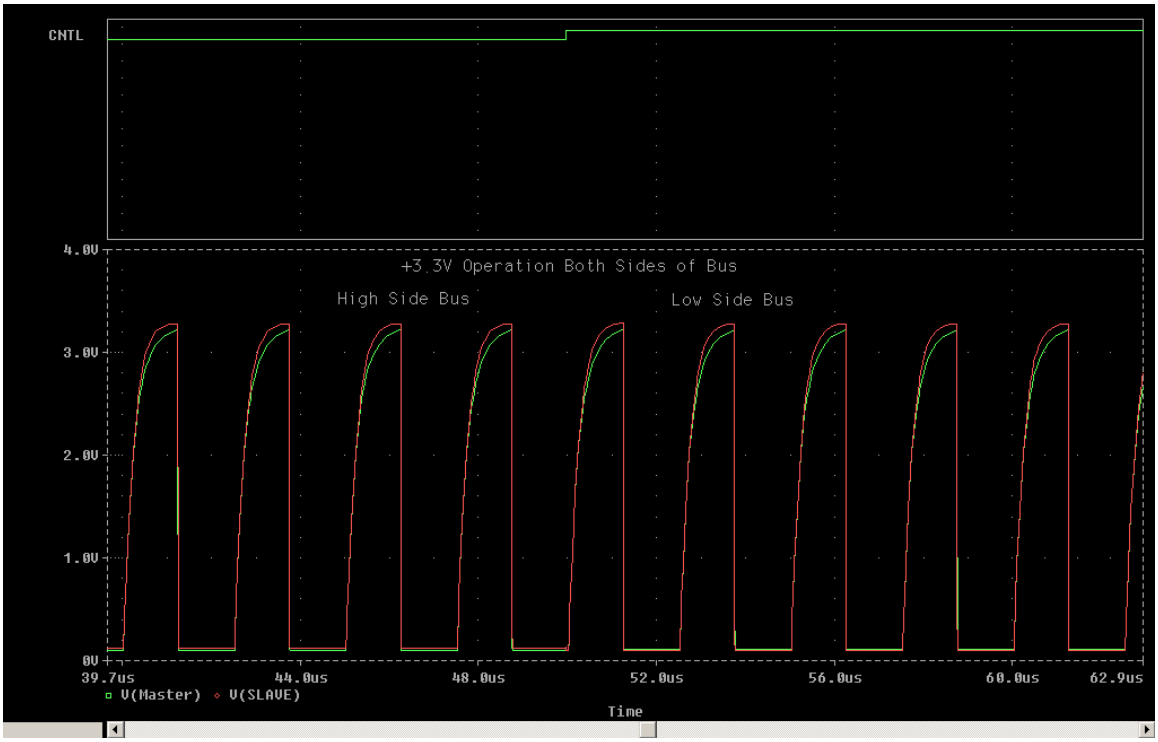

Figure 5. Random Data stream (+5V High-side, +3.3V Low-side)

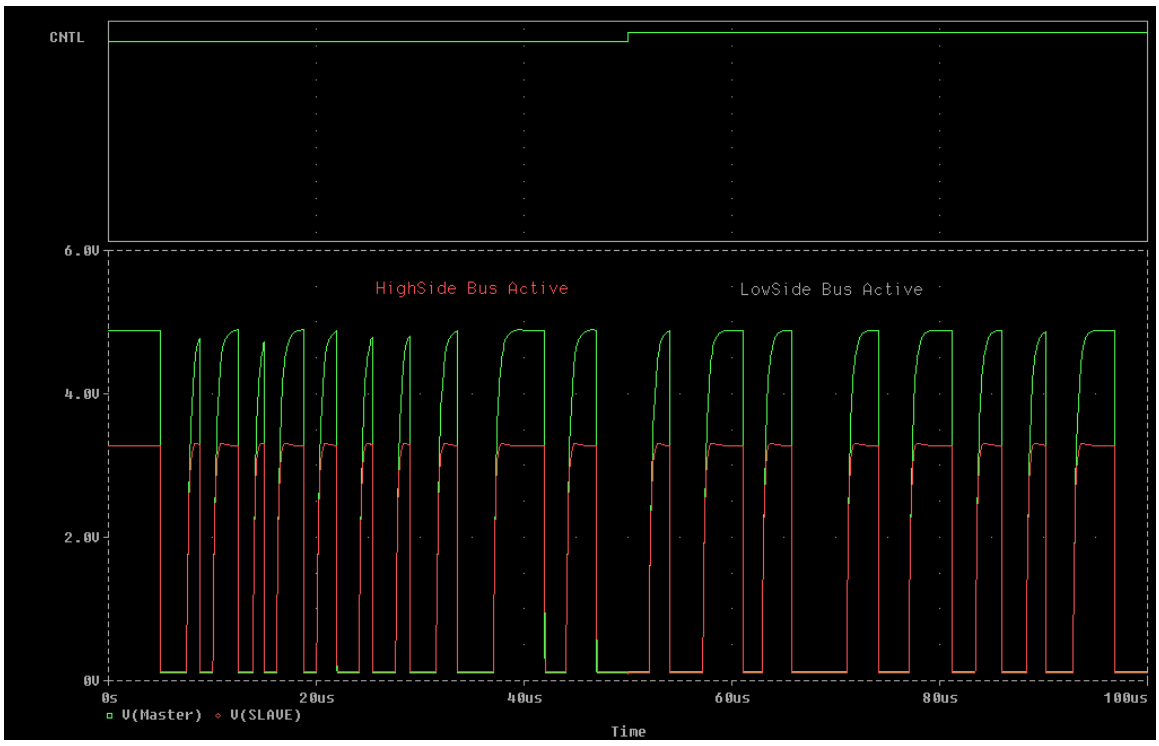

Figure 6. High-side and Low-side each operating at 3.3V

Full Translator Method

This approach implements full translators such as the MAX3737 from Maxim or PCA9509 by NXP. These devices provide level translation, power down isolation and the ability to actively isolate one side of the I^2C bus from the other.

Using a device such as the PCA9509, provides a flexible, robust means of managing the I^2C interface. Approximate solution costs are ~$0.90

Links to these devices can be found at the Maxim website (www.Maxim-ic.com) and NXP website (www.nxp.com).

References

- AN97055
  Philips Semiconductor
  www.philips.com

- MAX3733 Data Sheet
  Maxim Integrated Products
  www.Maxim-ic.com

- PCA9509 Data Sheet
  NXP Semiconductor
  www.nxp.com