PEX 8114BA PCI Express-to-PCI/PCI-X Bridge Errata Documentation

A. Affected Silicon Revision

This document details Errata for the following silicon:

Product	Revision	Description	Status
PEX 8114	BA	Four-Lane PCI Express-to-PCI/PCI-X Bridge	Production

B. Device Documentation Version

The following documentation is the baseline functional description of the silicon:

Document	Version	Description	Publication Date
PEX 8114BA Data Book	1.2	Data Book	March, 2007

C. Errata Documentation Revision History

Revision	Publication Date	Description
1.0	February 27, 2006	Baseline.
1.1	May 8, 2006	Changed erratum numbering scheme to improve usability. Transparent mode (Section E): ▪ Added errata E11 through E14 ▪ Moved erratum 7c to NT mode section, as new erratum F9 ▪ Clarified erratum E9, that in Reverse mode, it is only applicable to T mode (Forward mode is still applicable to T and NT modes) Non-Transparent mode (Section F) : ▪ Added erratum F9 (was erratum 7c in T mode section) ▪ Added errata F10 and F11 Added new Section G, "Cautions."
1.2	May 10, 2006	Clarified erratum F11, Solution/Workaround "d". Removed Note regarding fix in a future silicon revision.
1.3	May 23, 2006	Added erratum E15.
1.4	June 1, 2006	Added erratum E16.
1.5	June 14, 2006	Added NT Note to Section D, "Errata Summary." Clarified erratum E7.
1.6	June 27, 2006	Removed erratum E7, and combined its contents with erratum F9.
1.7	July 21, 2006	Added errata E17 through E20. Updated Data Book references to v1.0.
1.8	August 12, 2006	Added erratum G4.
1.9	October 5, 2006	Added erratum E21. Changed all instances of "15 DWords" to "1 DWord" in erratum E16.
1.91	October 16, 2006	Removed the word "memory" from the first sentence of erratum E12's Impact statement. Miscellaneous cosmetic changes.
2.0	February 21, 2007	Added errata E22 through E26. Updated Data Book references to v1.1. Miscellaneous cosmetic changes.
2.1	August 1, 2008	Added errata E227, E26, and E29. Corrected Caution G4. Updated Data Book references to v1.2.
2.2	March 18, 2011	Added Caution G5.

D. Errata Summary

Legend:

- F = Forward Bridge mode
- R = Reverse Bridge mode
- F/R = Forward or Reverse Bridge mode
- T = Transparent mode
- NT = Non-Transparent mode

Note: We do not recommend using the PEX 8114BA in NT mode due to the designated Non-Transparent errata listed below. There is no plan to fix the NT mode errata in future revisions of the PEX 8114.

#	Bus Mode	Bridge Mode	T/NT Mode	Description
Section E – Transparent Mode Only, or Transparent or Non-Transparent Mode				
E1	PCI/PCI-X	F	T/NT	PCI Express Lane Connection Restrictions
E2	PCI/PCI-X	F/R	T	16-Bit VGA Mode Does Not Decode Correctly
E3	PCI/PCI-X	F R	T/NT T	EP Bit Erroneously Set in Wrong TLP
E4	PCI/PCI-X	F R	T/NT T	Error Pollution – Malformed Packet with Received Target Abort
E5	PCI-X	R	T	Unsupported Request Error Status Bit Set on Configuration Writes with Data Parity Error
E6	PCI/PCI-X	F R	T/NT T	Parity Error Assertion Detected Is Erroneously Set
E7	–	–	–	***Removed, and combined with erratum F9.***
E8	PCI/PCI-X	F	T/NT	No Completion Supplied for Memory-Mapped Configuration Access to Register Offset C08h
E9	PCI-X	F R	T/NT T	In PCI-X Mode, Register Set Erroneously Indicates that PEX 8114 Is Medium Speed Device, Rather than Slow Speed Device
E10	PCI/PCI-X	F/R	T/NT	Data Bursts that Cross from 32- to 64-Bit Address Space Have Incorrect Address
E11	PCI/PCI-X	F	T/NT	Palette Snoop Bit Can Be Set in Forward Bridge Mode
E12	PCI-X	F	T/NT	Read Completion Delivery Is Gated by *Bus Master Enable* Bit

#	Bus Mode	Bridge Mode	T/NT Mode	Description
Section E – Transparent Mode Only, or Transparent or Non-Transparent Mode *(Cont.)*				
E13	PCI	F/R	T	PCI 64-Bit Data Corruption
E14	PCI/PCI-X	F/R	T/NT	Master Data Parity Error Bit Not Set if PERR# Occurs at End of Memory Write
E15	PCI	F	T/NT	PCI Express Completion Excluded Due to Pending PCI Interrupt Contending with Repetitive PCI Retries
E16	PCI-X	F/R	T/NT	PCI-X Immediate Read Completion Data Overflow
E17	PCI/PCI-X	F	T	PEX 8114 Completions with *Configuration Retry Status (CRS) Enable* Bit Set Can Result in Incorrect Byte Count, Incorrect Type Field, or Failure to Drop Late Completion
E18	PCI/PCI-X	F/R	T	Although Acknowledgement Is Received, PEX 8114 Incorrectly Re-transmits TLPs after Replay Timer Expires, and the Re-transmitted TLPs are Malformed
E19	PCI/PCI-X	F	T	PEX 8114 Configuration Completions Dropped if Type 1 Configuration Cycles are Inappropriately Targeted to Non-existent Extended CSR Locations on Downstream PCI Bus during High-Volume Traffic
E20	PCI/PCI-X	F R	NT T	Split Completion Error Incorrectly Caused by Transactions that Access Any of the Last 4 Bytes at Top of Base/Limit or BAR Register
E21	PCI/PCI-X	F	T/NT	ASPM Re-attempts to Enter L1 State without Waiting the Required 10 µs Delay
E22	PCI	F/R	T	Command Register *Memory Write and Invalidate* Bit Is Read-Writable, but Should Be Read-Only
E23	PCI	F/R	T/NT	PCI Bus Timing
E24	PCI/PCI-X	F/R	T	Silent Data Corruption Associated with Data Bursts that Cross 4-KB Address Boundary Spaces Starting from Specific Address
E25	PCI/PCI-X	F/R	T	Interoperability Alert – Configuration Status Register (CSR) Writes Will Be Unable to Update Only the Primary Bus Number or Only the Secondary Bus Number Register when Issuing a Configuration Write to the Bus Number Register (Offset 18h[7:0], [15:8])
E26	PCI	F	T	Requester ID in PME Message Is Cleared to 0
E27	PCI/PCI-X	F/R	T	PEX 8114 reverses its Lane Numbers if it receives Training Sets (TS) with Link Disable Bit set
E28	PCI/PCI-X	F/R	T	AC-JTAG Not Supported
E29	PCI/PCI-X	F	T	PCI/PCI-X bus REQ# not followed by FRAME# prevents PEX 8114 arbiter from servicing subsequent requests

#	Bus Mode	Bridge Mode	T/NT Mode	Description
Section F – Non-Transparent Mode Only				
F1	PCI-X	F	NT	Interrupts on PCI-X Interface Cannot Be Generated by Way of PCI Express Interface, through BAR 1 Using I/O Transactions in NT Mode
F2	PCI/PCI-X	F	NT	Loss of Link Does Not Cause PEX 8114 Reset in NT Mode
F3	PCI/PCI-X	F	NT	NT Mode I/O BAR Access to Internal Registers Fails If Bus Master Enable Bit Is Not Set
F4	PCI/PCI-X	F	NT	NT Mode ECRC Fails to Set Detected Parity Error Bit
F5	PCI-X	F	NT	NT Mode Split Completion Error Erroneously Caused by Transaction that Approaches Top of BAR or BAR Limit Register
F6	PCI	F	NT	Non-Transparent Conversion from 32-to-64-Bit Address Transactions Failure
F7	PCI-X	F	NT	Configuration Accesses from PCI-X-to-PCI Express Overwrite Values in PCI Express Captured Bus Number and Captured Device Number Registers
F8	PCI/PCI-X	F	NT	Serial EEPROM Fails to Load Advanced Error Reporting Capabilities and Control Register in NT Mode
F9	PCI/PCI-X	F	NT	Base and Limit Boundary Circuit Fails to Stop Bursts across Top of Memory Space
F10	PCI/PCI-X	F/R	NT	In Non-Transparent Mode, BAR 2 Setup Register Prefetchable Bit Is Used as Part of Base Address when Accessing from PCI Express Side of the Bridge
F11	PCI/PCI-X	F/R	NT	Interrupt Request (Doorbell) Registers Do Not Function Correctly in Non-Transparent Mode
Section G – Cautions				
G1	PCI/PCI-X	R	T	Reverse Bridge Mode PCI Express Non-Fatal Errors are Translated into PCI_SERR# on PCI Bus
G2	PCI/PCI-X	F/R	NT	Serial EEPROM Control Register Must Be in Benign State to Allow Access to Serial EEPROMs
G3	PCI	F/R	T/NT	Single Data Phase PCI Read Requests Generate TLPs with a Size Determined by Prefetch Count and Not Limited by Single Data Phase Size
G4	PCI	F	T/NT	Memory Read Line, Memory Read Multiple commands issued on PCI bus for PCI Express-to-PCI reads
G5	PCI	F	T/NT	PCI-X Interface May Respond With Retry Response to a Split Completion Request in a Specific Case

E. Transparent Mode Only, or Transparent or Non-Transparent Mode

This section discusses errata that are specific to **Transparent mode only, or both Transparent and Non-Transparent modes.** For Non-Transparent mode only, refer to the **Non-Transparent Mode Only** section.

E1. PCI Express Lane Connection Restrictions

Description

In PCI or PCI-X Forward Bridge Transparent or Non-Transparent mode, PEX 8114 does not support lane reversal.

For example, if the PEX 8114 is connected only on a one-lane device (*that is*, as an x1 device) then the PEX_PETn0 and PEX_PETp0 pair must be connected to the PEX_PERn0 and PEX_PERp0 pair of the upstream device. The PEX_PETn0 and PEX_PETp0 pair of the PEX 8114 cannot be connected to the PEX_PERn3 and PEX_PERp3 pair of the upstream device (presuming that the upstream device is also an x4 device). Similarly, if the PEX 8114 is connected as a two-lane device (*that is*, as an x2 device) then the PEX_PETn[1:0] and PEX_PETp[1:0] pair of the PEX 8114 must be connected to the corresponding PEX_PERn[1:0] and PEX_PERp[1:0] pair of the upstream device.

Solution/Workaround

If the upstream device supports Lane Reversal, that capability accommodates this defect, thus removing the connection restriction.

Impact

The lanes must be manually connected, starting with Lane 0. If no training sets are received on PEX 8114 preferred Lane 0 of the PCI Express port, the PEX 8114 always returns 0 in the *Link Number* field of the TS1 and TS2 training sets.

E2. 16-Bit VGA Mode Does Not Decode Correctly

Description

In PCI or PCI-X Forward or Reverse Bridge Transparent mode, the **Bridge Control** register *VGA 16-Bit Decode* bit (offset 3Ch[20]) does not function correctly. PCI Address bits [9:0] are correctly decoded; however, PCI Address bits [15:10] are not decoded, causing the PEX 8114 to ignore these Address lines.

Solution/Workaround

Use 10-bit VGA mode.

Impact

16-bit VGA addressing is inoperative.

E3. *EP* Bit Erroneously Set in Wrong TLP

Description

In PCI or PCI-X Forward Bridge Transparent or Non-Transparent mode, or Reverse Bridge Transparent mode, an *EP* bit (*Poison Data*, bit 6, byte 2, of the PCI Express Header) is set in a TLP with good data that precedes a TLP with a Data Parity error. The PEX 8114 must break the single PCI burst into two TLPs, if the following conditions exist:

- If the PEX 8114 is performing a PCI Burst transaction, with contiguous Byte Enables followed by discontiguous Byte Enables, and
- A Parity error is detected on the PCI DWord with discontiguous Byte Enables, and
- If the DWord with discontiguous Byte Enables and a Data Parity error is located on the upper 16 bits.

When the burst is broken into two TLPs, however, the PEX 8114 sets the *EP* bit in the TLP with good data, rather than the TLP with the Data Parity error.

Solution/Workaround

None.

Impact

A single PCI burst with discontiguous Byte Enables is correctly broken into two TLPs, if the DWord immediately preceding the discontiguous Byte Enables has a Data Parity error; however, the error is reported by setting the *EP* bit in the wrong TLP.

E4. Error Pollution – Malformed Packet with Received Target Abort

Description

In PCI or PCI-X Forward Bridge Transparent or Non-Transparent mode, or Reverse Bridge Transparent mode, when the PEX 8114 receives a malformed packet with Completer Abort completion status, it should only set the **Uncorrectable Error Status** register *Malformed TLP Status* bit (offset FB8h[18]=1). Instead, the PEX 8114 logs a malformed packet and sets the following register bit:

- **Forward Bridge mode** – **Status** register *Received Target Abort* bit (offset 04h[28]=1)
- **Reverse Bridge mode** – **Secondary Status** register *Received Target Abort* bit (offset 1Ch[28]=1)

Solution/Workaround

None.

Impact

After receiving a malformed packet, the PEX 8114 erroneously sets the *Received Target Abort* bit.

E5. *Unsupported Request Error Status Bit* Set on Configuration Writes with Data Parity Error

Description

In PCI-X Reverse Bridge Transparent mode, when a Non-Posted Type 0 PCI-X Configuration Write is sent to the PEX 8114 with a Data Parity error, the PEX 8114 correctly sets the following bits and sends a Fatal or Non-Fatal Error message:

- **Status** register *Detected Parity Error* bit (offset 04h[31]=1)
- **Secondary Uncorrectable Error Status** register *Uncorrectable Data Parity Error Detected* bit (offset FE0h[7]=1)

In addition to the above, the PEX 8114 erroneously sets the **Uncorrectable Error Status** register *Unsupported Request Error Status* bit (offset FB8h[20]=1) and sends a second Error message.

Solution/Workaround

None.

Impact

On Reverse mode Type 0 Configuration Write requests with Data Parity errors, the PEX 8114 erroneously sets the *Unsupported Request Error Status* bit and sends a second Error message.

E6. Parity Error Assertion Detected Is Erroneously Set

Description

In PCI or PCI-X Forward Bridge Transparent or Non-Transparent mode, or Reverse Bridge Transparent mode, there are three cases in which the **Advanced Error Reporting Secondary Uncorrectable Error Status** register *PERR# Assertion Detected* status bit is erroneously set (offset FE0h[11]=1).

Case 1

The *PERR# Assertion Detected* status bit should be set only when a device detects PERR# asserted by another device. In this case, however, the PEX 8114 is setting the bit when it is the device that asserted PERR#.

If the PEX 8114 performs a Memory Read transaction on the PCI-X Bus and detects a Data Parity error, the PEX 8114 asserts PERR#, if enabled (offset 3Ch[16]=1), and erroneously sets the *PERR# Assertion Detected* status bit. If Error Reporting is enabled (offset 70h[2, 1, and/or 0]=1), an erroneous Error message is sent. In Reverse Bridge mode, SERR# is erroneously asserted, if enabled (offset 3Ch[17]=1).

Case 2

The *PERR# Assertion Detected* status bit should be set only when a device detects PERR# asserted by another device. In this case, however, the PEX 8114 is setting the bit when it is the device that asserted PERR#.

If the PCI/PCI-X interface receives a Memory Write Request when a Data Parity error is detected and an I/O write is pending inside the PEX 8114, the PEX 8114 asserts PERR#, if enabled (offset 3Ch[16]=1). This results in two status bits being erroneously set:

- **Advanced Error Reporting Secondary Uncorrectable Error Status** register *PERR# Assertion Detected* status bit (offset FE0h[11]=1)
- **Forward Bridge mode** – **Secondary Status** register *Master Data Parity Error* status bit (offset 1Ch[24]=1)

  Reverse Bridge mode – **Status** register *Master Data Parity Error* status bit (offset 04h[24]=1)

If Error Reporting is enabled (offset 70h[2, 1, and/or 0]=1), an erroneous Error message is sent. In Reverse Bridge mode, SERR# is erroneously asserted, if enabled (offset 3Ch[17]=1).

Case 3

If a poisoned TLP (*Poison Data*, bit 6, byte 2 of the PCI Express Header is set) is received on the PCI Express link, the following correct behavior occurs:

- **Advanced Error Reporting Uncorrectable Error Status** register *Poisoned TLP Status* bit is set (offset FB8h[12]=1)
- If Error Reporting is enabled for *Poisoned TLP Status*, a Fatal or Non-Fatal Error message is sent to the Root Complex

In addition, the following erroneous behavior occurs:

- **Advanced Error Reporting Secondary Uncorrectable Error Status** register *PERR# Assertion Detected* status bit is set (offset FE0h[11]=1)
- If Error Reporting is enabled for *PERR# Assertion Detected* (offset 70h[2 or 1]=1), a second Fatal or Non-Fatal Error message is sent to the Root Complex

Solution/Workaround

It is not possible to cause the Error Reporting to function correctly; however, careful selection of enable bits can mask the incorrect functionality.

Impact

Cases 1 and 2

This is an Advanced Error Reporting failure. When software investigates the error status bits, erroneous information is found, as it is unable to determine the real cause of the error condition. If the header log is read, it indicates that the bridge was executing a Memory Read transaction or a Memory Write transaction was received when the *PERR# Assertion Detected* status bit was set. This indicates that the target of the Memory Read, or the originator of the Memory Write, asserted PERR# during the transaction, neither of which could ever occur.

Case 3

This is an Error Pollution failure. Two error status bits should not be set for one error condition. The poisoned TLP is the original error; therefore, the *Poisoned TLP Status* bit should be the only bit set. Software is unable to determine that the two status bits were set from the single poisoned TLP, and can therefore infer that two separate errors occurred.

E8. No Completion Supplied for Memory-Mapped Configuration Access to Register Offset C08h

Description

In PCI or PCI-X Forward Bridge Transparent or Non-Transparent mode, if a Configuration Read Register access is made from the PCI Express link to any ***reserved*** register (***reserved*** registers are registers that are not defined in the register set), a completion with an Unsupported Request should be returned. However, if the PEX 8114 receives a Memory-Mapped Configuration Read Access Request on the PCI Express link to offset C08h, no completion is supplied for this transaction. Offset C08h is a ***reserved*** register and there is no reason to access it; however, all register accesses should return completions to all Memory-Mapped Read accesses.

Solution/Workaround

None.

Impact

A PCI Express Completion time out occurs if offset C08h is accessed.

E9. In PCI-X Mode, Register Set Erroneously Indicates that PEX 8114 Is Medium Speed Device, Rather than Slow Speed Device

Description

In PCI-X Forward Bridge Transparent or Non-Transparent mode, or Reverse Bridge Transparent mode, the PEX 8114 erroneously indicates that it is a medium-speed, rather than a slow-speed, device, as follows:

- **Forward Bridge mode** – **Secondary Status** register *DEVSEL Timing* field (offset 1Ch[26:25]=01b)
- **Reverse Bridge mode** – **Status** register *DEVSEL Timing* field (offset 04h[26:25]=01b)

Solution/Workaround

None. These values are hardwired, and cannot be changed by serial EEPROM load.

Impact

In PCI-X Forward or Reverse Bridge Transparent and Non-Transparent mode, DEVSEL# timing is indicated as medium speed, when the PEX 8114 is actually a slow-speed device.

E10. Data Bursts that Cross from 32- to 64-Bit Address Space Have Incorrect Address

Description

In PCI or PCI-X Forward or Reverse Bridge Transparent or Non-Transparent mode, the PEX 8114 does not function correctly when a PCI-X transaction crosses the 4-GB boundary. When crossing the first 4-GB boundary, the transaction starts with a 32-bit address and crosses over to a 64-bit address. The 4-GB boundary is also a 4-KB boundary. The transaction should break into two TLP packets, one for each side of the 4-GB boundary. In addition, the first TLP should be a 3-DWord header and the second TLP should be a 4-DWord header. The PEX 8114 breaks up the transaction into 2 TLPs; however, it fails to update the TLP *Format* (*FMT*) field from a 3-DWord to a 4-DWord header. The result is the address is incorrect on the second TLP. Additionally, if the transaction starts on the lower side of the 4-GB boundary and crosses the 4-GB boundary and continues with a large amount of data, such that the result causes many Maximum Payload Size TLPs, each additional TLP will also have the wrong *FMT* setting. This causes address mismatches on a large amount of data. The erratum is no longer a problem after the transaction disconnects.

Solution/Workaround

Do not create PCI or PCI-X Write or Completion bursts that cross from 32-bit Address space to 64-bit Address space in a single PCI or PCI-X burst.

Impact

Data is written to or read from non-intended addresses.

E11. *Palette Snoop* Bit Can Be Set in Forward Bridge Mode

Description

When operating in Forward Bridge mode, the *Palette Snoop* bit is required by the *PCI Express to PCI/PCI-X Bridge Specification, r1.0,* to be Read-Only and set to 0. In PCI or PCI-X Forward Bridge mode, the PEX 8114's *Palette Snoop* bit can be written as 0 or 1. There are no other incorrect functional effects resulting from clearing or setting this bit.

Solution/Workaround

None.

Impact

When running in Forward Bridge mode, the **Command** register *Palette Snoop* bit (offset 04h[5]) is set.

E12. Read Completion Delivery Is Gated by *Bus Master Enable* Bit

Description

In PCI-X Forward mode, the delivery of PCI-X Read completions to the PCI Express link is incorrectly gated by the **Command/Status** register *Bus Master Enable* bit (offset 04h[2]).

Solution/Workaround

Set the **Command/Status** register *Bus Master Enable* bit (offset 04h[2]), while running in Forward Bridge PCI-X mode, to receive Memory Read completions from the PCI-X endpoint.

Impact

If the PCI Express Host sends a Read request downstream to a PCI-X endpoint through the PEX 8114, the completion generated by the PCI-X endpoint fails to be returned to the PCI Express Host if the PEX 8114 *Bus Master Enable* bit is not set. The completion should be returned, regardless of the *Bus Master Enable* bit state. The endpoint also experiences a Master Abort.

E13. PCI 64-Bit Data Corruption

Description

When operating in 64-Bit PCI Forward or Reverse Bridge Transparent mode, an overly long PCI Burst Write or Multiple Consecutive long PCI Burst Write can result in a malformed TLP. The malformed TLP is created when the internal memory becomes full, just as the Internal State machines are storing header information for the new TLP's creation. The additional header data being stored results in a malformed TLP. In default error handling situations, a PCI_SERR# signal is returned to the PCI Bus. This defect does not occur in PCI or PCI-X 32-Bit mode. The defect causes a single malformed TLP only on a very low statistical percentage of the times that the memory becomes full.

Solution/Workaround

a. Run in PCI-X mode or PCI 32-Bit mode, or ensure that the average bandwidth on the PCI Express link is greater than the bandwidth on the PCI link.

b. Alternatively, if the PCI data writing patterns can guarantee that the PCI endpoints connected to the PEX 8114 PCI side of the bridge do not write more that 2 KB of data in 16 consecutive Write or Read transactions, this defect does not occur. *For example*, if the endpoint can limit its PCI burst length to 64 bytes, this defect does not cause data errors.

c. The PEX 8114 Latency Timer can be programmed to cause the PEX 8114 to disconnect after 64 bytes of a Write transaction and a vacant PCI_REQ can be asserted if no other request is asserted. PCI_REQ then causes the overly long Write to disconnect.

Impact

Data corruption is signaled by a malformed TLP and PCI_SERR#.

E14. *Master Data Parity Error* Bit Not Set if PERR# Occurs at End of Memory Write

Description

In PCI or PCI-X Forward or Reverse Bridge mode, when the PEX 8114 masters a Memory Write transaction on the PCI-X Bus in response to a PCI Express transaction, the PEX 8114 does not set the **Secondary Status** register *Master Data Parity Error* bit (offset 1Eh[8]) for PERR# assertions that occur during the last two clocks after FRAME# de-asserts on the PCI Bus cycle. Because PERR# lags the data it corresponds to by two clocks, it is legal for PERR# to be asserted for the two cycles following FRAME# de-assertion on a Memory Write transaction. For PERR# assertions on Memory Write transactions within this small window (two clocks after FRAME# de-assertion), the *Master Data Parity Error* bit is not set.

Solution/Workaround

None.

Impact

The *Master Data Parity Error* bit is not set when Parity errors occur during the last two clocks of a Data burst.

E15. PCI Express Completion Excluded Due to Pending PCI Interrupt Contending with Repetitive PCI Retries

Description

In PCI Forward mode, the PEX8114 BA can go into a Live Lock condition in which high-frequency PCI Read request Retries can exclude the PEX 8114's receipt of the PCI Express completion that would fulfill the PCI Read request. To enter this Live Lock scenario, the PCI endpoint must Retry often enough that there are no more than two consecutive Clock cycles during which PCI_FRAME# is de-asserted and there must also be a pending PCI interrupt. This combination of pending PCI interrupt and high-frequency PCI Read requests cause the PEX 8114 to ignore the PCI Express Completion.

If the PCI_FRAME# signal is de-asserted for more that two Clock cycles, or if the PCI interrupt is de-asserted, this Live Lock condition does not occur. This defect does not affect PCI-X mode nor Reverse Bridge mode operations. It does not affect systems that do not Retry eternally with no more than two consecutive Clocks where PCI_FRAME# is de-asserted.

Solution/Workaround

Design your PCI endpoint such that it does not repeatedly Retry with only two Clock cycles between consecutive PCI_FRAME# assertions. This usually occurs because the PCI endpoint does not naturally Retry persistently. However, if your endpoint does persistently Retry with only the minimum PCI_FRAME# de-assertion time, then any other type of PCI Bus Master cycle, injected by either your endpoint or another endpoint, will throw the persistent PCI device off its Retry cadence and the transaction will go through.

Impact

If the PCI endpoint persistently Retries transactions with only two Clock cycles of PCI_FRAME# de-assertion between consecutive Retries, and if the endpoint also issues interrupts, the PEX 8114 could enter the Live Lock condition described in this erratum.

E16. PCI-X Immediate Read Completion Data Overflow

Description

In PCI-X mode, if the PEX 8114 issues a PCI-X Read request and receives an Immediate Completion larger than 1 DWord, the PEX 8114 can overflow its internal buffers and lose data. The problem is caused by the PEX 8114's failure to check the fullness of the internal memory after it starts accepting data during an Immediate Completion to a PCI-X Read request.

The PEX 8114 does, however, check the fullness of its internal memory before issuing a Read request, and if there is less than 1 DWord of Data space remaining, it does not issue the Read. Thus, the PEX 8114 can accept at least 1 DWord of data, and usually much more, if the buffers are not full.

Typically, PCI-X devices running in PCI-X mode respond only to Configuration cycles with Immediate Completions. In the case of Immediate Completions of Configuration cycles that are shorter than 1 DWord, there is no memory overflow.

Solution/Workaround

Use the more common Split Completion, or limit Immediate Completions to 1 DWord.

Impact

Silent data corruption if data overflow occurs.

E17. PEX 8114 Completions with *Configuration Retry Status (CRS) Enable* Bit Set Can Result in Incorrect Byte Count, Incorrect Type Field, or Failure to Drop Late Completion

Description

In PCI or PCI-X Forward Bridge Transparent mode, when the PEX 8114 *Configuration Retry Status (CRS) Enable* bit is set, the PEX 8114 incorrectly handles tardy Configuration Completions from the PCI/PCI-X side of the bridge, as follows:

1. PEX 8114 returns the completion with Configuration Retry Status (CRS), which:

   a. **PCI and PCI-X mode** – Has an incorrect Byte Count; additionally,

   b. **PCI mode only** – For the TLP intended to be a Completion with CRS, the TLP has incorrect values in its *Type* field; and

2. PEX 8114 fails to drop the late Completion if a Completion is eventually sent by the PCI-X side of the bridge to the PEX 8114 after the Completion with CRS is sent to the PCI Express Initiator.

For orientation and further details, refer to the *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*, Section 4.3.

This Completion with CRS is only supposed to be returned if the **Device Control** register *Bridge Configuration Retry Enable* bit (offset 70h[15]) in the PCI Express Capabilities List has been changed from its default state and is set. Thus, this defect is encountered only if the system software modifies the default state.

Workaround

Leave the **Device Control** register *Bridge Configuration Retry Enable* bit (offset 70h[15]) in the PCI Express Capabilities List in its default cleared state, so that the PEX 8114 does not return Completions with CRS with incorrect *Type* field to PCI Express Configuration requests. Or, the software must be prepared for a Completion with an incorrect Type and for Completions that should have been dropped.

Impact

Malformed completions can be transmitted if the *CRS Enable* bit is set.

E18. Although Acknowledgement Is Received, PEX 8114 Incorrectly Re-transmits TLPs after Replay Timer Expires, and the Re-transmitted TLPs are Malformed

Description

In PCI or PCI-X Forward or Reverse Bridge mode, this defect occurs when the PEX 8114BA transmits a TLP on the PCI Express link and the receiving PCI Express endpoint significantly delays returning a DLLP acknowledgement (ACK) that the packet was correctly received, until the last 2 clocks prior to the expiration of the PEX 8114's ACK Replay Timer.

Workaround

The endpoint receiving TLPs from the PEX 8114 should be configured, if possible, such that the ACK DLLP is transmitted as quickly as possible upon packet receipt. There are no CSRs that will extend the length of, or disable, the Replay buffer.

Impact

None. The system sees a duplicate TLP, which is silently dropped as a duplicate packet.

E19. PEX 8114 Configuration Completions Dropped if Type 1 Configuration Cycles are Inappropriately Targeted to Non-existent Extended CSR Locations on Downstream PCI Bus during High-Volume Traffic

Description

In PCI or PCI-X Forward Bridge Transparent mode, when the PCI Express Root Complex attempts to send a Configuration request through the PEX 8114 bridge to CSR locations above 255 on PCI-X devices downstream of the bridge which do not have extended CSR space above 255.

If the PCI Express endpoint is sending this type of anomalous Extended Configuration through the PEX 8114, the bridge should respond with an Unsupported Request (UR); however, if the Extended Configuration request from the PCI Express side of the bridge is issued during periods of heavy traffic from the PCI side of the bridge, the PEX 8114 can potentially lose the UR Completion, or create a malformed TLP that it is supposed to be returned to the PCI Express Initiator.

Single-threaded configurations do not exhibit this condition.

Workaround

Do not send Extended Address configurations across the bridge. Execute single-threaded configurations. Minimize configurations during heavy runtime traffic.

Impact

This defect can result in loss of a Completion, resulting in Completion timeout on the Requester.

E20. Split Completion Error Incorrectly Caused by Transactions that Access Any of the Last 4 Bytes at Top of Base/Limit or BAR Register

Description

In PCI or PCI-X Forward Bridge Non-Transparent mode or Reverse Bridge Transparent mode, when issuing a Burst transaction that accesses locations within the last 4 Dwords of the Memory space-defined by a Base/Limit or BAR register, a Split completion error is incorrectly generated. The error should not be generated, however, until the transaction crosses out of the top of the Base/Limit- or BAR-defined Address space.

Workaround

Ignore the Split Completion error or do not use the top 4 Dword locations of the Base/Limit.

Impact

In Transparent mode, a Split Completion error can be incorrectly caused by using the top 4 Dwords in a Base and Limit Address space. This can result in a Master Abort, and *Master Abort* Error bits being set in some systems. These bits might be set because the transaction with data is completed, and that transaction is then followed by the Split Completion Error message. If the PCI-X Host relinquishes the Tag when the data is returned, which is typical, then later when the Split Completion Error message is sent, it will be terminated with a Master Abort.

E21. ASPM Re-attempts to Enter L1 State without Waiting the Required 10 µs Delay

Description

In PCI or PCI-X Forward Bridge Transparent or Non-Transparent mode, there is a defect in the Active-State Power Management of the PEX 8114. When the PEX 8114 is operating in Forward Bridge mode as the downstream device on a link and attempts to enter the L1 power state while the upstream device refuses to allow the link to enter the L1 power state, the PEX 8114 should wait 10 µs before re-attempting to enter the L1 power state. However, the PEX 8114 re-attempts to enter the L1 power state in 7 µs, which violates the errata on the ASPM on the *PCI Express Base Specification, Revision 1.0a*.

Workaround

Using the serial EEPROM, set the **Link Capabilities** register *Active-State Power Management Support* field (offset 74h[11:10]) to 01b, to force support for only the L0s state. Also, set the **Link Control** register *Active-State Power Management Control* field (offset 78h[1:0]) to 01b, to enable the L0s state and disable the L1 state.

After changing these register field values, the PEX 8114 is forced to not support the L1 state based on the Power Management Capability, and thus it should never broadcast L1 ASPM support to the Root Complex, and therefore never enter into L1 ASPM.

Impact

If L1 ASPM diagnostics are enabled on the motherboard, the hardware chipset is capable of supporting L1 ASPM and can respond to any cycles from the Endpoint or the downstream side of the bridge. When L1 ASPM diagnostics are run, the PEX 8114 broadcasts that it is capable of L1 ASPM; however, it is unable to wait for the 10 µs required by the *PCI Express Base Specification, Revision 1.0a*. The Root Complex waits for 10 µs, as per the specification, and thus hangs the bus.

E22. Command Register *Memory Write and Invalidate* Bit Is Read-Writable, but Should Be Read-Only

Description

This defect applies only to PCI Forward or Reverse Transparent Bridge mode. The **Command** register *Memory Write and Invalidate* bit (offset 04h[4]), should be a Read-Only bit with a default value of 0. In the PEX 8114, Silicon Revisions AA and BA, this bit is incorrectly implemented as Read-Writable.

When the PCI Bus is in PCI mode, the *Memory Write and Invalidate* bit controls and indicates the bridge's ability to translate PCI Express Writes into PCI Memory Write and Invalidate transactions on the PCI Bus. The capability to translate PCI Express Memory Write commands to PCI Memory Write and Invalidate commands is optional. The PEX 8114 does not convert PCI Express Memory Write commands to Memory Write and Invalidate commands, and thus this bit should be Read-Only with a default value of 0.

Solution/Workaround

None.

Impact

The **Command** register *Memory Write and Invalidate* bit (offset 04h[4]), incorrectly implemented as Read-Writeable, erroneously communicates to software that the PEX 8114 can translate PCI Express Memory Write commands into PCI Memory Write and Invalidate commands.

E23. PCI Bus Timing

Description

In PCI Forward and Reverse, Transparent and Non-Transparent Bridge modes, the following PCI Bus timing errors exist in the PEX 8114BA; however, all timing is met at typical conditions:

a. In PCI mode at 66 MHz, the setup time on signals being driven into the PEX 8114's PCI inputs must be 1.5 ns greater than the 3 ns guaranteed by the *PCI Local Bus Specification, Revision 3.0*. The PEX 8114 requires 4.5 ns setup time on the PCI inputs in 66 MHz mode.

b. There are no timing violations in PCI mode at 33 MHz.

Note: *There are no timing violations in PCI-X operation.*

Solution/Workaround

Limit the loading on the bus. These timing violations do not inherently predict a system level bus timing deficiency; they may erode the margins provided for signal propagation on a maximally heavily loaded bus.

Impact

PCI timing problems can affect transaction signal integrity.

E24. Silent Data Corruption Associated with Data Bursts that Cross 4-KB Address Boundary Spaces Starting from Specific Address

Description

In PCI or PCI-X Forward or Reverse Transparent Bridge mode, the PEX 8114 experiences silent data corruption if two consecutive PCI or PCI-X Memory Write Burst (specifically, this includes a Memory Write, Memory Write Invalidate, or Memory Write block) transactions are issued such that the second of the two transactions burst data across the 4-KB Address Boundary space, with each of the two transactions ending and starting, respectively, at a specific critical address just prior to the 4-KB Address Boundary space. In general terms, this defect is caused by a problem in the circuitry that prepares the second PCI-X Write transaction to be broken at the 4-KB Address Boundary space into two PCI Express TLPs.

The following describes the critical transactions that occur when the Maximum Payload Size is 256 bytes:

a. The first of two consecutive PCI/PCI-X transactions must end on an address that is between 62 and 64 DWords prior to the next 4-KB Address Boundary space. The ending address values of these locations are XXX_XF08h to XXX_XF00h.

b. The second PCI/PCI-X transaction must start at location XXX_XF78h (which is 34 DWords prior to the 4-KB Address Boundary space) and must burst through the 4-KB Address Boundary space. This requires the PCI-X Master to be able to source a Continuous PCI-X burst of data that has a length of more that 2 ADQs (256 bytes).

c. There must be no other transactions of any kind between the first and second transaction.

The following describes the critical transactions that occur when the Maximum Payload Size is 128 bytes:

a. The first of two consecutive PCI/PCI-X transactions must end on an address that is between 30 and 34 DWords prior to the next 4-KB Address Boundary space. The ending address values of these locations are XXX_XF78h to XXX_XF80h.

b. The second PCI/PCI-X transaction must start at location XXX_XFB8h (which is 18 DWords prior to the 4-KB Address Boundary space) and must burst through the 4-KB Address Boundary space. This requires the PCI-X Master to be able to source a Continuous PCI-X burst of data that has a length of more that 1 ADQ (128 bytes).

c. There must be no other transactions of any kind between the first and second transaction.

Impact

In devices that source long Continuous PCI-X Data bursts across a 4-KB Address Boundary space, this defect can occur if the sequence described above is executed. Data is corrupted, starting at the 4-KB Address Boundary space and continues until the end of the burst that crossed the 4-KB Address Boundary space. The characteristics of the data corruption are that the QWord that should have been sent to the 4-KB Address Boundary space location is lost and the data sent to the address 4 KB + *n* is the data that should have been sent to address 4 KB + *n* + 1, where *n* = 0 through 1 minus the last intended location to be written. The last intended location is not written to and retains its original data. All data written to address prior to the 4-KB Address Boundary space is correct.

Workarounds

Use one of the following workarounds:

a. Do not execute PCI Burst Write transactions across 4-KB Address Boundary spaces.

b. Limit the size of Continuous bursts to 2 ADQs in 256 Maximum Payload Size mode (1 ADQ in 128 Maximum Payload Size mode) when bursting through 4-KB Address Boundary spaces. This can be done by disconnecting the:

   - PCI Write burst at least every other Allowable Disconnect Boundary boundaries when running with a 256-byte Maximum Packet Size

   - PCI Write burst at least every Allowable Disconnect Boundary boundaries when running with 128-byte Maximum Packet Size

   Many PCI or PCI-X Cycle Controllers or DMA Controllers that feed the PCI-X Bus have a burst size limit of 128 or 256 bytes, due to internal DMA FIFO size limitations. Other PCI or PCI-X Cycle Controllers or DMA Controllers often have Configuration Space register controls in the endpoint or DMA Controller that limit the burst size. When considering the impact of this erratum, take these endpoint limitations into account, as they may preclude this defect being hit.

c. Ensure that the two sequential Write transactions just prior to the 4-KB Address Boundary spaces access contiguous addresses.

   For example, assume that PCI-X Write transaction *n* is *m* bytes long and starts at address *x*. Transaction *n* + 1 would be accessing contiguous addresses if *n* + 1 begins at byte location *x* +*m* + 1). If they are naturally contiguous in the DMA Controller's transfer algorithm, the required gap between the first transaction's ending address and the second transaction's beginning address [as described in steps a and b (256-byte Maximum Payload Size) or steps a and b (128-byte Maximum Payload Size) of the Description above] will never occur and the defect and its associated Data errors will not be triggered.

E25. Interoperability Alert – Configuration Status Register (CSR) Writes Will Be Unable to Update Only the Primary Bus Number or Only the Secondary Bus Number Register when Issuing a Configuration Write to the Bus Number Register (Offset 18h[7:0], [15:8])

Description

In PCI-X Forward or Reverse Transparent Bridge mode, the PEX 8114 has an externally visible copy, as well as an internal shadow copy, of the **Bus Number** register (offset 18h).

A Write to the **Bus Number** register *Primary Bus Number* and *Secondary Bus Number* registers (offset 18h[7:0, 15:8], respectively), should update both the externally visible copy, as well as the internal shadow copy, of the **Bus Number** register. However, the internal shadow copy of the **Bus Number** register becomes corrupted, because Byte Enables are ignored during the Write, causing incorrect values to be written in the internal shadow copy. To correctly update both the externally visible and internal shadow copies of the **Bus Number** register, the Primary Bus Number and Secondary Bus Number must be written concurrently.

Reads initiated on the PCI Express/PCI-X interface to the **Bus Number** register correctly reflect the Primary Bus Number and Secondary Bus Number in the externally visible copy of the register; However, Reads of the internal shadow copy do not display the correct Primary Bus Number nor Secondary Bus Number.

This defect affects only the Bus Number IDs of Completions and messages.

Impact

This defect only affects error messages and CSR Completions that are sent as a result of transactions targeting the PEX 8114 internal resources.

The following transaction types are not affected:

- Data Read completions from downstream devices
- CSR Type 1 Completion from downstream devices
- UR Completions for Type 1 Configuration transactions
- Messages from downstream devices

The Requester ID in messages and the Completer ID in Completions issued as the result of access to the PEX 8114 internal resources can be incorrect.

The following transaction types are affected:

- Messages generated by the PEX 8114 from internal events, *such as* timeouts, malformed packets, and ECRC errors
- Completion for Type 0 (internal to the PEX 8114) CSR Reads and Writes

Workarounds

When modifying the Primary or Secondary Bus Number value by writing to the **Bus Number** register (offset 18h), load the lower 16 bits such that the Primary Bus Number and Secondary Bus Number values are both correct, because both are loaded regardless of the Byte Enable settings.

Another approach is as follows. After enumeration by a BIOS that has corrupted the internal shadow copies of the **Bus Number** register, a device driver could read the correct value of the *Primary Bus Number* and *Secondary Bus Number* registers (offsets 18h[7:0] and [15:8], respectively) (because the visible copy of the register is not corrupt) from the PEX 8114, and then write the value back as a DWord Write, thereby correcting the internal shadow copy of the register.

E26. Requester ID in PME Message Is Cleared to 0

Description

In PCI Forward Transparent Bridge mode, when the PME line is asserted indicating a Power Management Event (PME) on the PCI Bus, the PEX 8114 creates a PME message and sends it to the Root Complex. This PME message should have a Requester ID that indicates the initiating bus. However, the PME message sent by the PEX 8114 incorrectly clears the Requester ID to 0.

Impact

If PME signaling is used, the Requester ID for the PME message is 0.

Workarounds

None.

E27. PEX 8114 reverses its Lane Numbers if it receives Training Sets (TS) with Link Disable Bit set

Description

In PCI or PCI-X Forward or Reverse Transparent Bridge mode, if the PEX 8114 during the course of link up receives Training Sets (TS1/TS2) with Link Disable Bit Set it reverses its Lane Numbers in the following TS ordered sets that it transmits during subsequent Link Training.

Impact

None if the other device supports Lane Reversal. If it does not, then the PCIe Link will not come up. In most systems Link disable is not used.

Workarounds

Issue a PERST# following the Link Disable.

E28. AC-JTAG Not Supported

Description

The SerDes receiver circuitry contains a circuit defect that causes the scan flip-flop to be falsely cleared just before it is to be scanned. The receiver fails to operate reliably at conditions that would normally be used for system level AC-JTAG operations. The conclusion is that the SerDes AC-JTAG model is not reliable for typical system environments and is no longer included in the BSDL file. DC-JTAG (1149.1) is unaffected.

Impact

Boundary-Scan instructions *EXTEST_PULSE* and *EXTEST_TRAIN* are not supported .

Workarounds

None. AC-JTAG has been removed from the BSDL file.

E29. PCI/PCI-X bus REQ# not followed by FRAME# prevents PEX 8114 arbiter from servicing subsequent requests

Description

In forward mode, if a PCI/PCI-X bus REQ# is not followed by FRAME# assertion, this can prevent the PEX 8114 arbiter from servicing subsequent REQ# from another requestor. GNT# will stay asserted for the last requestor. Typical bus masters do not exhibit this behavior, although it is not forbidden by the PCI revision 2.3 specification section 3.4.1(Arbitration Signaling Protocol).

Impact

PCI_GNT# to a subsequent PCI_REQ# may not be asserted.

Workarounds

None.

F. Non-Transparent Mode Only

Note: We do not recommend using the PEX 8114BA in NT mode due to the designated Non-Transparent errata listed below. There is no plan to fix the NT mode errata in future revisions of the PEX 8114.

This section discusses errata that are specific to **Non-Transparent mode only**. In addition to these errata, refer also to the following errata in the **Transparent Mode Only, or Transparent or Non-Transparent Mode** section:

E1. PCI Express Lane Connection Restrictions

E3. EP Bit Erroneously Set in Wrong TLP

E4. Error Pollution – Malformed Packet with Received Target Abort

E6. Parity Error Assertion Detected Is Erroneously Set

E8. No Completion Supplied for Memory-Mapped Configuration Access to Register Offset C08h

E9. In PCI-X Mode, Register Set Erroneously Indicates that PEX 8114 Is Medium Speed Device, Rather than Slow Speed Device

E10. Data Bursts that Cross from 32- to 64-Bit Address Space Have Incorrect Address

E11. Palette Snoop Bit Can Be Set in Forward Bridge Mode

E12. Read Completion Delivery Is Gated by *Bus Master Enable* Bit

E14. Master Data Parity Error Bit Not Set if PERR# Occurs at End of Memory Write

E15. PCI Express Completion Excluded Due to Pending PCI Interrupt Contending with Repetitive PCI Retries

E16. PCI-X Immediate Read Completion Data Overflow

E20 Split Completion Error Incorrectly Caused by Transactions that Access Any of the Last 4 Bytes at Top of Base/Limit or BAR Register

E21 ASPM Re-attempts to Enter L1 State without Waiting the Required 10 µs Delay

E23 PCI Bus Timing

F1. Interrupts on PCI-X Interface Cannot Be Generated by Way of PCI Express Interface, through BAR 1 Using I/O Transactions in NT Mode

Description

In PCI-X Forward Bridge Non-Transparent mode, Interrupt registers located in the PCI-X register set at offsets 90h, 94h, 98h, and 9Ch cannot be accessed from the PCI Express side through BAR 1 using I/O transactions, as they are not mapped in the PCI Express interface I/O space.

Solution/Workaround

Access these registers by using Memory-Mapped transactions through BAR 0, or by using the **Configuration Address** and **Configuration Data** registers implementing indirect register access.

Impact

Interrupts on the PCI-X Bus cannot be generated by way of the PCI Express interface, through BAR 1 using I/O transactions.

F2. Loss of Link Does Not Cause PEX 8114 Reset in NT Mode

Description

In PCI or PCI-X Forward Bridge Non-Transparent mode, the PEX 8114 does not automatically go into reset if the PCI Express link becomes non-operational and the Data Link Layer reports DL_Down status to the Transaction Layer (indicating that the link is non-operational). However, the advertised credits are reset to initial values that represent a device with all internal memory available. With the advertised credits reset, but some of the memory consumed, the PEX 8114 can run out of memory.

Solution/Workaround

The PCI Express Host must reset the PEX 8114 when it detects the link reporting DL_Down status.

Impact

Memory overflows can result from advertised available credit being reinitialized.

F3. NT Mode I/O BAR Access to Internal Registers Fails If *Bus Master Enable* Bit Is Not Set

Description

In PCI or PCI-X Forward Bridge Non-Transparent mode, BAR 1 is an I/O BAR used to access the first 256 bytes of the internal Configuration registers. For I/O accesses from the PCI-X interface, if the **Command** register *I/O Access Enable* bit is set (offset 04h[0]=1), the PEX 8114 should accept accesses that target BAR 1.

However, and incorrectly, if the PCI Express interface **Command** register *Bus Master Enable* bit is cleared (offset 04h[2]=0), the PEX 8114 does not accept the I/O transaction.

If the PCI Express interface *Bus Master Enable* bit and PCI-X interface *I/O Access Enable* bit are both set (offset 04h[2, 0]=11b), the PEX 8114 accepts transactions targeting BAR 1.

Solution/Workaround

Use software to set the PCI Express interface **Command** register *Bus Master Enable* bit (offset 04h[2]=1) before attempting BAR 1 accesses, or use the serial EEPROM load to set the bit.

Impact

A PCI Express Completion time out occurs if the **Command** register *Bus Master Enable* bit is not set and an I/O access is attempted.

F4. NT Mode ECRC Fails to Set *Detected Parity Error* Bit

Description

In PCI or PCI-X Forward Bridge Non-Transparent mode, per the *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0,* the PEX 8114 must set the **Status** register *Detected Parity Error* bit (offset 04h[31]=1) when a TLP with an ECRC error is detected; however, the PEX 8114 does not set the bit.

Solution/Workaround

None.

Impact

The **Status** register *Detected Parity Error* bit is not set when a TLP with an ECRC error is detected.

F5. NT Mode Split Completion Error Erroneously Caused by Transaction that Approaches Top of BAR or BAR Limit Register

Description

In PCI-X Forward Bridge Non-Transparent mode, if a Burst Read Request from the PCI-X Bus comes within 4 KB of the top of the BAR or the BAR **Limit** register, all requested data is correctly sent to the PCI-X endpoint; however, an erroneous Split Completion Error message, indicating an out-of-bounds transaction, follows the data.

Solution/Workaround

Use one of the following workarounds:

- Set the **Limit** register higher than necessary
- Do not use data locations within the top 4 KB of the BAR
- Ignore the erroneous Split Completion message

Impact

A device (other than a bridge) that receives a Split Completion message with the *Split Completion Error* attribute bit set must set its **PCI-X Status** register *Received Split Completion Error Message* bit (offset 5Ch[29]. A device (requester or bridge) that receives a Split Completion message reporting an error condition that corresponds to Non-Posted Write Uncorrectable Data errors, Master Abort conditions, and Target Abort conditions must set the corresponding bit in the Conventional **PCI Status** register (offset 04h) [or **Secondary Status** register (offset 1Ch) in a bridge].

Refer to *PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0a*, Section 5.2.6, for further details.

F6. Non-Transparent Conversion from 32-to-64-Bit Address Transactions Failure

Description

In PCI Forward Bridge Non-Transparent mode, transactions initiated on the PCI Express interface as 32-bit Address transactions should be able to be translated across the bridge to 64-bit Address transactions on the PCI Bus. This translation works for transactions that target **BAR 2/BAR 3**; however, it does not function correctly when the transaction targets **BAR 4/BAR 5** – the **BAR 2/BAR 3** setup applies not only to **BAR 2/BAR 3**, but to **BAR 4/BAR 5** as well.

Solution/Workaround

Use **BAR 4/BAR 5** such that all PCI Express transactions that enter **BAR 4/BAR 5** are 64-bit Address transactions. These 64-bit transactions are correctly translated to either 32- or 64-bit Address transactions. Or, if possible, plan **BAR 4/BAR 5** such that the translation configured for **BAR 2/BAR 3** is acceptable for **BAR 4/BAR 5** transactions.

Impact

Limited to one set of BARs for 32- to 64-bit address translation; **BAR 4/BAR 5** cannot be used for 32- to 64-bit translation.

F7. Configuration Accesses from PCI-X-to-PCI Express Overwrite Values in PCI Express Captured Bus Number and Captured Device Number Registers

Description

In PCI-X Forward Bridge Non-Transparent mode, registers on the PCI Express interface that can be accessed through Configuration transactions from the PCI-X Bus are:

- **IRQ** registers, offsets A0h through ACh
- **Scratchpad** registers, offsets B0h through CCh
- **BAR Setup** registers, offsets E4h through F4h

PCI-X-to-PCI Express Configuration accesses to these registers overwrite the PCI Express interface's **Captured Bus Number** and **Captured Device Number** register values to the same values as those in the PCI-X domain. This corrupts the PCI Express domain's Requester ID, which must be used in subsequent transactions.

Solution/Workaround

a. The PCI-X interface is configured first and during this time, the PCI Express interface attempts Configuration Retries. After the BIOS performs its tasks and the operating system boots on the PCI-X Bus, the PCI Express interface is enabled to accept Configuration transactions. The operating system can then use Memory-Mapped transactions instead of Configuration transactions, because Memory-Mapped transactions use the correct Bus Number and do not have the problem experienced with Configuration transactions.

b. Access these registers with Memory-Mapped accesses to the Device-Specific registers.

Impact

When the NT PCI Express interface **Captured Bus Number** and **Captured Device Number** registers are corrupted, Memory Requests generated by the NT PCI Express interface contain the wrong Requester ID. When the Completion for this Memory Read Request is received, it can be misrouted because the corresponding Memory Read Request contains the wrong Requester ID.

F8. Serial EEPROM Fails to Load Advanced Error Reporting Capabilities and Control Register in NT Mode

Description

In PCI or PCI-X Forward Bridge Non-Transparent mode, during serial EEPROM load, the **Advanced Error Reporting Capabilities and Control** register (offset FCCh) is not loaded correctly, which causes the value loaded to have no effect on bridge functionality. Although the register can be read back and appears to loaded correctly, it functions as if set to its power-on reset default value. The Power-on reset value is 0h, which turns Off the *ECRC Check Enable* and *ECRC Generation Enable* bits (offset FCCh[8, 6]=00b).

Solution/Workaround

After the serial EEPROM load, the Configuration register at offset FCCh can be written to with a Configuration Write transaction, which sets offset FCCh to the correct value.

Impact

ECRC is not checked nor generated correctly if the **Advanced Error Reporting Capabilities and Control** register *ECRC Check Enable* or *ECRC Generation Enable* bits are cleared (offset FCCh[8 or 6]=0) during serial EEPROM load.

F9. Base and Limit Boundary Circuit Fails to Stop Bursts across Top of Memory Space

Description

The following three instances of the PEX 8114BA silicon not stopping bursts across the top of non-power of 2 Limit-defined Memory space in Non-Transparent mode have been found:

a. Prefetching Bursts through Top of Non-Power of 2 Limit-Defined Memory Spaces on PCI Memory Reads

   In PCI Forward Bridge Non-Transparent mode, using the shortened Limit memory addressing (refer to the *PEX 8114BA Data Book, v1.1*, Section 5.3.5.4) with the **Limit** register programmed such that the top end of the BAR is restricted to an ending address that does not end on a 4-KB or Cache Line/Prefetch boundary, if a PCI Read Request is initiated on the PEX 8114 PCI Bus, The PEX 8114 can initiate a Prefetchable Read request (equal to one Cache Line Size) on the PCI Express interface that erroneously crosses over the top limit of the BAR. This Burst Read over the top of the non-power of 2 limit of the BAR occurs if the Start address of the Read request is less than one Cache Line Size from the top of the non-power of 2 Limit Memory space.

   ### Solution/Workaround

   The application software accessing the device should ensure that the Memory Read/Memory Read Line/Memory Read Line Multiple commands do not have a starting address that, in conjunction with the **Prefetch** register *Prefetch Space Count* (offset FA4h[13:8]) and **Miscellaneous Control** register *Cache Line Size* (offset 0Ch[7:0]), cross over the top of the Base and Limit-defined Memory space.

   ### Impact

   Burst Read crosses the top of a non-power of 2 Limit-defined Memory space on the PCI Express interface if the Read is executed to Prefetchable Memory space from the PCI Bus, with the beginning of the Read closer to the top of the Base and Limit-defined Memory space than the Prefetch or Cache Line Size. This can result in a Master Abort in cases where the next sequential addresses after the Base and Limit-defined Memory space are not supported or might have other consequences, depending on the address map of the system.

b. Base and Limit Boundary Circuit Fails to Stop Bursts through Top of Base and Limit-Defined Memory Space on PCI-X 4-KB Transactions

In PCI-X Forward Bridge Non-Transparent mode, when a PCI-X Read Request is exactly 4 KB in size, the PCI Express Write or Read of a PCI Express endpoint bursts through the top of the non-power of 2 Limit-defined Memory space (refer to the *PEX 8114BA Data Book, v1.1*, Section 5.3.5.4), if the beginning address is closer than 4 KB to the top of the Base and Limit-defined Memory space.

Solution/Workaround

The application software accessing the device should ensure that the starting address is at least 4 KB from the top of the Base and Limit-defined Memory space for a 4-KB Write or Read request.

Impact

Burst Read crosses the top of a non-power of 2 Limit-defined Memory space on the PCI Express interface if a 4-KB Write or Read is executed from the PCI-X Bus, with the beginning of the Read closer to the top of the Base and Limit-defined Memory space than 4 KB. This can result in a Master Abort in cases where the next sequential addresses after the Base and Limit-defined Memory space are not supported or might have other consequences, depending on the address map of the system.

c. BAR Boundary Circuit Fails to Stop Bursts through Top of BAR Limit

In PCI or PCI-X Forward Bridge Non-Transparent mode, the endpoint bursts through the top of the BAR when a Non-Transparent PCI or PCI-X endpoint initiates a Write or Read, with a beginning address and length that exceed the BAR **Limit** register value. This problem occurs when accessing BAR 2, 4, or 5, and the **Limit** register is set to a non-zero value.

Solution/Workaround

Read and Write commands must be issued such that the beginning address and length do not exceed the BAR **Limit** register value.

Impact

This can result in a Master Abort in cases where the next sequential addresses after the BAR are not supported or might have other consequences, depending on the address map of the system.

F10. In Non-Transparent Mode, BAR 2 Setup Register Prefetchable Bit Is Used as Part of Base Address when Accessing from PCI Express Side of the Bridge

Description

In PCI or PCI-X Non-Transparent mode, the PEX 8114 incorrectly uses the **BAR 2 Setup** register *Prefetchable* bit (offset D4h[3]) as part of the BAR's Base address when accessing the bridge from the PCI Express link. This results in the first eight locations, which should be accepted during a Downstream access, being rejected.

Solution/Workaround

Double the size of the BAR window and use only the top half in locations accessed by the PCI Express interface that cannot be adjusted up by eight locations.

Impact

The lower eight bytes of the bytes programmed into the **BAR 2 Setup** register are not accepted by the bridge as being within the BAR's Address Range window.

F11. Interrupt Request (Doorbell) Registers Do Not Function Correctly in Non-Transparent Mode

Description

In PCI or PCI-X Non-Transparent mode, the PEX 8114 should assert PCI_INTA# on the PCI-X side of the bridge in response to a Write to the PCI Interrupt registers from the PCI Express side of the bridge. However, this does not occur. The PEX 8114 should also generate an Assert_INTA# message or MSI Interrupt Write on the PCI Express side of the bridge in response to a Write to the PCI Express Interrupt registers from the PCI-X side of the bridge. This works, but not by accessing the registers listed in the *PEX 8114BA Data Book, v1.1*. To generate an Assert_INTA# or MSI on the PCI Express side of the bridge, use the **Set PCI-X Interface IRQ** register *Set IRQ* field (offset 90h[15:0]).

Solution/Workaround

a. Poll the **Mailbox** registers.

b. Process Memory Writes across the bridge, to imitate MSI interrupts.

c. If an Interrupt Line assertion becomes necessary, and all Clock outputs are not being used, use the spare Clock lines and write to the **PCI Clock Enable** register *PCI_CLKO_EN[3:0]* field (offset FA0h[3:0]) to enable or disable the Clock output. This causes a Pulsing interrupt when enabled, or a High when disabled.

d. To cause an MSI interrupt or Assert_INT*x*# on the PCI Express side of the bridge, write to the **Set PCI-X Interface IRQ** register *Set IRQ* field (offset 90h[15:0]). This causes an MSI to be sent to the PCI Express side of the bridge if MSI is enabled, or an Assert_INT*x*# if MSI is not enabled.

Impact

The NT mode Interrupt Request feature does not function as described in the *PEX 8114BA Data Book, v1.1*.

G. Cautions

G1. Reverse Bridge Mode PCI Express Non-Fatal Errors are Translated into PCI_SERR# on PCI Bus

Description

In PCI and PCI-X Reverse Bridge Transparent mode, Fatal and Non-Fatal errors that occur on the PCI Express side of the bridge are translated into a PCI_SERR# assertion on the PCI side of the bridge. This occurs because the *PCI Express to PCI/PCI-X Bridge Specification, r1.0,* Section A.5.3, requires that, "A reverse bridge is required to convert all Error Fatal and Error Non-Fatal messages into SERR# on the PCI interface." This requirement causes problems because certain boards send a Non-Fatal Error message when, during the enumeration process, the system polls non-existent Function Numbers on the board. When these Non-Fatal Error messages are converted into SERR# signal assertions in current PCI systems, SERR# causes the system to shut down.

Solution/Workaround

Ignore SERR# if possible. Alternatively, PCI Express endpoints should not generate Non-Fatal errors.

Impact

The system is susceptible to possible SERR# signals being generated by PCI Express Non-Fatal Error messages, which might cause the system to hang or bluescreen.

G2. Serial EEPROM Control Register Must Be in Benign State to Allow Access to Serial EEPROMs

Description

In PCI or PCI-X Non-Transparent mode, the Expansion ROM is inaccessible following modification of the serial EEPROM values if the user software leaves the **Serial EEPROM Control** register *Serial EEPROM Command* field (offset 260h[15:13]) loaded with a non-zero value.

Solution/Workaround

After modifying the serial EEPROM, the **Serial EEPROM Control** register *Serial EEPROM Command* field (offset 260h[15:13]) should be loaded with the value 000b, the register's power-on reset value.

Impact

If the user software loads the serial EEPROM using the **Serial EEPROM Control** register and, at the conclusion of the load, does not write the control register back to its power-on reset value and does not reboot the system, the Expansion ROM might not be accessible.

G3. Single Data Phase PCI Read Requests Generate TLPs with a Size Determined by Prefetch Count and Not Limited by Single Data Phase Size

Description

In PCI-X Forward or Reverse Bridge Transparent and Non-Transparent mode, if the PCI endpoint issues a Read request, the Prefetch Size of the request forwarded to the PCI Express endpoints is determined by the value in the **Prefetch** register *Prefetch Space Count* field (offset FA4h[13:8]).

If a PCI Read request is a single Data phase Read request, where the PCI_FRAME# signal drops for only one Clock cycle, that Read request can be determined to require only 4 or 8 DWords, depending on the bus width. Currently, the PEX 8114 prefetches the number of bytes in the **Prefetch** register *Prefetch Space Count* field, which can be more than the 4 or 8 DWords indicated by the single Data phase Read request. This problem was experienced when a PCI Express endpoint failed to complete the transaction for the larger Byte Count.

Solution/Workaround

Clear the **Prefetch** register *Prefetch Space Count* field to 00h.

G4. Memory Read Line, Memory Read Multiple commands issued on PCI bus for PCI Express-to-PCI reads

Description

When the PEX 8114 is operating as a PCI Express-to-PCI forward bridge, Memory Read Request TLPs to Non-Prefetchable PCI Address Space received by PEX 8114's PCI Express interface will be completed on PCI bus using a combination of Memory Read Multiple (MRM), Memory Read Line (MRL) or single DWord Memory Read (MR) transactions. PEX 8114 will use the faster MRM/MRL commands to read PCI data up to the end of the last cache line boundary (defined by PCI CSR 0Ch, Miscellaneous Control[7:0]) that occurs on or before the last DWord to be read on PCI. Remaining DWords located after the last cache line boundary will be read using single MR accesses.

Example 1. If the Cache Line Size is eight DWords and PEX 8114 receives a Memory Read Request TLP for ten DWords at address xxxx.xx00h, the PEX 8114 will issue a single MRL command for the first request. This will return eight Dwords. The remaining two DWords (at offsets 00h, 04h) would then be read using two MR accesses This method requires three transactions on PCI bus.

Example 2. If the Cache Line Size is eight DWords and PEX 8114 receives a Memory Read Request TLP for ten DWords at address xxxx.xx04h, the PEX 8114 will issue a single MRL command for the first request. This will return seven DWords. The remaining three DWords (at offsets 00h, 04h, 08h) would then be read using three MR accesses This method requires four transactions on PCI bus.

Example 3. If the Cache Line Size is 8 DWords, and a Memory Read Request TLP is received requesting 1 DW at address xxxx.xx1C, the PEX 8114 will issue a single MRL command to the PCI bus. This is because the last word read from PCI lies at the end of a cache line.

Solution/Workaround

None.

G5. PCI-X Interface May Respond With Retry Response to a Split Completion Request in a Specific Case

Description

PCI-X Protocol Specification v2.0a, Section 8.4.5 specifies that a bridge is permitted to terminate a Split Completion transaction with Retry in specific cases only. PEX 8114 will also terminate a Split Completion transaction with Retry in the following additional cases.

Case 1:

If PEX 8114's PCI-X interface receives a non-aligned Memory Write Block transaction (with byte enables de-asserted between the first DWord and last DWord), and the Memory Write Block request is followed closely by a Split Completion Request, the PEX 8114 may terminate the Split Completion with a Retry. When this occurs, the *Split Completion Overrun* bit, 58h[20], will be set. The reason for this behavior is because a write request with discontinuous byte enables must be internally decomposed into two PCI Express Memory Write TLPs. Formation and forwarding of the additional TLP requires additional PCI-X clock cycles following the write transaction on PCI-X. This time can vary, but in the minimum (ideal) case, 18 clock cycles are required between the end of the write transaction and the next transaction request. During this interval, any requests received on PCI-X bus, including Split Completion Requests, will be terminated with Retry by PEX 8114.

Case 2:

(Forward Bridge Only)

If PEX 8114 detects a transition on any PCI_INT*n*# input ball, rising or falling, occurring within 5 PCI-X clocks of a Split Completion Request (or any request) received on PCI-X bus, the Split Completion Request will be terminated with Retry by PEX 8114. This 5-clock time interval is increased if additional transitions on any PCI_INT*n*# ball are received during that time (two transitions within 10 clocks, three within 15, etc.).

Solution/Workaround

None. If the PCI-X device that issued the split completion repeats the Split Completion request, the completion is forwarded to PCI Express as expected.