PCI 9656RDK-LITE
Hardware Reference Manual

PCI 9656RDK-LITE
Hardware Reference Manual

Version 1.4

January 2006

Website: http://www.plxtech.com/
Technical Support: http://www.plxtech.com/support/
Phone: 408 774-9060
800 759-3735
Fax: 408 774-2169

Order Number: PCI 9656/LITE-RDK-HRM-P1-1.4

Printed in the USA, January 2006

PREFACE

NOTICE

This document contains PLX Confidential and Proprietary information. The contents of this document may not be copied nor duplicated in any form, in whole or in part, without prior written consent from PLX Technology, Inc.

PLX provides the information and data included in this document for your benefit, but it is not possible to entirely verify and test all the information, in all circumstances, particularly information relating to non-PLX manufactured products. PLX makes neither warranty nor representation relating to the quality, content, or adequacy of this information. The information in this document is subject to change without notice. Although every effort has been made to ensure the accuracy of this manual, PLX shall not be liable for any errors, incidental, or consequential damages in connection with the furnishing, performance, or use of this manual or examples herein. PLX assumes no responsibility for damage or loss resulting from the use of this manual, for loss or claims by third parties, which may arise through the use of the Rapid Development Kit (RDK), or for any damage or loss caused by deletion of data as a result of malfunction or repair.

ABOUT THIS MANUAL

This document describes the PLX PCI 9656RDK-LITE Rapid Development Kit from a hardware perspective. It contains a description of all major functional circuit blocks on the board. This manual also includes the complete schematics and bill of materials.

The PCI 9656RDK-LITE supports designs with either multiplexed or non-multiplexed generic Processor/Local Buses (J or C Processor/Local Bus Modes). For Motorola PowerQUICC designs (M Processor/Local Bus Mode), use the CompactPCI 9656RDK-860.

For all software installation and usage information, refer to the Software Development Kit (SDK) documentation.

DOCUMENT INFORMATION

REVISION HISTORY

Date	Version	Comments
November 2000	0.50	Yellow Book Initial Release
March 2003	1.0	Production Release
April 2003	1.1	Corrected EEPROM tables
October 2004	1.2	Updated CPLD code, EEPROM table, BOM and schematics
May 2005	1.3	Modified table 2-8 by adding R71 and R79
January 2006	1.4	Updated Figure 1-1

TABLE OF CONTENTS

1. GENERAL INFORMATION 1

1.1 About the PCI 9656RDK-LITE 1
1.2 Features 2
1.3 RDK Installation 2

2. HARDWARE ARCHITECTURE 3

2.1 System Architecture 4
2.2 PCI 9656 4
2.3 Hardware Memory Map 4
2.4 Serial EEPROM 5
2.4.1 Serial EEPROM Contents 5
2.5 Synchronous Burst SRAM 7
2.6 Xilinx CPLD 7
2.7 Test Headers 7
2.8 PLX Option Module Connector 7
2.9 Hardware Modules 7
2.9.1 RS-232 Interface 7
2.9.2 Debug and Status LEDs 8
2.9.3 Reset Circuitry 8
2.9.4 Flash ROM Socket 8
2.10 Prototyping Area 8
2.10.1 Surface Mount Footprints 8
2.10.2 BGA Footprints 8
2.11 Power Supply 11
2.12 RDK Mode Configuration 11

3. EXAMPLES OF TESTING THE ONBOARD 32KX32 SRAM WITH PLXMON 12

4. CPLD VERILOG CODE 13

4.1 Verilog Code 13

5. BILL OF MATERIALS / SCHEMATICS 17

LIST OF FIGURES

Figure 1-1. PCI 9656RDK-LITE Layout Diagram 1

Figure 2-1. PCI 9656RDK-LITE Hardware Block Diagram..... 3

Figure 2-2. BGA Device Prototyping Diagram..... 9

LIST OF TABLES

Table 2-1. PCI 9656RDK-LITE Processor/Local Bus Memory Map..... 4

Table 2-2. Long Serial EEPROM Load Registers 5

Table 2-3. Extra Long Serial EEPROM Load Registers..... 6

Table 2-4. RS-232 Transceiver Configuration..... 7

Table 2-5. Reset Circuit Configuration 8

Table 2-6. Thirty (30) Surface Mount Footprints 10

Table 2-7. Two BGA Footprints..... 10

Table 2-8. RDK Board Mode Configuration..... 11

Table 5-1. Bill of Materials 17

1. GENERAL INFORMATION

1.1 About the PCI 9656RDK-LITE

The PCI 9656RDK-LITE (RDK-LITE) is a flexible development platform for designs using the PCI 9656 with generic 32-bit Processor/Local Bus devices. The RDK-LITE is shipped pre-configured for de-multiplexed generic address/data bus (C mode) operation, but is very easily reconfigured for multiplexed address/data bus (J mode) applications. The RDK-LITE provides 30 surface-mount footprints and 2 BGA footprints for hardware designers to easily add processors, DSPs, ASICs, FPGAs, memory, and I/O devices to test, simulate, and debug their designs without fabricating their own boards. This can save a considerable amount of time and money in the development process and shorten time to market. The PCI 9656RDK-LITE's software, hardware registers and footprints are backward compatible with the PCI 9054RDK-LITE, simplifying the migration of existing 32-bit, 33 MHz PCI designs into 64-bit, 66 MHz PCI products.

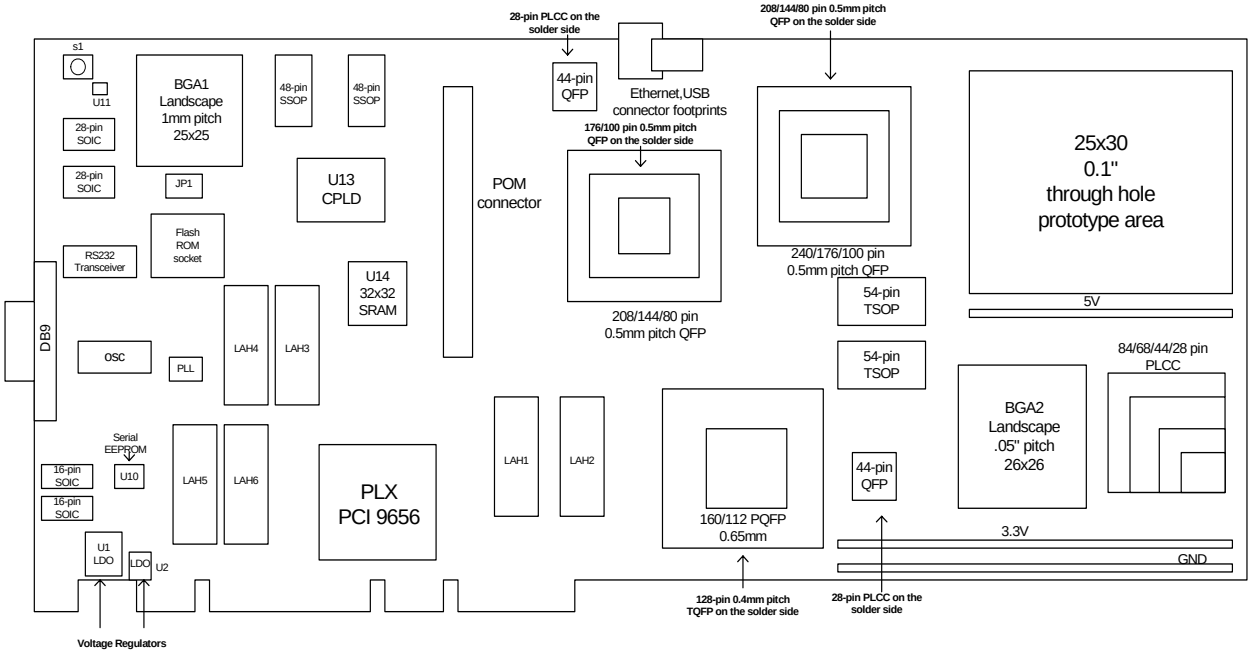


Figure 1-1. PCI 9656RDK-LITE Layout Diagram

1.2 Features

The PCI 9656RDK-LITE is a flexible 64-bit, 66 MHz PCI Bus Master Rapid Development Kit (RDK), containing a six-layer assembled 12.28"L x 5.20"W PC board with the following features:

- PLX PCI 9656 PCI I/O Accelerator in a 272-pin 1.27mm ball pitch PBGA package
- Supports 64-bit PCI bus operation with speeds up to 66 MHz
- Supports 32-bit C (default) or J mode Processor/Local Bus operation with speeds up to 66 MHz
- Large prototyping area with thirty (30) surface mount footprints, two (2) common pitch BGA footprints, and one (1) 25x30, 0.1" through-hole grid
- Socketed serial EEPROM for configuring the PCI 9656
- Boot Flash ROM socket
- 128KB synchronous SRAM with CPLD memory controller demonstrates the PCI 9656 continuous burst feature
- One (1) power-on LED and four (4) user defined status/debug LEDs
- Built-in DB9 connector and programmable DTE/DCE RS-232 transceiver for adding a serial port
- Pushbutton reset module at the Processor/Local Bus, user-configurable for $D3_{COLD}$ PME# generation
- Socketed oscillator for Processor/Local Bus clock and PLLs
- A 5V to 3.3V voltage regulator allows the card to be plugged into 5-volt only PCI slots
- Six logic analyzer headers with standard HP footprint facilitate probing of Processor/Local Bus signals
- RJ45 connector and USB type A connector footprints for I/O expansion
- PLX J-Bus Option Module (POM) connector for expansion

1.3 RDK Installation

To install the RDK hardware into your computer, please refer to your computer's instruction manual for the correct preparation and installation for adding a PCI card.

For all RDK software installation and usage information, refer to the Software Development Kit (SDK) documentation.

2. HARDWARE ARCHITECTURE

This section provides a detailed description of the hardware included in the PCI 9656RDK-LITE. Figure 2-1 shows the RDK hardware block diagram.

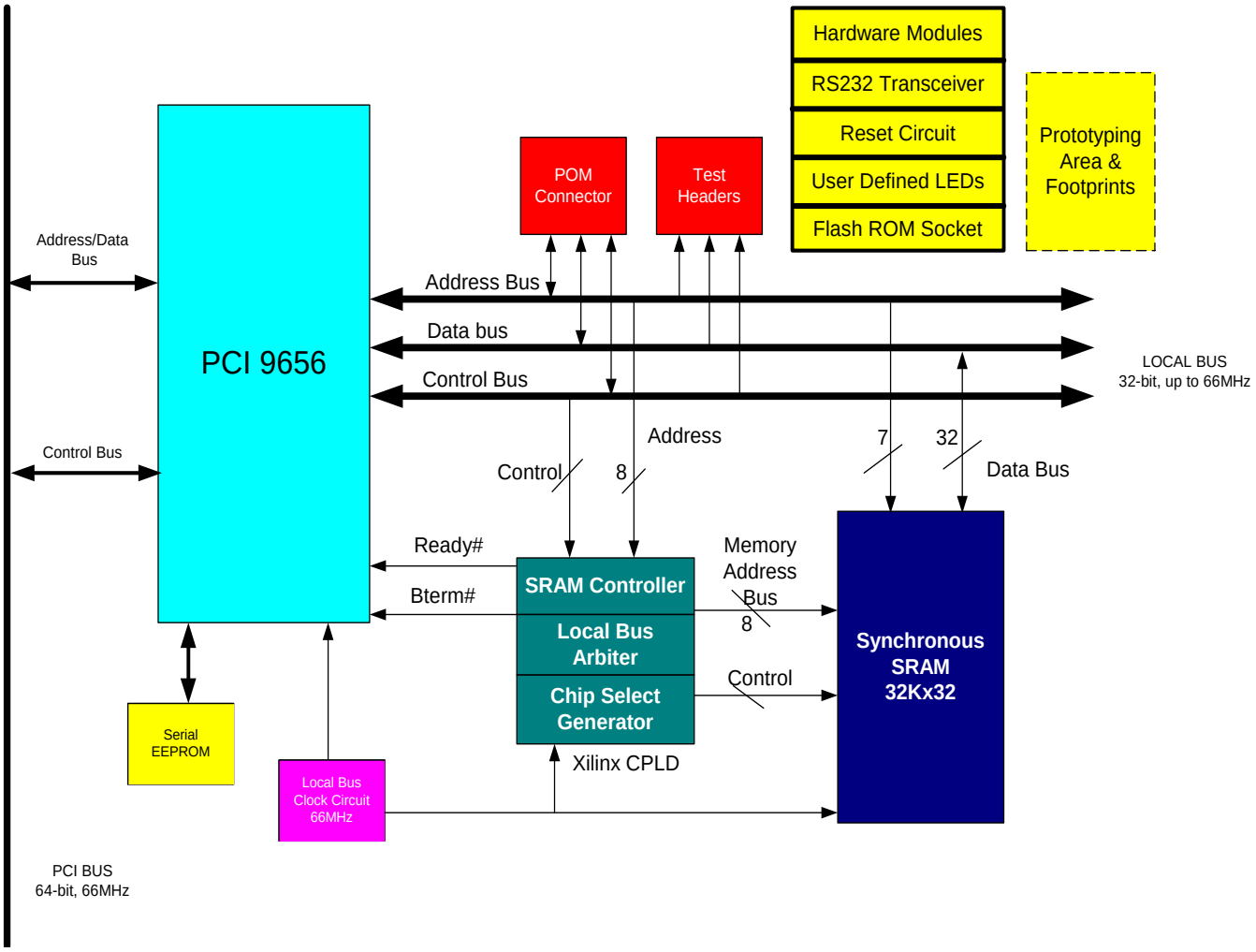


Figure 2-1. PCI 9656RDK-LITE Hardware Block Diagram

2.1 System Architecture

As shown in Figure 2-1, the RDK hardware contains:

- The PCI 9656 64-bit, 66 MHz PCI I/O Accelerator
- Four PCI 9656 Processor/Local Bus components (CPLD, SRAM, Test Headers, and POM connector)
- Four hardware development modules (LEDs, Flash ROM Socket, Reset Circuitry, and RS232 Interface)
- Large prototyping area

The RDK's Processor/Local Bus is pre-configured for non-multiplexed address and data bus operation (C mode), but it is user configurable for multiplexed address and data operation (J Mode). (See Section 2.12 for details on re-configuring the RDK hardware for J Mode operation.) Once the board is correctly installed into a PC computer system, a PCI master, such as the motherboard's processor, can perform single memory read/write cycles, multiple memory read/write cycles, and burst memory read/write cycles from/to the on-board synchronous SRAM in Direct Slave mode. The microprocessor can also program the PCI 9656 I/O Accelerator to perform DMA data transfers between the PCI bus and the SRAM.

Four hardware development modules in the RDK provide the basic hardware building blocks for PCI 9656-based generic bus designs.

Thirty (30) surface-mount footprints, two (2) BGA footprints, and a 25x30, 0.1" through-hole grid allow fast prototyping of processors, DSPs, memory, I/O devices, etc.

2.2 PCI 9656

The PLX PCI 9656 is a 64-bit, 66 MHz PCI Bus Master I/O Accelerator for PowerQUICC and Generic 32-bit, 66 MHz Processor/Local Bus designs. It is a PCI r2.2 and PICMG 2.1 r2.0 CompactPCI Hot Swap compliant device. It features PLX's Data Pipe Architecture®, which includes two DMA channels, Direct Slave and Direct Master data transfer, EOT and Demand Mode, and an Intelligent Messaging Unit. For more detailed information about the PCI 9656, please refer to the PCI 9656 Data Book.

2.3 Hardware Memory Map

The PCI 9656RDK-LITE board Processor/Local Bus memory map is shown in Table 2-1.

Table 2-1. PCI 9656RDK-LITE Processor/Local Bus Memory Map

Hex Address Range	Device	Chip Select	Comments
FFFF FFFF 5000 0000	Unused	–	Available
4FFF FFFF 4000 0000	Unused	CS3#	Available & Re-programmable
3FFF FFFF 3000 0000	Unused	CS2#	Available & Re-programmable
2FFF FFFF 2000 0000	Unused	CS1#	Available & Re-programmable
1FFF FFFF 1000 0000	J mode POM connector	CS0#	32-bit, multiplexed address/data bus
0FFF FFFF 0002 0000	Unused	–	Available
0001 FFFF 0000 0000	Synchronous SRAM 32Kx32	SRAMCS#	8-, 16-, or 32-bit access

2.4 Serial EEPROM

A socketed 2 Kbit serial EEPROM (U10) is used in this RDK. It is connected directly to the PCI 9656 and provides the configuration data to initialize the PCI 9656 after the system reset is removed. There are 100 bytes of pre-programmed configuration data in the serial EEPROM, which include device and functional information for Plug-and-Play (PnP), PCI memory resource allocation, and initial values of internal registers.

2.4.1 Serial EEPROM Contents

Table 2-2. Long Serial EEPROM Load Registers

Serial EEPROM Offset	Serial EEPROM Hex Value	Description	Register Bits Affected
0h	9601	Device ID	PCIIDR[31:16]
2h	10B5	Vendor ID	PCIIDR[15:0]
4h	0680	Class Code	PCICCR[23:8]
6h	00BA	Class Code, Revision of the PCI 9656	PCICCR[7:0] / PCIREV[7:0]
8h	0000	Maximum Latency, Minimum Grant	PCIMLR[7:0] / PCIMGR[7:0]
Ah	0100	Interrupt Pin, Interrupt Line Routing	PCIIPR[7:0] / PCIILR[7:0]
Ch	0000	MSW of Mailbox 0 (User Defined)	MBOX0[31:16]
Eh	0000	LSW of Mailbox 0 (User Defined)	MBOX0[15:0]
10h	0000	MSW of Mailbox 1 (User Defined)	MBOX1[31:16]
12h	0000	LSW of Mailbox 1 (User Defined)	MBOX1[15:0]
14h	FFFE	MSW of Range for PCI-to-Local Address Space 0	LAS0RR[31:16]
16h	0000	LSW of Range for PCI-to-Local Address Space 0	LAS0RR[15:0]
18h	0000	MSW of Local Base Address (Re-map) for PCI-to-Local Address Space 0	LAS0BA[31:16]
1Ah	0001	LSW of Local Base Address (Re-map) for PCI-to-Local Address Space 0	LAS0BA[15:0]
1Ch	0120	MSW of Mode/DMA Arbitration Register	MARBR[31:16]
1Eh	0000	LSW of Mode/DMA Arbitration Register	MARBR[15:0]
20h	2030	Local Miscellaneous Control Register 2 / Serial EEPROM Write-Protected Address Boundary	LMISC2[7:0] / PROT_AREA[7:0]
22h	8500	Local Miscellaneous Control Register 1 / Processor/Local Bus Big/Little Endian Descriptor Register	LMISC1 [7:0] / BIGEND [7:0]
24h	0000	MSW of Range for PCI-to-Local Expansion ROM	EROMRR[31:16]
26h	0000	LSW of Range for PCI-to-Local Expansion ROM	EROMRR[15:0]
28h	0000	MSW of Local Base Address (Re-map) for PCI-to-Local Expansion ROM	EROMBA[31:16]
2Ah	0000	LSW of Local Base Address (Re-map) for PCI-to-Local Expansion ROM	EROMBA[15:0]
2Ch	4343	MSW of Bus Region Descriptors for PCI-to-Local Address Space 0 and Expansion ROM	LBRD0[31:16]
2Eh	00C3	LSW of Bus Region Descriptors for PCI-to-Local Address Space 0 and Expansion ROM	LBRD0[15:0]
30h	0000	MSW of Range for Direct Master-to-PCI	DMRR[31:16]
32h	0000	LSW of Range for Direct Master-to-PCI	DMRR[15:0]

Serial EEPROM Offset	Serial EEPROM Hex Value	Description	Register Bits Affected
34h	5000	MSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[31:16]
36h	0000	LSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[15:0]
38h	4000	MSW of Processor/Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[31:16]
3Ah	0000	LSW of Processor/Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[15:0]
3Ch	0000	MSW of PCI Base Address (Re-map) for Direct Master-to-PCI	DMPBAM[31:16]
3Eh	0000	LSW of Processor/Local Bus Address for Direct Master-to-PCI Memory	DMPBAM[15:0]
40h	0000	MSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCRGA[31:16]
42h	0000	LSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCFGA[15:0]

Table 2-3. Extra Long Serial EEPROM Load Registers

Serial EEPROM Offset	Serial EEPROM Hex Value	Description	Register Bits Affected
44h	9656	Subsystem ID	PCISID[15:0]
46h	10B5	Subsystem Vendor ID	PCISVID[15:0]
48h	FFFE	MSW of Range for PCI-to-Local Address Space 1	LAS1RR[31:16]
4Ah	0000	LSW of Range for PCI-to-Local Address Space 1	LAS1RR[15:0]
4Ch	0000	MSW of Local Base Address (Re-map) for PCI-to-Local Address Space 1	LAS1BA[31:16]
4Eh	0001	LSW of Local Base Address (Re-map) for PCI-to-Local Address Space 1	LAS1BA[15:0]
50h	0000	MSW of Bus Region Descriptors for PCI-to-Local Address Space 1	LBRD1[31:16]
52h	01C3	LSW of Bus Region Descriptors for PCI-to-Local Address Space 1	LBRD1[15:0]
54h	0000	Hot Swap Control/Status Register	Reserved
56h	4C06	Hot Swap Control/Status Register / Hot Swap Next Capability Pointer	HS_NEXT[7:0] / HS_CNTL[7:0]
58h	0000	Reserved	Reserved
5Ah	0000	PCI Arbiter Control	PCIARB[15:4] / PCIARB[3:0]
5Ch	7A02	Power Management Capabilities	PMC[15:9,2:0]
5Eh	4801	Power Management Next Capability Pointer / Power Management Capability ID (the LSB is reserved)	PMNEXT[7:0] / PMCAPID[7:0]
60h	0000	Power Management Data / PMCSR Bridge Support Extensions (the LSB is reserved)	PMDATA[7:0]/ PMCSR_BSE[7:0]
62h	0000	Power Management Control/Status (Bits 15, 7:2, and 1:0 are reserved)	PMCSR[15:0]

2.5 Synchronous Burst SRAM

A 100-pin, 7.5ns, 32K x 32 Micron Synchronous Burst SRAM (U14) is used for Processor/Local Bus data storage on the RDK. During Direct Slave memory burst cycles, the SRAM performs continuous back-to-back single read cycles or single write cycles. The Xilinx CPLD SRAM controller (U13) does all of the timing conversion and generates the lower 8 address bits to the SBSRAM. The SBSRAM takes 7 upper address lines (LA16-LA10) directly from the PCI 9656 and 8 lower address lines (MA[9:2]) from the SRAM controller. The data lines of the SRAM are directly connected to the PCI 9656 local data bus (LD31-LD0).

2.6 Xilinx CPLD

A 5ns Xilinx XC9572XL-5TQ100C CPLD (U13) is used as the SRAM controller, external Processor/Local Bus arbiter, and chip select generator.

The SRAM controller in the CPLD generates the lower 8-bit memory address (MA[9:2]), SRAM chip select (SRAMCS#), SRAM output enable (SRAMOE#), and SRAM byte write enables (SRAM_BW_[3:0]) to the SRAM. It latches the starting address signals (LA[9:2] for C mode and LAD[9:2] for J mode), and uses its built-in internal address counter to advance the addresses to the SRAM. The SRAM controller also generates the active low ready signal (READY#) to terminate normal PCI 9656 memory cycles and also generates the active low (BTERM#) input to the PCI 9656 to break the continuous burst memory cycle when its internal address counter reaches the final count (FFh).

The external Processor/Local Bus arbiter in the CPLD accepts the Processor/Local Bus request signals (LBR [1:0]) from Processor/Local Bus masters, if there are any, and the bus request from the PCI 9656 (LHOLD). It generates bus grant signals LBG [1:0] to the Processor/Local Bus masters and LHOLDA to the PCI 9656.

The chip select generator in the CPLD generates the SRAM chip select (SRAMCS#) and four additional active low chip selects for the Processor/Local Bus devices. The chip select signals are partially decoded from the upper four address lines (LA31-LA28) on the Processor/Local Bus. They can be re-programmed by altering the CPLD Verilog code.

2.7 Test Headers

The RDK board has six (6) 0.1", 2x10 logic analyzer headers (LAH1-LAH6) that follow the HP format and can be used for probing or prototype area extension. All PCI 9656 Processor/Local Bus signals, configuration and status signals are well arranged within these headers. Headers LAH1 and LAH2 contain Processor/Local Bus address signals. Headers LAH3 and LAH4 contain Processor/Local Bus data signals. Headers LAH5 and LAH6 contain Processor/Local Bus control and status signals. These headers do not provide any power source. Schematic page 6 provides the connector signal details.

2.8 PLX Option Module Connector

The PLX Option Module Connector (J3) assumes that the Processor/Local Bus is configured for 32-bit multiplexed address/data bus (J mode) operation. (See Section 2.12 for details on re-configuring the RDK hardware for J Mode operation.) It can be used for expansion and prototyping. Both/either a master and/or a slave device may be connected to this connector, which resides at Processor/Local Bus address range 1000 0000 – 1FFF_FFFFh. The external arbiter in the CPLD uses CS0# to select the POM module. Schematic page 5 provides the connector signal details.

2.9 Hardware Modules

2.9.1 RS-232 Interface

The RS-232 interface circuit combines a DB9 male connector (J2) with a Maxim RS-232 transceiver (U12). The transceiver chip can be hardware configured or software programmed as Data Terminal Equipment (DTE) or Data Circuit Equipment (DCE). See Table 2-4 for details.

Table 2-4. RS-232 Transceiver Configuration

DTE mode (default)	R44 (not installed)
	R45 (installed)
DCE mode	R44 (installed)
	R45 (not installed)

2.9.2 Debug and Status LEDs

There are five green LEDs (D1-D5) at the top edge of the RDK board – D5 is a power on indicator, and four are user-defined LEDs. The anode of each user-defined LED is connected to $3.3V_{CC}$ through a 150-ohm ¼ watt resistor. The cathode of each LED is connected to a prototyping pad for customer use. As long as an active low signal can sink 16 – 20 mA of current, it can drive the LEDs without changing the resistor value.

2.9.3 Reset Circuitry

The reset circuitry ships configured as a user-defined reset circuit for general power-on reset and manual reset by pressing the pushbutton (S1).

The reset circuitry can be re-configured to emulate the power management event request (PMEREQ#) from the Processor/Local Bus side to wake up the PCI system from the $D3_{cold}$ state. When the pushbutton (S1) is pressed, the reset circuitry asserts PMEREQ# to the PCI 9056. In response, the PCI 9056 will assert the PCI bus PME# signal to wake up the system from $D3_{cold}$ state. (Note: please view Erratum #11 which describes PME# generation in $D3_{cold}$. This erratum will affect the above functionality and should be taken into consideration in your product design).

Table 2-5 details the how to configure the RDK reset circuitry for user-defined reset and Power Management Event request generation.

Table 2-5. Reset Circuit Configuration

User defined reset circuit (default)	R41 (installed)
	R40, R43 (not installed)
Emulate PMEREQ# input	R40, R43 (installed)
	R41 (not installed)

2.9.4 Flash ROM Socket

A 32-pin PLCC socket (FP31) is provided on the RDK, which can be used to install a 3.3V, 512KBx8 Flash memory device. Its power and ground are pre-wired and it has pads available on the board for control signals and data/address lines.

2.10 Prototyping Area

The RDK board contains a large prototyping area with surface-mount footprints, BGA footprints, and a through-hole grid.

2.10.1 Surface Mount Footprints

The RDK board has thirty (30) surface mount footprints. See Table 2-6 for details.

These footprints will accommodate a wide variety of devices, including industry leading embedded microprocessors, DSPs, FPGAs, FIFOs, memory, I/O devices, etc.

2.10.2 BGA Footprints

This RDK has two (2) common pitch BGA footprints. See Table 2-7 for details.

BGA1 is a full matrix of 25x25 @ 1.0mm pitch holes with a plated hole size of 0.0165” diameter +/-0.001”. BGA2 is a full matrix of 26x26 @ 0.05” pitch holes with a plated hole size of 0.022” diameter +/-0.001”.

Note. These BGA footprints appear on the RDK board, but are not included in the schematics.

PLX recommends using Ironwood Electronics (www.ironwoodelectronics.com) BGA Land Sockets and/or Minigrid Sockets to convert from BGA to PGA, and prototype BGA chips on this RDK.

BGA1 Prototyping

1. Use only BGA Land Sockets from Ironwood Electronics.
2. Solder the BGA device on the top of the Land Socket and solder the Land Socket to the PC board.

BGA2 Prototyping

1. Use both the Minigrid Socket and the BGA Land Socket from Ironwood Electronics.
2. Solder the Minigrid Socket to the PC board.
3. Solder the BGA device to the Land Socket and plug the Land Socket to the Minigrid Socket.

Note: The size of each hole on BGA1 is 0.0165" in diameter. The holes are large enough to accept the 0.014" diameter Land Socket pins. They are too small to accept the 0.018" diameter Minigrid Socket pins.

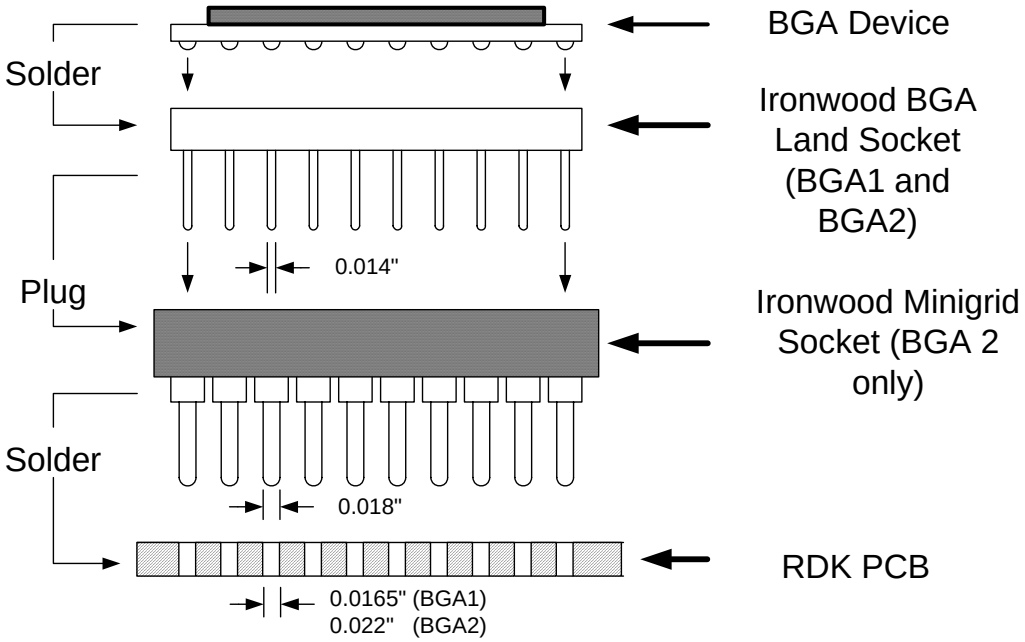


Figure 2-2. BGA Device Prototyping Diagram

Table 2-6. Thirty (30) Surface Mount Footprints

Package	Quantity	Pin Pitch	Examples of Applications
16-pin SOIC	2	0.05"	Discrete Logic
28-pin SOIC	2	0.05"	Discrete Logic
28-pin PLCC	3	0.05"	PALs
44-pin PLCC	1	0.05"	CPLDs
44-pin PQFP	2	0.8mm	CPLDs
48-pin SSOP	2	0.025"	Discrete Logic, data transceivers
54-pin TSOP	2	0.8mm	SDRAM, SRAM
68-pin PLCC	1	0.05"	CPLD, ADS-2104L
80-pin PQFP	2	0.5mm	PPC401GF
84-pin PLCC	1	0.05"	CPLDs, MIPS CPUs, PPC401GF
100-pin PQFP	2	0.5mm	CPLDs, TI 320/C541/LC541/LC543/LC546, ADSP-2186L
112-pin PQFP	1	0.65mm	SH7032/7034/7040
128-pin PQFP	1	0.4mm	LC542/545
144-pin PQFP	2	0.5mm	CPLDs, TI C542/KC542/LC548/LC549/VC549, SH7604, IDT RC32364
160-pin PQFP	1	0.65mm	FPGAs, PPC403GA, MCF5206e
176-pin PQFP	2	0.5mm	SH7410
208-pin PQFP	2	0.5mm	FPGAs, SH7707/7709/7750, ADSP 20165L
240-pin PQFP	1	0.5mm	FPGAs, ADSP 21061L/21062L

Table 2-7. Two BGA Footprints

Package	Quantity	Pin Pitch	Examples of Applications
BGA1 (25x25)	1	1.0mm	PPC403GC/GCX, TI TMS 320C6202
BGA2 (26x26)	1	0.05"	MPC801/821/823/850

2.11 Power Supply

The electronic devices on the RDK require 2.5V, 3.3V, and/or 5V DC power. A 3A LDO regulator (U1) is used to convert the 5 VDC to 3.3 VDC, and a 2A LDO regulator (U2) is used to convert the 5 VDC to 2.5 VDC power for the on board devices. As long as the output current from the voltage converter remains less than the maximum current outputs from both LDOs, the RDK board will function correctly.

2.12 RDK Mode Configuration

The RDK hardware's Processor/Local Bus is pre-configured for non-multiplexed data and address (C mode) Processor/Local Bus operation. It can be reconfigured for multiplexed data and address Processor/Local Bus operation (J mode). Several resistors configure the RDK hardware's Processor/Local Bus for C or J Mode. The specific resistors to install and remove for each mode are detailed in Table 2-8. ('X' means installed; no 'X' means removed.)

Table 2-8. RDK Board Mode Configuration

Resistors	Value	C Mode (Default)	J Mode
Mode Pins Configuration			
R4	1/10w, 10K ohm, 5%		X
R5	1/10w, 10K ohm, 5%		
R6	1/10w, 0 ohm, 5%	X	
R7	1/10w, 0 ohm, 5%	X	X
Data/Address Pins Configuration			
R46	1/10w, 10K ohm, 5%	X	
R47	1/10w, 10K ohm, 5%		X
R48	1/10w, 10K ohm, 5%	X	
R49	1/10w, 10K ohm, 5%		X
R50	1/10w, 10K ohm, 5%	X	
R51	1/10w, 10K ohm, 5%		X
R71	1/10w, 10K ohm, 5%		X
R79	1/10w, 10K ohm, 5%	X	
R93	1/10w, 10K ohm, 5%		X
R94	1/10w, 10K ohm, 5%	X	
R95	1/10w, 10K ohm, 5%		X
R96	1/10w, 10K ohm, 5%	X	
R97	1/10w, 10K ohm, 5%		X
R98	1/10w, 10K ohm, 5%	X	
R99	1/10w, 10K ohm, 5%		X
R100	1/10w, 10K ohm, 5%	X	
R101	1/10w, 10K ohm, 5%		X
R102	1/10w, 10K ohm, 5%	X	
R103	1/10w, 10K ohm, 5%		X
R104	1/10w, 10K ohm, 5%	X	
R105	1/10w, 10K ohm, 5%		X
R106	1/10w, 10K ohm, 5%	X	
R107	1/10w, 10K ohm, 5%		X
R108	1/10w, 10K ohm, 5%	X	

3. EXAMPLES OF TESTING THE ONBOARD 32KX32 SRAM WITH PLXMON

1) Single read/write from/to onboard SRAM

   a) At the lower command line window of PLXMon, type in the following commands to perform single 32bit, 16bit and 8bit memory read/write transfers from/to the onboard SRAM.

      dl s0 1

      <= read one 32-bit long word from address s0

      el s0 88888888

      <= write 32-bit data, 88888888h, to address s0

      dw s0 1

      <= read one 16-bit word from address s0

      ew s0 8888

      <= write 16-bit data, 8888h, to address s0

      db s0 1

      <= read a byte from address s0

      eb s0 88

      <= write 8-bit data, 88h, to address s0

2) DMA burst read/write from/to onboard SRAM:

   a) At the lower pane of PLXMon, type **Vars** to obtain the addresses for HBuf, the 60K-byte DMA scratch buffer located in the PC's main memory. For example, assume HBuf has a physical address starting at 01F80000h.

   b) Enter 8 long words of test data to the SRAM. For example,

      el s0 11111111

      el s0+4 22222222

      el s0+8 33333333

      el s0+c 44444444

      el s0+10 55555555

      el s0+14 66666666

      el s0+18 77777777

      el s0+1c 88888888

   c) Click the DMA button on PLXMon to open the DMA registers window.

   d) Configure DMA CH0 for burst transfer and the transfer direction from Local-to-PCI. The settings on DMA channel 0 would be similar to the following

      Mode (80h): 143

      PCI address (84h): **01F80000**

      Local address (88h): 00000000

      Transfer size (8ch): 100

      Descriptor pointer (90h):8

      Check the box for data transfer enable

   e) Click on the [Start Transfer] button to transfer data from the onboard SRAM to the DMA scratch buffer.

   f) Compare the data from step 'b' by typing the **dl HBuf** command.

   g) Change the contents of the DMA scratch buffer

      el HBuf 99999999

      el HBuf+4 88888888

      el HBuf+8 77777777

      el HBuf+c 66666666

      el HBuf+10 55555555

      el HBuf+14 44444444

      el HBuf +18 33333333

      el HBuf+1c 22222222

   h) Change the direction of the DMA transfer to PCI-to-Local for DMA CH0, by modifying the Descriptor Pointer (90h) value from 8 to 0.

   i) Click the [Start Transfer] button to perform a DMA transfer again

   j) Type in **dl s0** to compare the data from step 'g'.

4. CPLD VERILOG CODE

4.1 Verilog Code

```
//============================================================
//
//   4/12/2001
//
//   Synchronous SRAM controller for PLX PCI 9x56 mode C and J.
//   128K byte (32K x 32 bit) synchronous SRAM is used.
//   The memory map for the sync. SRAM is 0000_0000 - 0001_FFFFh.
//   A partial memory decode is used. The decode is only involved
//   address lines A31 to A28 (or A31-A29 and LD28 in J mode)
//
//   1/4/2002
//
//   changed the bterm# and ready# signal to tri-state if there is
//   no SRAM cycle.
//
//   10/22/2004
//
//   Changed two bufifo(…) statements after defining the internal
//   variables to call the Xilinx's BUFE macro.
//
//============================================================
`timescale 1ns/100ps

module sramctr9x56 ( clk,adsn,blastn,lwdrdn,lhold,lbr,lben,adds_in,adds_4msb,
                     readyn,btermn,sramcsn,sramoen,lholda,lbg,sram_adds,
                     sram_bwn,csn);

    input            clk,adsn,blastn,lwdrdn,lhold;
    input   [1:0]    lbr;
    input   [3:0]    lben;
    input   [9:2]    adds_in;
    input   [31:28]  adds_4msb;

    output           readyn,btermn,sramcsn,sramoen,lholda;
    output  [1:0]    lbg;
    output  [9:2]    sram_adds;
    output  [3:0]    sram_bwn;
    output  [3:0]    csn;

    reg     [9:2]    sram_adds;
    reg     [1:0]    lbg;
    reg              sramcsn,sramoen,lholda;
    tri              readyn,btermn;

    // internal veriables

    reg     [3:0]    a31_28;
    reg     [1:0]    state;
    reg              oer,oeb;

    BUFE tt1(.O(readyn),.E(!oer),.I(oer));
    BUFE tt2(.O(btermn),.E(!oeb),.I(oeb));
```

```
// chip selects
// Four uppermost address lines, A31-A28, are used to generate four
// chip select signals for the board. They are CS[3:0] with addresses
//
//  csn_0: 1000_0000h
//  csn_1: 2000_0000h
//  csn_2: 3000_0000h
//  csn_3: 4000_0000h


wire [3:0] csn = (adds_4msb == 4'b0001) ? 4'b1110:
                 (adds_4msb == 4'b0010) ? 4'b1101:
                 (adds_4msb == 4'b0011) ? 4'b1011:
                 (adds_4msb == 4'b0100) ? 4'b0111: 4'b1111;

// byte enable encode for SRAM write cycles

wire [3:0] sram_bwn =({lwdrdn,a31_28}=='b1_0000)
                    ? lben[3:0] : 4'b1111;

// store the upper address LA31 - LA28

always @ (posedge clk)

   if (!adsn & (adds_4msb==4'b0000))
       a31_28[3:0] <= adds_4msb[31:28];


// SRAM control state machine
parameter s0=2'b00, s1=2'b01, s2=2'b10, s3=2'b11;

always @ (posedge clk)

    casex (state)
        s0: begin
                sramoen <=1;
                oeb <='b1;
                if (!adsn && !adds_4msb)
                    begin
                        sram_adds[9:2] <= adds_in[9:2];
                        sramcsn <= 0;
                        if (lwdrdn)
                            oer <= 'b0;
                        else
                            oer <= 'b1;
                        state <= s1;
                    end
                else
                    begin
                        oer <= 'b1;
                        sramcsn <= 1;
                        state <= s0;
                    end

            end
```

```
s1: if (lwdrdn && (!blastn))
        begin
            sram_adds[9:2] <=sram_adds[9:2]+1;
            sramoen <=1;
            sramcsn <=1;
            oer <='b1;
            oeb <='b1;
            state <= s0;
        end
    else    if (lwdrdn && blastn)
                begin
                    if (sram_adds[9:2]== 'hfe)
                        begin
                            oeb <='b0;
                            sram_adds[9:2] <= sram_adds[9:2]+1;
                            state <= s3;
                        end
                    else
                        begin
                            sram_adds[9:2] <= sram_adds[9:2]+1;
                            sramoen <=1;
                            sramcsn <=0;
                            oer <='b0;
                            oeb <='b1;
                            state <=s1;
                        end
                end
            else
                begin
                    sram_adds[9:2] <=sram_adds[9:2]+1;
                    sramoen <=0;
                    sramcsn <=0;
                    oer <='b0;
                    oeb <='b1;
                    state <= s2;
                end
```

```
            s2: if ((!lwdrdn) && (!blastn))
                    begin
                        sramoen <=1;
                        sramcsn <=1;
                        oer <='b1;
                        oeb <='b1;
                        state <=s0;
                    end
                else
                    begin
                       if (sram_adds[9:2]=='hff)
                           begin
                               oeb <='b0;
                               sram_adds[9:2] <= sram_adds[9:2]+1;
                               state <=s3;
                           end
                       else
                           begin
                               sram_adds[9:2] <= sram_adds[9:2]+1;
                               sramoen <=0;
                               sramcsn <=0;
                               oer <='b0;
                               oeb <='b1;
                               state <=s2;
                           end
                    end

            s3: begin
                    sramcsn <=1;
                    oer <='b1;
                    oeb <='b1;
                    state <=s0;
                end

            default: state <=s0;
        endcase

    always @(posedge clk)

        begin
            if (lhold)
                lholda <= lhold;
            else
                lholda <= 0;

            if (!lhold && lbr[1])
                lbg[1] <= lbr[1];
            else
                lbg[1] <= 0;

            if (!lhold && !lbr[1] && lbr[0])
                lbg[0] <= lbr[0];
            else
                lbg[0] <= 0;
        end

endmodule
```

5. BILL OF MATERIALS / SCHEMATICS

The following pages list the bill of materials and the schematics for the PCI 9656RDK-LITE circuit board.

The PCI 9656 is a 272-pin 1.27mm ball pitch PBGA package. The PCI 9656 signal names used in the schematics are the C mode signal names, except for the POM connector, which uses J mode signal names.

Table 5-1. Bill of Materials

Item No.	Qty.	Man.	Manufacturer's Part Number	Description	Package Type	Source	Component Designator(s)
SURFACE MOUNT COMPONENTS							
1	1	Linear Technology	LT1587CM-3.3	IC, 3A 5V to 3.3V LDO regulator	SMT, M package, 3-lead plastic DD PAK	Marshall	U1
2	1	Semtech	EZ1117ACST-2.5	IC, 1A 5V to 2.5V LDO regulator	SOT-223	Electec Sales, 408-764-0600, All America 1800-573-2727	U2
3	1	TI	TPS2103DBVT	IC, Vaux power-distribution switch	SMT, 5-pin DVB, R-PDSO-G5	Avnet	U3
4	1	Semtech	SC2982CSK-2.5	IC, 50mA 2.5Voutput LDO	SMT, SOT-23-5	Electec Sales, 408-764-0600, All America 1800-573-2727	U4
5	1	Fairchild Semi	FDN335N	IC, N-channel 2.5V MOSFET	SSOT-3, SMT	Arrow Electronics	U5
6	1	PLX	PCI 9656-BA66BI (or PCI 9656-BA66BES)	IC, PCI I/O accelerator, 3.3V	PBGA-272pin	PLX	U6
7	1	Cypress	CY2305SC-1	IC, zero delay buffer, 3.3V, 250ps skew	8-pin 150-mil SOIC	FAI	U9
8	1	Xilinx	XC9572XL-5TQ100C	IC, CPLD, 72 userIO pins, 5ns delay, 3.3V	100-pin TQFP	Avnet	U13
9	1	Maxim	MAX214CWI	IC, programmable DTE/DCE RS232 transceiver, 5V	28-pin wide SOP	Digi-Key	U12
10	1	Maxim	MAX6306UK30D3-T	IC, Reset Controller, 200ms reset time	SOT23-5	Maxim distribution 1800-835-8769	U11
11	1	Samsung	K7B403625M-QC75000	IC, 4Mb Syncburst SRAM, 128Kx36, 7.5ns access time	100-pin TQFP	Marshall	U14
13	5	Hewlett Packard	HSMG-C650	LED, green, SMT	SMT, 1206	Digi-key	D1-D5
14	1	Kycon	K20HT-E9P-N	Connector, DB9, plug	SMT	Digi-key	J2
15	1	AMP	1-104655-1	Header, two row 100-pin, 50 mil pitch	SMT	Electrosonic	J3
16	1	Samtec	TSM-106-01-T-SV	Header, 6-pin single row, 0.1" SMT unshrouded	SMT	FAI	JP1
17	1	Samtec	TSM-109-01-T-SV	Terminal Strip, 1x9, 0.1" oc, PCB mounted	SMT	FAI	JP2
18	6	Samtec	TSM-110-01-T-DV	Terminal strip, 2x10, 0.1"oc, PCB mounted	SMT	FAI	LAH1 - LAH6

Item No.	Qty.	Man.	Manufacturer's Part Number	Description	Package Type	Source	Component Designator(s)
19	1	Samtec	ICF-314-T-O	Socket, 14-pin DIP, 300mil	SMT, 14-pin DIP	FAI	U8
20	1	Samtec	ICF-308-T-O	Socket, 8-pin DIP, 300 mil, for serial EEPROM	SMT, 8-pin DIP	FAI	U10
21	1	AMP	822273-1	Socket, 32-pin PLCC	SMT, 32-pin PLCC	Digi-key	FP31
22	1	Omron	B3S1002	Switch, Push Button	SMT,	Digi-key	S1
23	1	Steward	L10805E400R	Ferrite chip, 500mA	SMT, 0805	Digi-Key	L1
24	20	CTS	742-08-3-103-J-BK	Res. Network, 10K, 5%, 4R, isolated	SMT,Ccase	Digi-Key	RN1-RN7, RN9-RN21
25	27	Panasonic	ERJ-6GEYJ0R0V	Res. 1/10W, zero ohm, 5%	SMT, 0805	Digi-Key	R6, R7, R25-R31, R38, R41, R45, R46, R48, R50, R86, R94, R96, R98, R100, R102, R104, R106, R108, R112, R113, R115
26	4	Panasonic	ERJ-6GEYJ220V	Res. 1/10W, 22 ohm, 5%	SMT, 0805	Digi-Key	R12, R14-R16
27	1	Panasonic	ERJ-6GEYJ330V	Res. 1/10W, 33 ohm, 5%	SMT, 0805	Digi-Key	R13
28	5	Panasonic	ERJ-6GEYJ151V	Res. 1/10W, 150 ohm, 5%	SMT, 0805	Digi-Key	R32-R36
29	11	Panasonic	ERJ-6GEYJ102V	Res. 1/10W, 1K, 5%	SMT, 0805	Digi-Key	R58-R66,R116-R117
30	1	Panasonic	ERJ-6GEYJ392V	Res. 1/10W, 3.9K, 5%	SMT, 0805	Digi-key	R21
32	27	Panasonic	ERJ-6GEYJ103V	Res. 1/10W, 10K, 5%	SMT, 0805	Digi-Key	R1, R8, R11, R17-R20, R23, R24, R42, R54-R57, R67-R70, R75-R79, R81, R82, R84, R90
35	1	Panasonic	ERJ-6ENF5112B	Res. 1/10W, 51.1 K ohm, 1%	SMT, 0805	Digi-Key	R37
36	2	Panasonic	ERJ-6GEYJ244V	Res. 1/10W, 240K ohm, 5%	SMT, 0805	Digi-Key	R2-R3
37	7	Kemet	C0805C473M5UAC	Cap. Ceramic, 0.047uF, 50V, 20%	SMT, 0805	Electrosonic	C9-C15
38	1	Kemet	C0603C103M5UAC	Cap. Ceramic, 0.01uF, 50V, 20%	SMT, 0603	Electrosonic	C65
39	30	Kemet	C0805C103M5UAC	Cap. Ceramic, 0.01uF, 50V, 20%	SMT, 0805	Electrosonic	C4, C8, C16-C29, C45-C48, C55-C60, C69-C71, C73
40	18	Kemet	C0805C104M5UAC	Cap. Ceramic, 0.1uF, 50V, 20%	SMT, 0805	Electrosonic	C2, C6, C30-C31, C33, C41-C44, C49-C54, C66-C68
41	5	Kemet	ECJ-3YB1C05K	Cap. Ceramic, 1uF, 16V, 10%	SMT, 1206	Digi-Key	C34-C38
42	2	Kemet	T491B105M025AS	Cap. Tantalum, 1uF, 25V, Bcase	SMT, B case	Electrosonic	C39-C40
43	9	Panasonic	ECS-T1DC106R	Cap. Tantalum, 10uF, 20V, Ccase	SMT, C case	Newark	C1, C3, C5, C7, C32, C61-C64

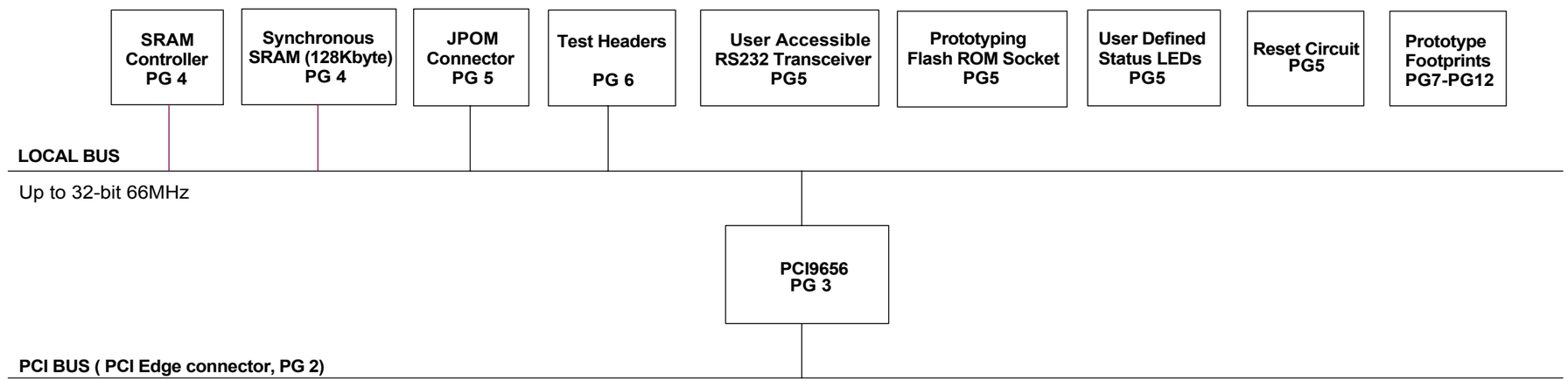
Item No.	Qty.	Man.	Manufacturer's Part Number	Description	Package Type	Source	Component Designator(s)
MANUALLY INSERTED COMPONENTS							
44	1	Ecliptek	EP1345HSPD-66.000M	OSC, 66 MHz clock oscillator, 3.3V, 50ppm, 40-60% duty cycle	8-pin half size DIP	Ecliptek	U7
45	1	Microchip	93LC56B/P	IC, 2Kb(x16) serial EEPROM, 2.5-6V, 2 MHz	8-pin DIP	Microchip online	U10
MISCELLANEOUS COMPONENTS							
46	1	Velostat	2100R/7X15	7" x 15" anti-static bag		FAI	BAG1
47	2		492-100	Phillips, 4-40, 1/4", PH screw (for PCB bracket)		Spaenaur	SCREW1 SCREW2
48	1	PLX	90-0017-400-A	9656RDK-LITE PCB Rev 400			
49	2	Kycon	JS-1000	Screw, Hex, Jack, 4-40		Kycon	
50	1	Keystone	CB-1095-PLX	PCI Bracket, with DB9 connector cut out		Keystone	
PARTS THAT SHOULD *NOT* BE ASSEMBLED							
12	0	Fairchild Semi	NC7WZ17P6	IC, dual buffer with schmitt trigger inputs, 3.3V	SMT, 6-lead SC70, EIAJ SC88, 1.25mm wide	Arrow Electronics	U15
24	0	CTS	742-08-3-103-J-BK	Res. Network, 10K, 5%, 4R, isolated	SMT, Ccase	Digi-Key	RN22-RN24
25	0	Panasonic	ERJ-6GEYJ0R0V	Res. 1/10W, zero ohm, 5%	SMT, 0805	Digi-Key	R39, R43, R47, R49, R51-R53, R80, R93, R95, R97, R99, R101, R103, R105, R107, R109-R111
29	0	Panasonic	ERJ-6GEYJ102V	Res. 1/10W, 1K, 5%	SMT, 0805	Digi-Key	R22,R91
32	0	Panasonic	ERJ-6GEYJ103V	Res. 1/10W, 10K, 5%	SMT, 0805	Digi-Key	R4-R5, R9, R44, R71-R74, R85, R92
34	0	Panasonic	ERJ-6GEYJ303V	Res. 1/10W, 30K 5%	SMT, 0805	Digi-key	R10
36	0	Panasonic	ERJ-6GEYJ244V	Res. 1/10W, 240K ohm, 5%	SMT, 0805	Digi-Key	R40
41	0	Kemet	ECJ-3YB1C05K	Cap. ceramic, 1uF, 16V, 10%	SMT, 1206	Digi-Key	C72
51	0	AMP	520251-4	Modular jack assembly, 8 position	RJ45, PCB mounted	Digi-Key	J4
52	0	Molex	87531-0001	USB receptacle, 4 position, type A	PCB mounted	Digi-Key	J5
11	0	Micron	MT58L32L32FT-7.5	IC, 1Mb syncburst SRAM, 32Kx32, 7.5ns	100-pin TQFP	Marshall	U14
SECOND SOURCE							
2	1	National	LM1117MPX-2.5	IC, .8A 5V to 2.5V LDO regulator	SMT, SOT-223	Digikey	U2
4	1	National	LP2982IM5-2.5	IC, 50mA 2.5Vouput LDO	SMT, SOT-23-5	Digikey	U4

PLX Part #: 91-0017-017-A

REVISION HISTORY

REVISION NUMBER	DATE	NOTE
000	10/5/2001	Released to production
100	5/6/2002	Modified IDDQEN# circuit; changed R92 to 10K, pull-up to 2,5V, removed LA28 pull-down R91(10K)
200	7/2/2002	swapped sourc and drain of n-channel MOSFET (U5) and removed R83 pull-up.
201	8/2/2002	connected pin6 of RN20 to ground
202	11/20/2002	Modified notes in schematic#4 and #5
203	3/29/2004	Added R91, R116 and R117 to U14.

PCI 9656RDK-LITE BLOCK DIAGRAM



PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title: **Electrical Block Diagram**

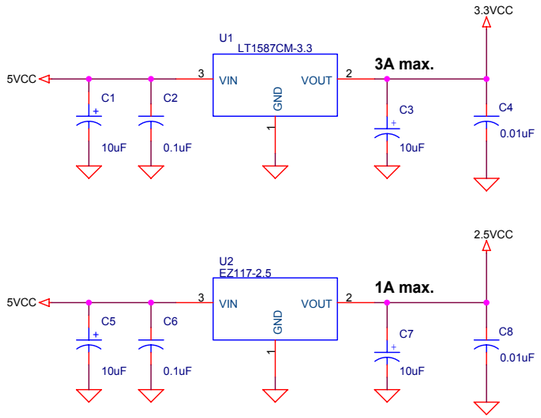
Size	Document Number	Rev
Custom	91-0017-200-A	203

Date: Monday, March 29, 2004 Sheet 1 of 13

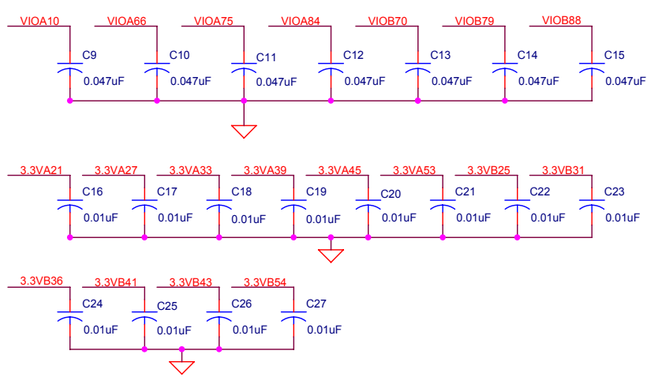
64-bit PCI Card Edge Connector

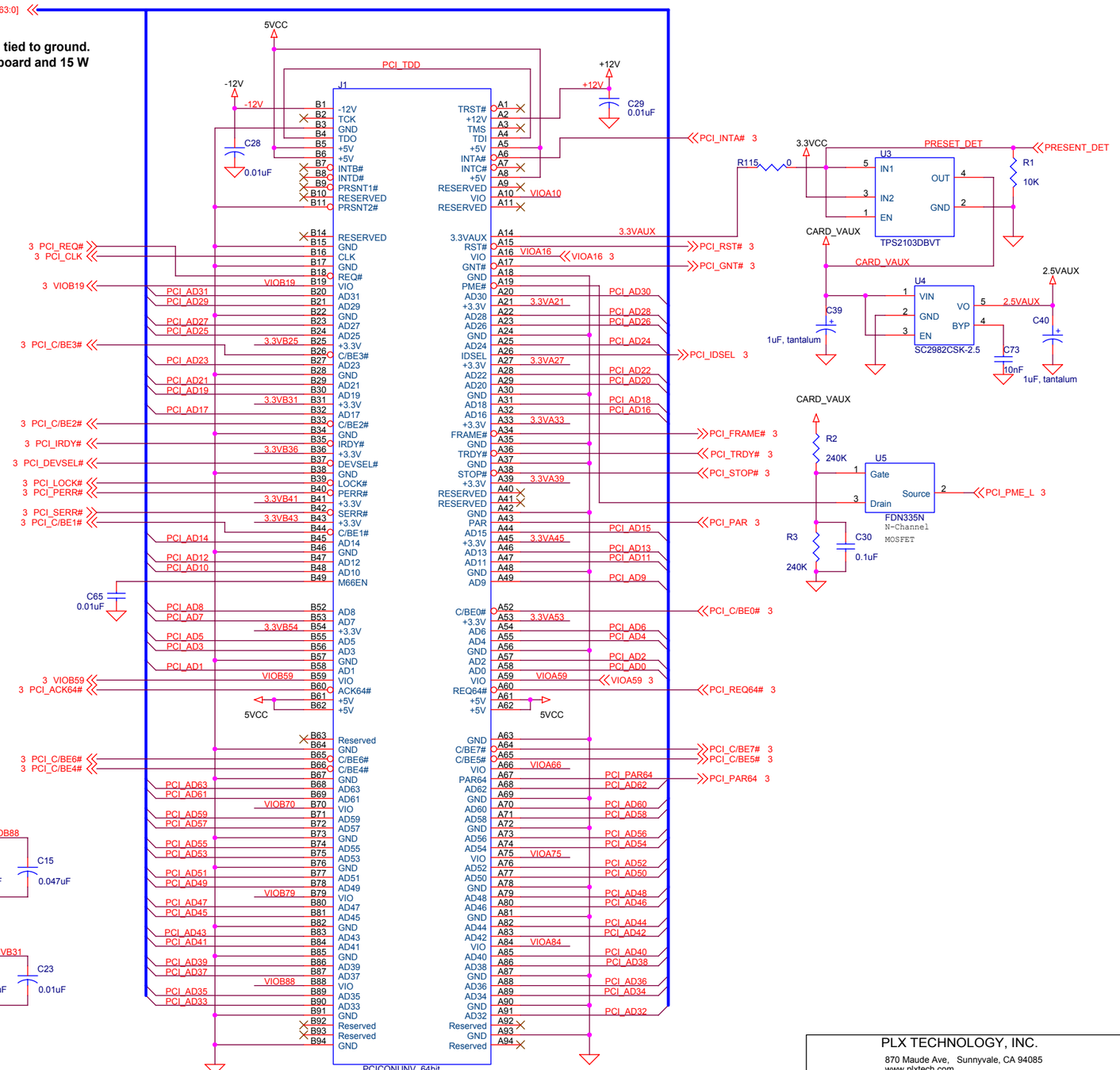
Note: PRSNT1# is open and PRSNT2# is tied to ground. That indicat the presence of expansion board and 15 W maximum in the power level.

DC Voltage Conversion



Decoupling Capacitors





PLX TECHNOLOGY, INC.	
870 Maude Ave, Sunnyvale, CA 94085	
www.plxtech.com	
Title	64-bit PCI Card Edge Connector
Size: Custom	Document Number: 91-0017-200-A
Rev: 203	
Date: Friday, December 30, 2005	Sheet 2 of 13

PLX PCI 9656

C & J Mode

PCI Signals

U6

2 PCI_AD[63:0]

AD[63:0]

4,5,6 LD[31:0]

4,5,6 LA[31:2]

LD0/LAD0 … LD31/LAD31

LA31/DT_R# … LA2

4,5,6 LBE0# … LBE3#

LBE0# … LBE3#

LCLK

MODE1, MODE0

IDDQEN#

HOSTEN#

CCS#

TCK, TMS, TDI, TRST#, TDO

2.5VAUX

CARD_VAUX

PRESENT_DET

PCI_C/BE0# … PCI_C/BE7#

PCI_FRAME#, PCI_IRDY#, PCI_TRDY#, PCI_STOP#, PCI_DEVSEL#, PCI_IDSEL, PCI_PERR#, PCI_SERR#, PCI_LOCK#, PCI_PAR, PCI_PAR64

PCI_GNT# 2

REQ1# … REQ6#

PCI_REQ64#, PCI_ACK64#

PCI_REQ# 2

GNT1# … GNT6#

PCI_INTA#, PCI_CLK, PCI_RST#, PCI_PME_L

64EN#, BD_SEL#, CPCISW, ENUM#, LEDon#

PMEREQ# 5,6

DP0 … DP3 6

ADS# 4,5,6

BLAST# 4,5,6

LW/R# 4,5,6

READY# 4,5,6

WAIT# 5,6

LHOLD 4,6

LHOLDA 4,6

LINT# 5,6

LINTo# 5,6

LRESET# 5,6

USERi/LLOCKi# 5,6

LSERR# 6

BIGEND# 6

BREQi 5,6

BREQo 5,6

BTERM# 4,5,6

DMPAF/EOT# 5,6

USERo/LLOCKo# 5,6

DREQ0# … DREQ1# 5,6

DACK0# … DACK1# 5,6

EECS, EESK, EEDI/DO

93CS56L or 66L(8DIP-Socket)

PCI9656-PBGA272

VIOA16, VIOB19, VIOA59, VIOB59

3.3VCC, 2.5VCC, 2.5VAUX, CARD_VAUX

R79 10K, R71 10K

R71should not be installed by default

R92 10K, R86 0, R10, C72 30K, 1uF

U15 NC7WZ17

For revision AD silicon: install R92 R10, C72, and U15, remove R86.
For revision BA silicon: install R86, removel R92, R10, C72, and U15.

R4 10K, R5 10K, R6 0, R7 0

R8 10K, R9 10K, R11 10K

JP1 JTAG Port

R78 10K

R4 and R5 should not be installed by default.

	MODE0	MODE1
M	1	1
C	0	0
J	1	0

R9 is used to enable CCS# and should not be installed by default.

R20 10K

R21 3.9K, R22 1K

R22 should not be installed by default

U10 93CS56L or 66L(8DIP-Socket)

R23 10K, R24 10K, C33 0.1uF

C66–C71: 0.1uF, 0.1uF, 0.1uF, 0.01uF, 0.01uF, 0.01uF

C41–C48: 0.1uF, 0.1uF, 0.1uF, 0.1uF, 0.01uF, 0.01uF, 0.01uF, 0.01uF

RN1 LA2–LA5 · RN2 LA6–LA9 · RN3 LA10–LA13 · RN4 LA14–LA17 · RN5 LA18–LA21 · RN6 LA22–LA25 · RN7 LA26–LA31 · RN9 LD0–LD3 · RN10 LD4–LD7 · RN11 LD8–LD11 · RN12 LD12–LD15 · RN13 LD16–LD19 · RN14 LD20–LD23 · RN15 LD24–LD27 · RN16 LD28–LD31 · RN17 DP0–DP3 · RN18 ADS#, BLAST#, READY#, WAIT# · RN19 LRESET#, BTERM#, LBE0#, LBE1# · RN20 LBE2#, LBE3#, BREQo, DREQ0# · RN21 LINTi#, LSERR#, LW/R#, USERi/LLOCKi# · RN22 REQ5#, GNT5#, REQ6#, GNT6# · RN23 REQ1#, GNT1#, REQ2#, GNT2# · RN24 REQ3#, GNT3#, REQ4#, GNT4#

All: 742-08-3-103-J-XX

Clock Circuit

U7 osc_halfsize, U8 66MHz OSC (full size), option

L1 Ferrite 500mA, C31 0.1uF, C32 10uF

OSC_CLK

U9 CY2305

R12 22, R13 33, R14 22, R15 22, R16 22

CLK_66MHZ 4, SRAM_CLK 4, POM_CLK 5, P1, LCLOCK 6

R72 10K, R73 10K, R74 10K, R84 10K, R90 10K, R75 10K, R76 10K, R77 10K, R85 10K

R72- R74, and R85 should not be installed by default.

PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

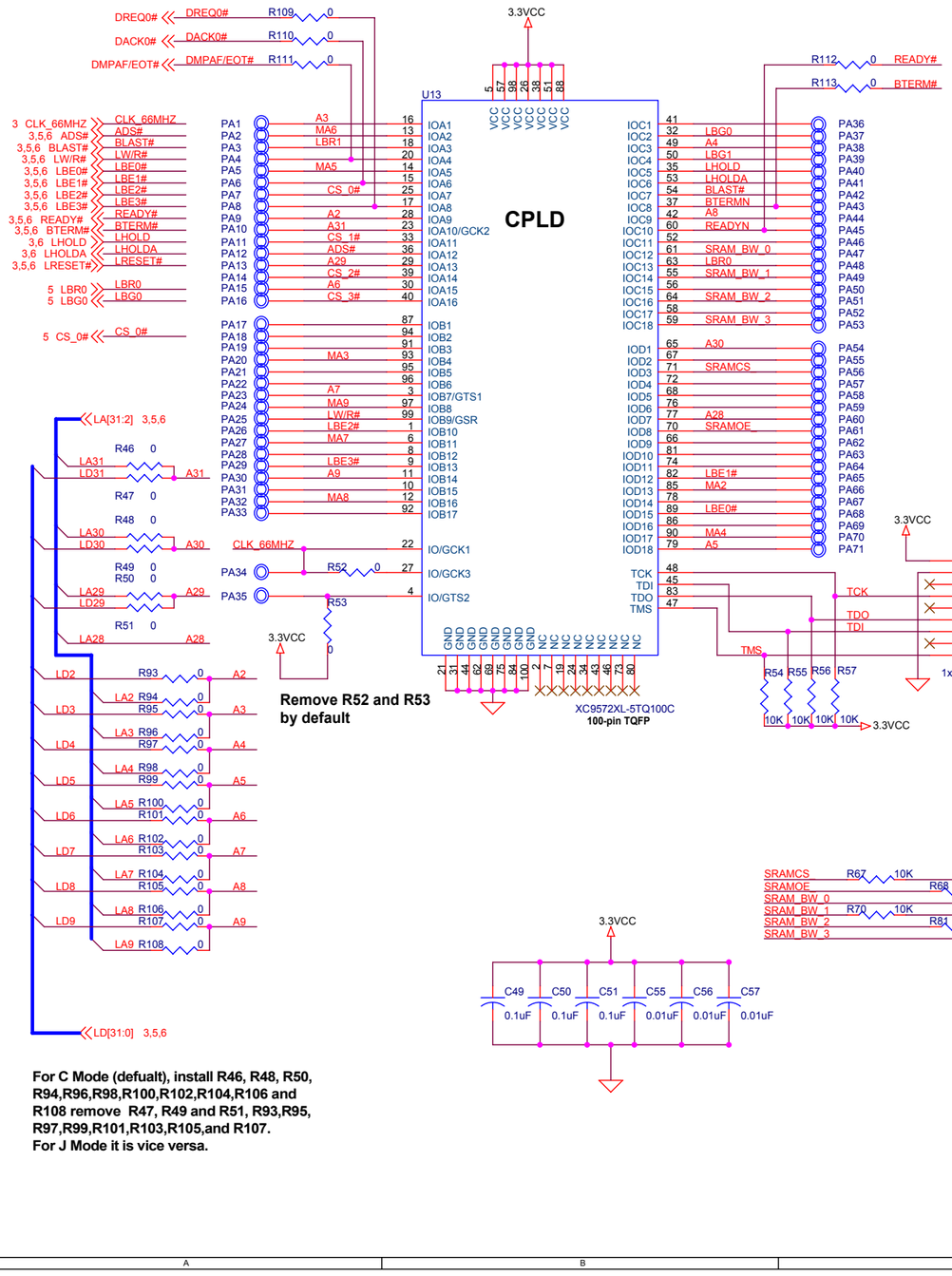
Title: PCI9656 PCI I/O Accelerator

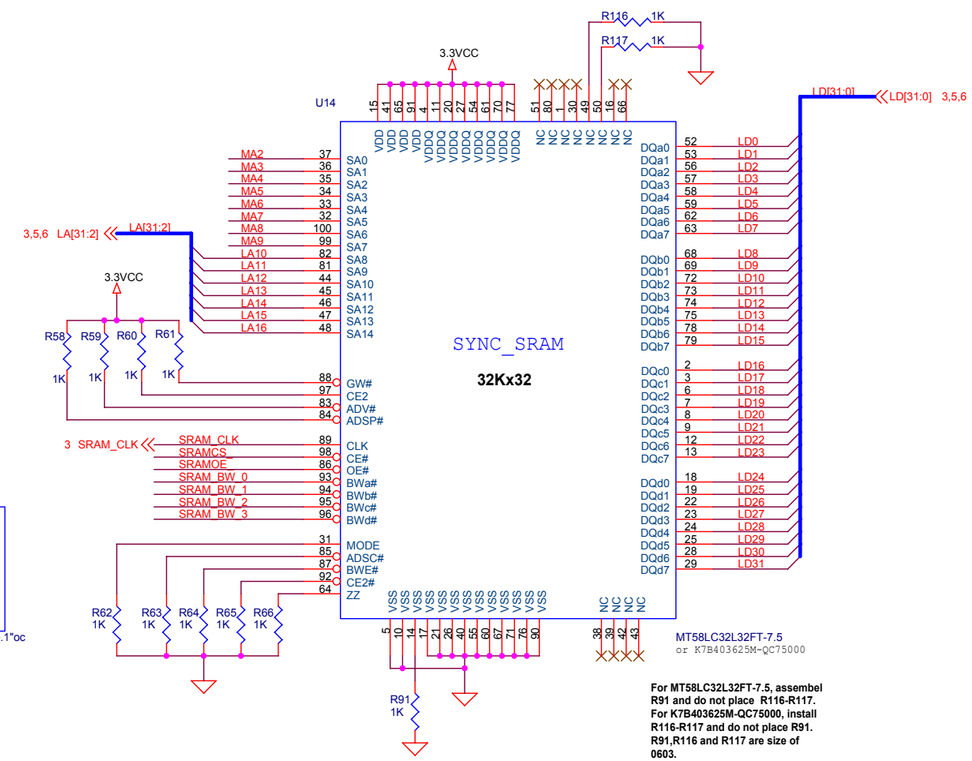
Size: Custom | Document Number: 91-0017-200-A | Rev: 203

Date: Friday, December 30, 2005 | Sheet 3 of 13

Synchronous SRAM and Controller Circuit

R109 to R111 should not be installed by default





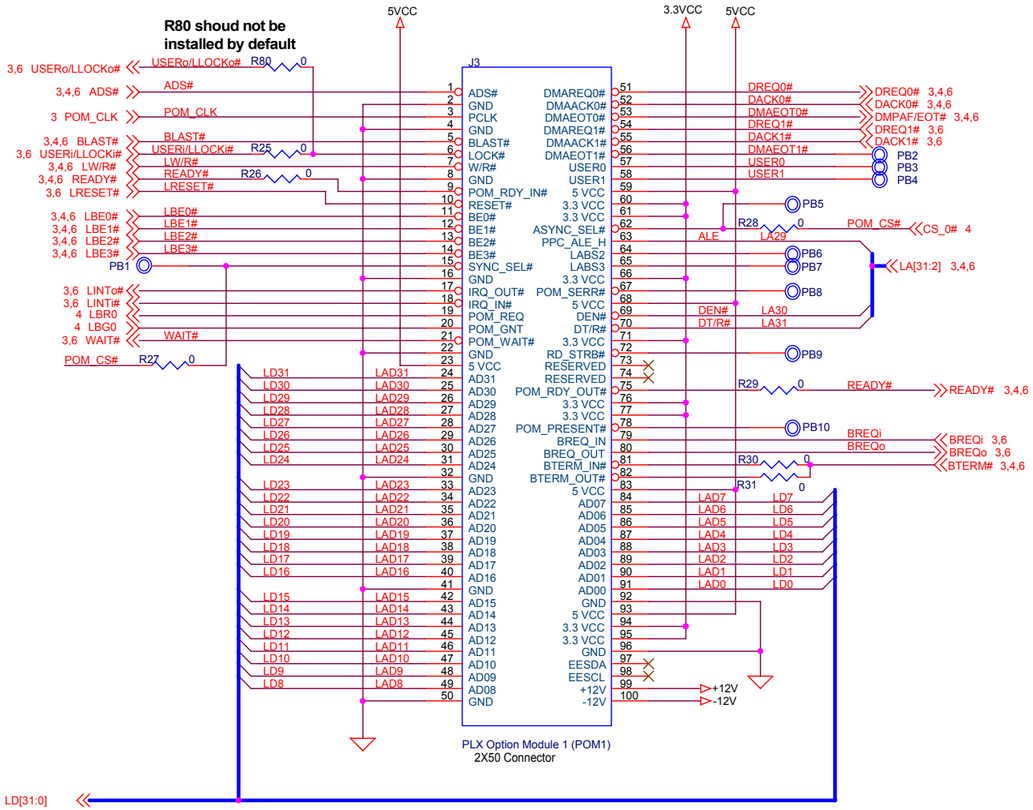
PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title: **SRAM, CPLD, Serial Port, ROM Socket and LEDs**

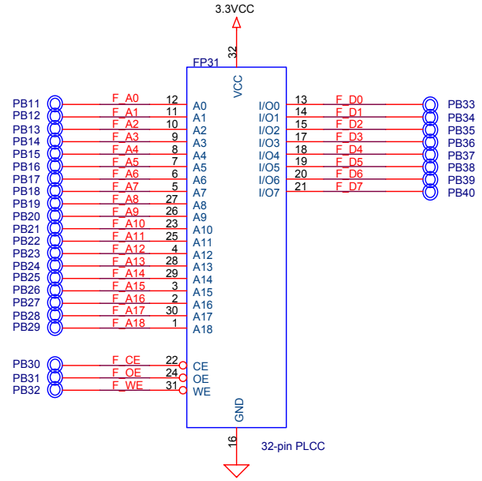
Size	Document Number	Rev
Custom	91-0017-200-A	203

Date: Friday, December 30, 2005 Sheet 4 of 13

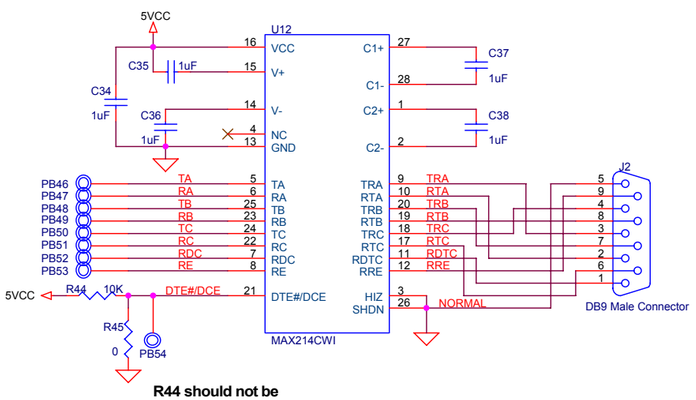
PLX Option Module Connector



Prototyping Flash ROM Socket

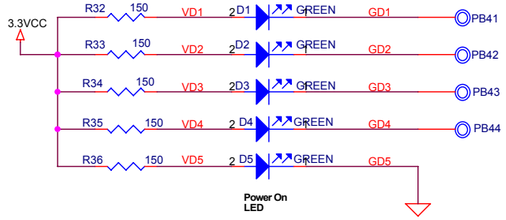


User Programmable DTE/DCE RS-232 Transceiver

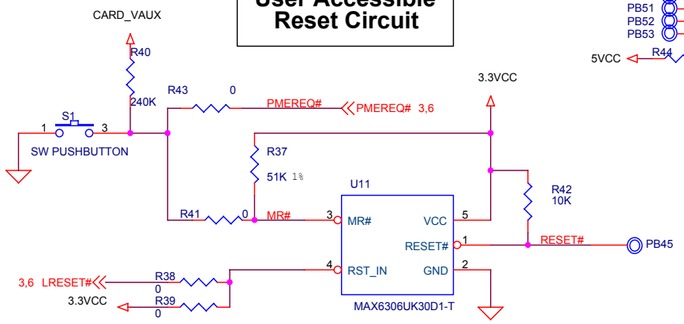


R44 should not be installed by defualt.

User Defined Status LEDs



User Accessible Reset Circuit



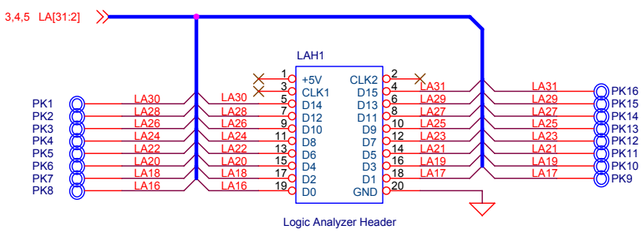
Install R41, remove R40, R43 and R39 by default.

PLX TECHNOLOGY, INC.			
870 Maude Ave, Sunnyvale, CA 94085			
www.plxtech.com			
Title: PLX Option Module Connector			
Size: Custom	Document Number: 91-0017-200-A		Rev: 203
Date: Monday, March 29, 2004	Sheet 5 of 13		

Test Headers

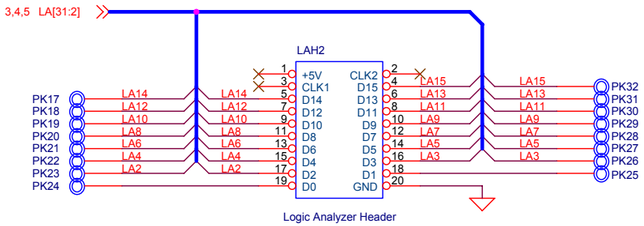
Note: they are designed to hook up directly to HP logic analyzer termination adapter 01650-63203.

Local Address Bus -Upper Half



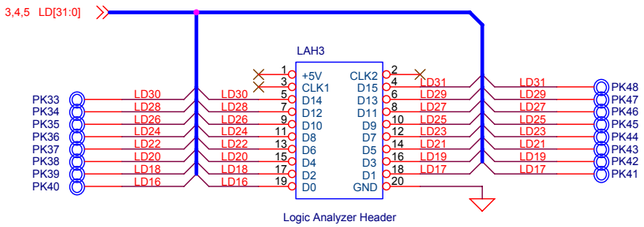
19: LA16
18: LA17
17: LA18
16: LA19
15: LA20
14: LA21
13: LA22
12: LA23
11: LA24
10: LA25
9: LA26
8: LA27
7: LA28
6: LA29
5: LA30
4: LA31

Local Address Bus - Lower Half



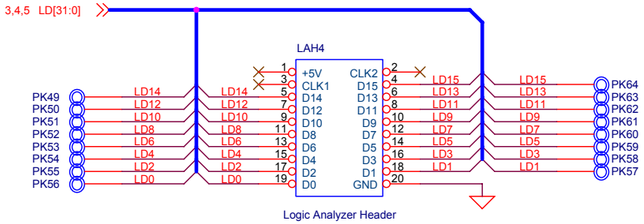
19: Unused
18: Unused
17: LA2
16: LA3
15: LA4
14: LA5
13: LA6
12: LA7
11: LA8
10: LA9
9: LA10
8: LA11
7: LA12
6: LA13
5: LA14
4: LA15

Local Data Bus - Upper Half



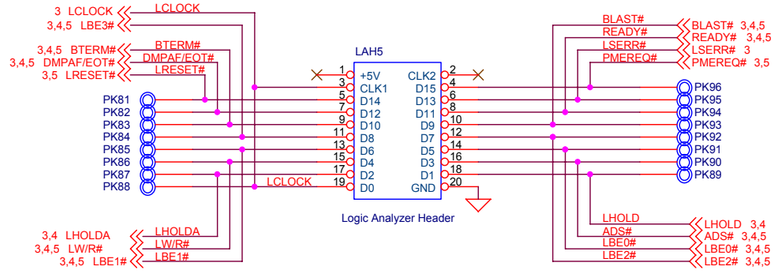
19: LD16
18: LD17
17: LD18
16: LD19
15: LD20
14: LD21
13: LD22
12: LD23
11: LD24
10: LD25
9: LD26
8: LD27
7: LD28
6: LD29
5: LD30
4: LD31

Local Data Bus - Lower Half



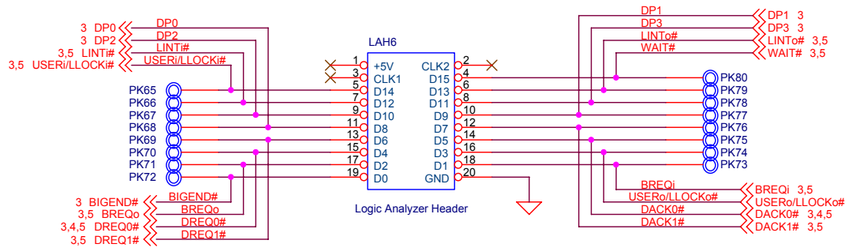
19: LD0
18: LD1
17: LD2
16: LD3
15: LD4
14: LD5
13: LD6
12: LD7
11: LD8
10: LD9
9: LD10
8: LD11
7: LD12
6: LD13
5: LD14
4: LD15

Control Signals in Local Bus (A)



19: LCLOCK
18: LHOLD
17: LHOLDA
16: ADS#
15: LW/R#
14: LBE0#
13: LBE1#
12: LBE2#
11: LBE3#
10: BLAST#
9: BTERM#
8: READY#
7: DMPAF/EOT#
6: LSERR#
5: LRESET#
4: PMEREQ#
3: LCLOCK

Control Signals in Local Bus (B)



19: BIGEND#
18: BREQi
17: BREQo
16: USERo/LLOCKo#
15: DREQ0#
14: DACK0#
13: DREQ1#
12: DACK1#
11: DP0
10: DP1
9: DP2
8: DP3
7: LINTi#
6: LINTo#
5: USERi/LLOCKi#
4: WAIT#

PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title: **Logic Analyzer Test Headers**

Size	Document Number	Rev
Custom	91-0017-200-A	203

Date: Monday, March 29, 2004 Sheet 6 of 13

Prototyping Footprint A

Note: Place four PLCC devices co-incident on the component side of the board; that is, they share common pins and the 28 fits inside the 44 which fits inside the 68 which fits inside the 84.

FP4 — 28 Pin PLCC, 0.05" pitch

FP3 — 44 Pin PLCC, 0.05" pitch

FP2 — 68 Pin PLCC, 0.05" pitch

FP1 — 84 Pin PLCC, 0.05" pitch

FP5 — 44 Pin TQFP, 0.8mm pitch

Place FP5 on the component side

Place FP6 on the solder side under FP5

FP6 — 28 Pin PLCC, 0.05" pitch

Place FP7 on the solder side under FP8

FP7 — 28 Pin PLCC, 0.05" pitch

FP8 — 44 Pin TQFP, 0.8mm pitch

Place FP8 on the component side

TB3 — HEADER 30

TB4 — HEADER 15

TB2 — HEADER 30

TB5 — HEADER 15

TB1 — HEADER 30

3.3VCC

5VCC

FP11 — 28-pin SOIC, 0.05" pitch

FP12 — 28-pin SOIC, 0.05" pitch

FP13 — 48-pin SSOP, 0.025" pitch

FP14 — 48-pin SSOP, 0.025" pitch

FP9 — 16-pin SOIC, 0.05" pitch

FP10 — 16-pin SOIC, 0.05" pitch

Place FP9-FP14 on the component side

PCI1:841

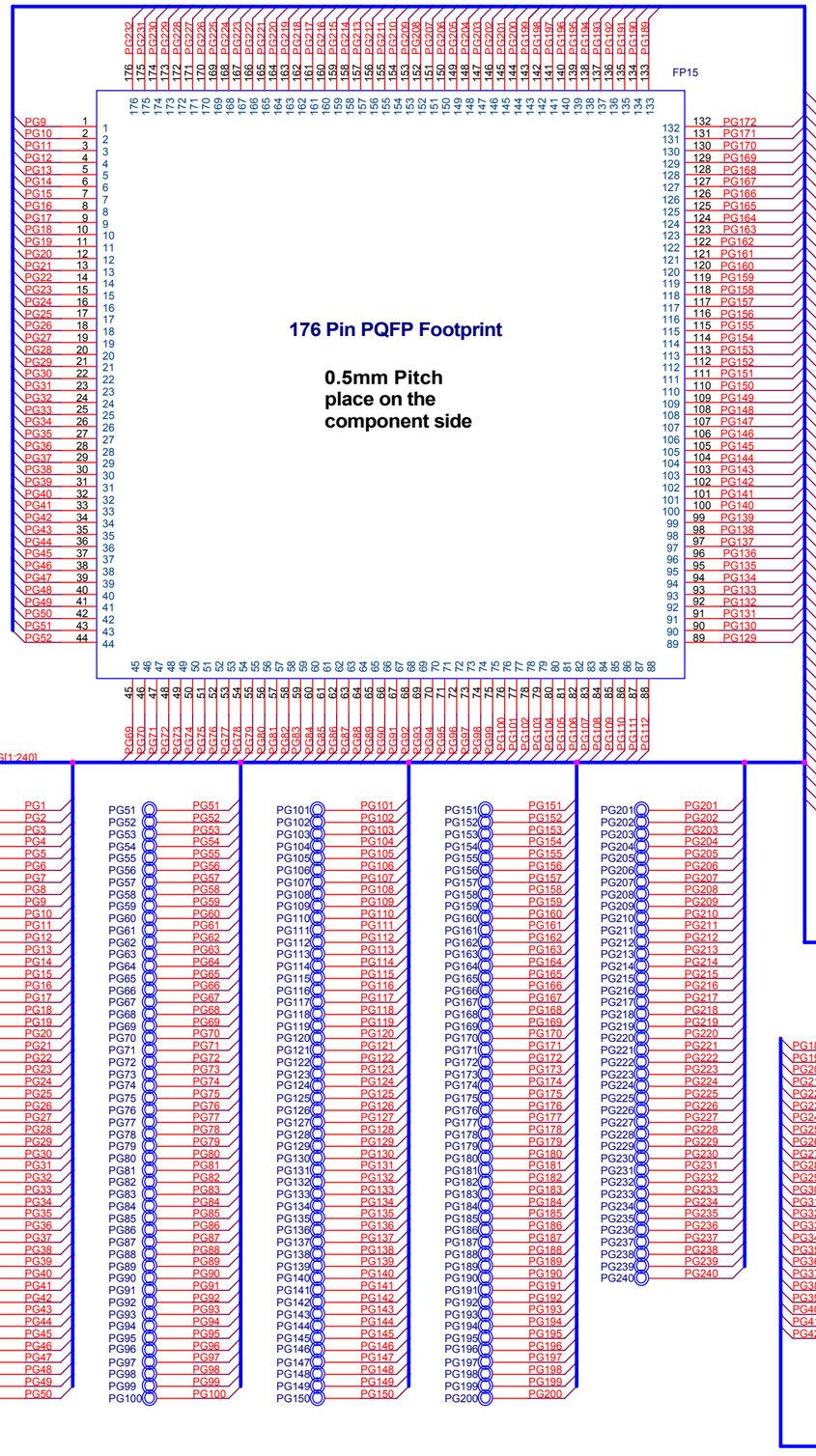
PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

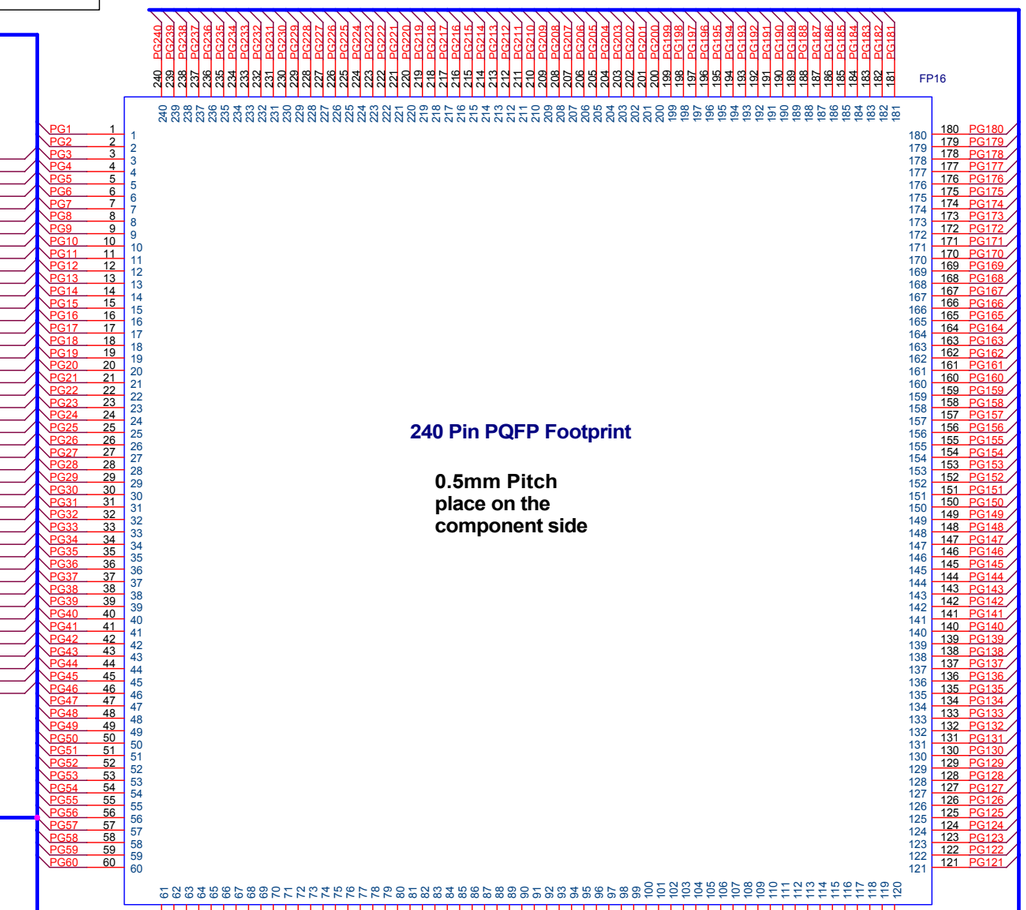
Title: **Prototyping Footprint A**

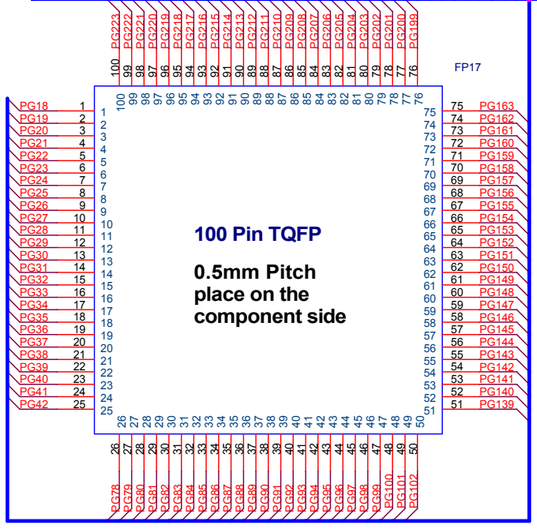
Size: Custom | Document Number: 91-0017-200-A | Rev: 203

Date: Monday, March 29, 2004 | Sheet 7 of 13

Prototyping Footprint B







9 PG[1:240]

PG[1:240]

Note: three QFP footprints are placed on the component side of the PCB. They are arranged as FP17 inside of FP15 and FP15 inside of FP16. All 240 holes for prototyping are located outside of 240-pin PQFP footprint.

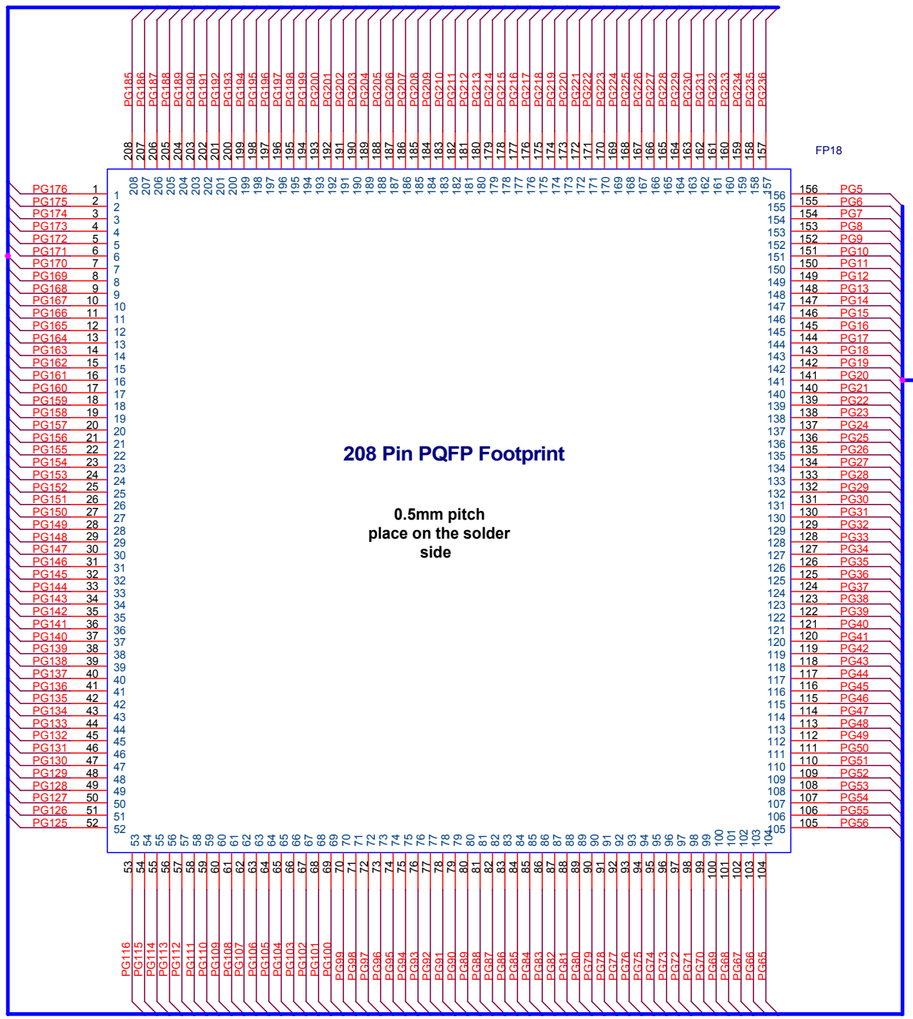
PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

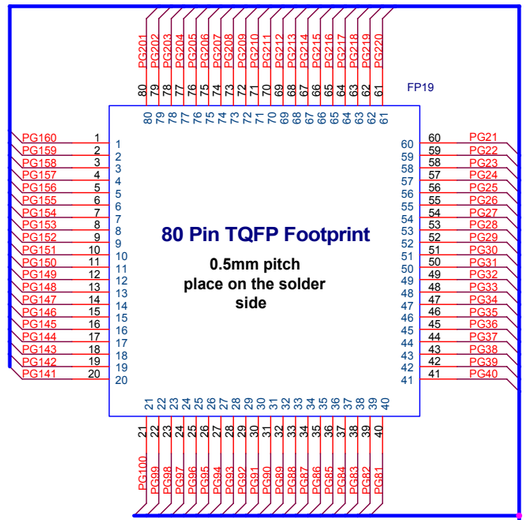
Title: **Prototyping Footprint B**

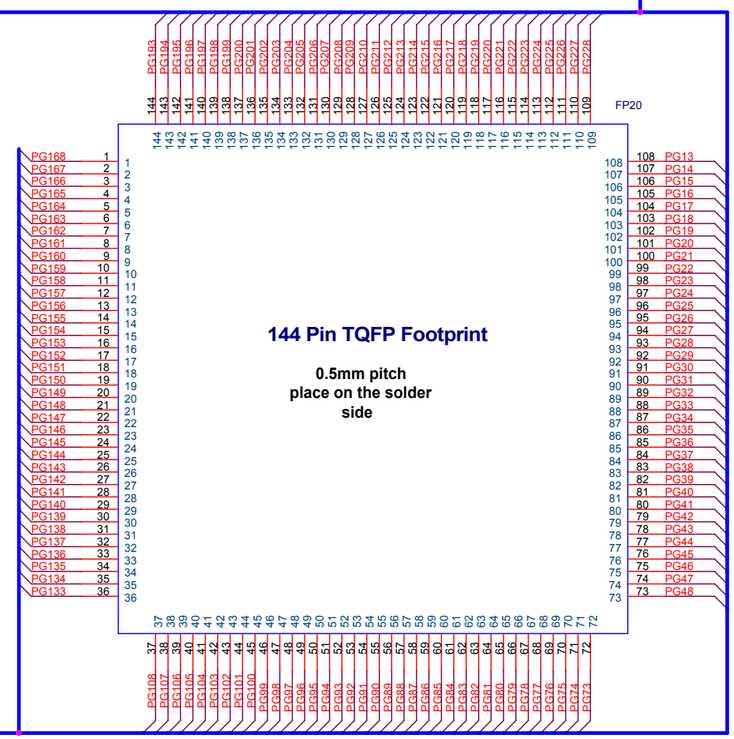
Size	Document Number	Rev
Custom	91-0017-200-A	203

Date: Monday, March 29, 2004 Sheet 8 of 13

Prototyping Footprint C







8 PG[1:240] PG[1:240]

Note: three footprints in this schematic are placed on the solder side of the PCB under the footprint of 240-pin PQFP (FP16). They are arranged as FP19 inside of FP20 and FP20 inside of FP18. All of them share prototyping holes with FP16.

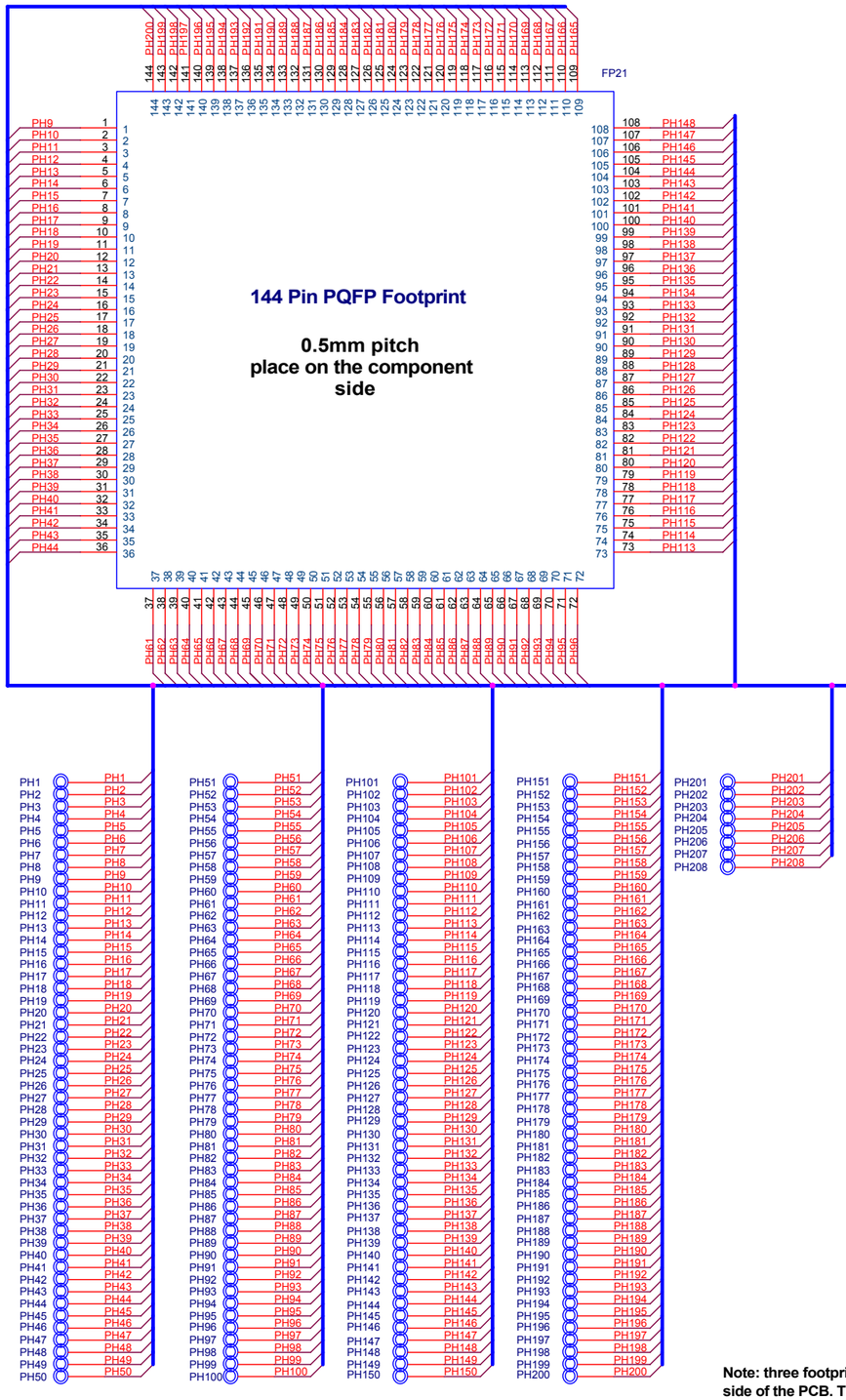
PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

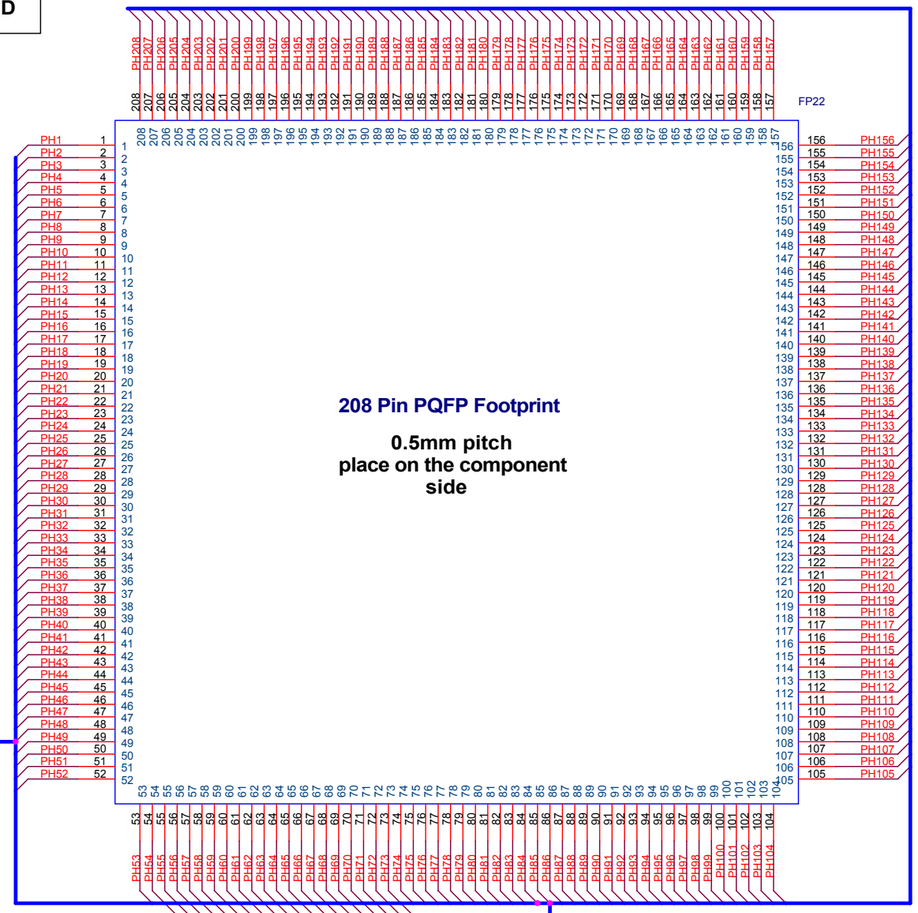
Title: **Prototyping Footprint C**

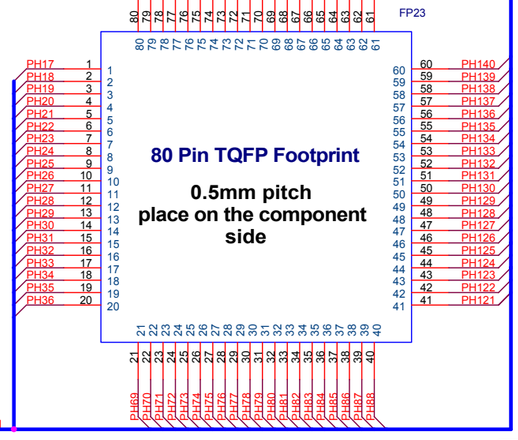
Size	Document Number	Rev
Custom	91-0017-200-A	203

Date: Monday, March 29, 2004 Sheet 9 of 13

Prototyping Footprint D







11 PH[1:208] <<< PH[1:208]

Note: three footprints are placed on the component side of the PCB. They are arranged as FP23 inside of FP21 and FP21 insde of FP22. All 208 holes for prototyping are located outside of 208-pin PQFP footprint.

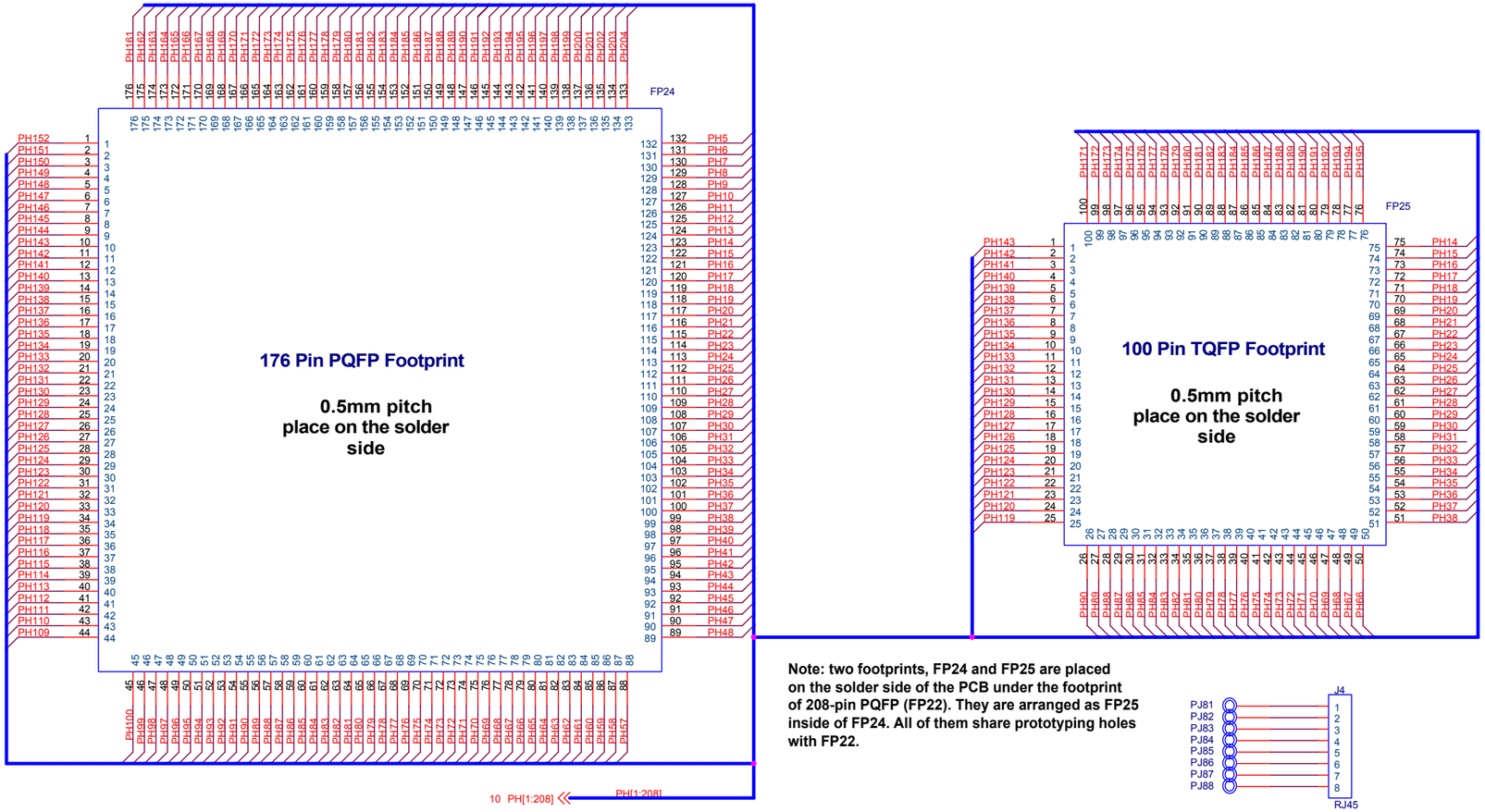
PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title: **Prototyping Footprint D**

Size	Document Number	Rev
Custom	91-0017-200-A	203

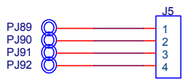
Date: Monday, March 29, 2004 Sheet 10 of 13

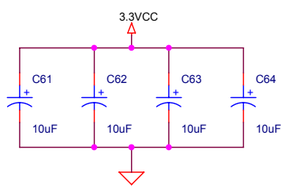
Prototyping Footprint E

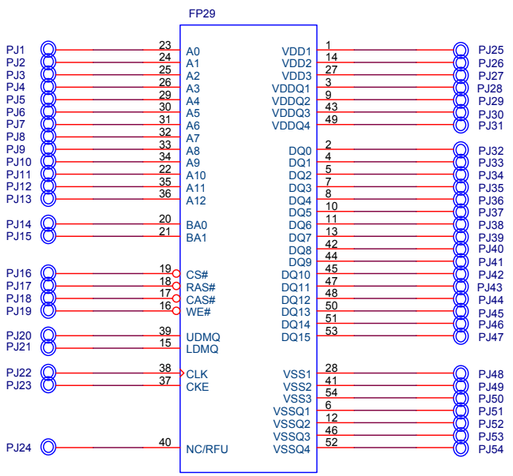


Note: two footprints, FP24 and FP25 are placed on the solder side of the PCB under the footprint of 208-pin PQFP (FP22). They are arranged as FP25 inside of FP24. All of them share prototyping holes with FP22.

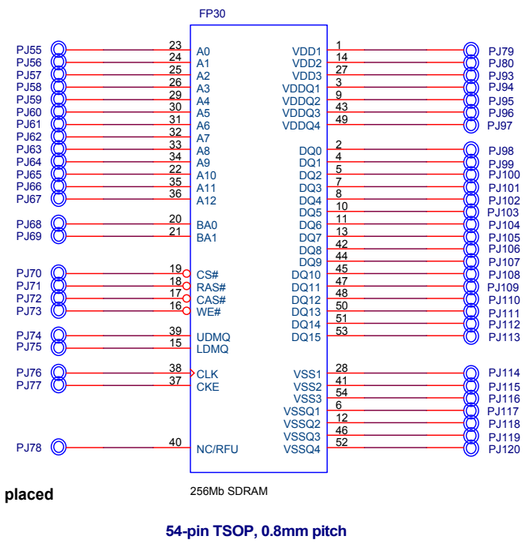
The above connectors are placed on the component side.







Note: FP29 and FP30 are placed on the component side.



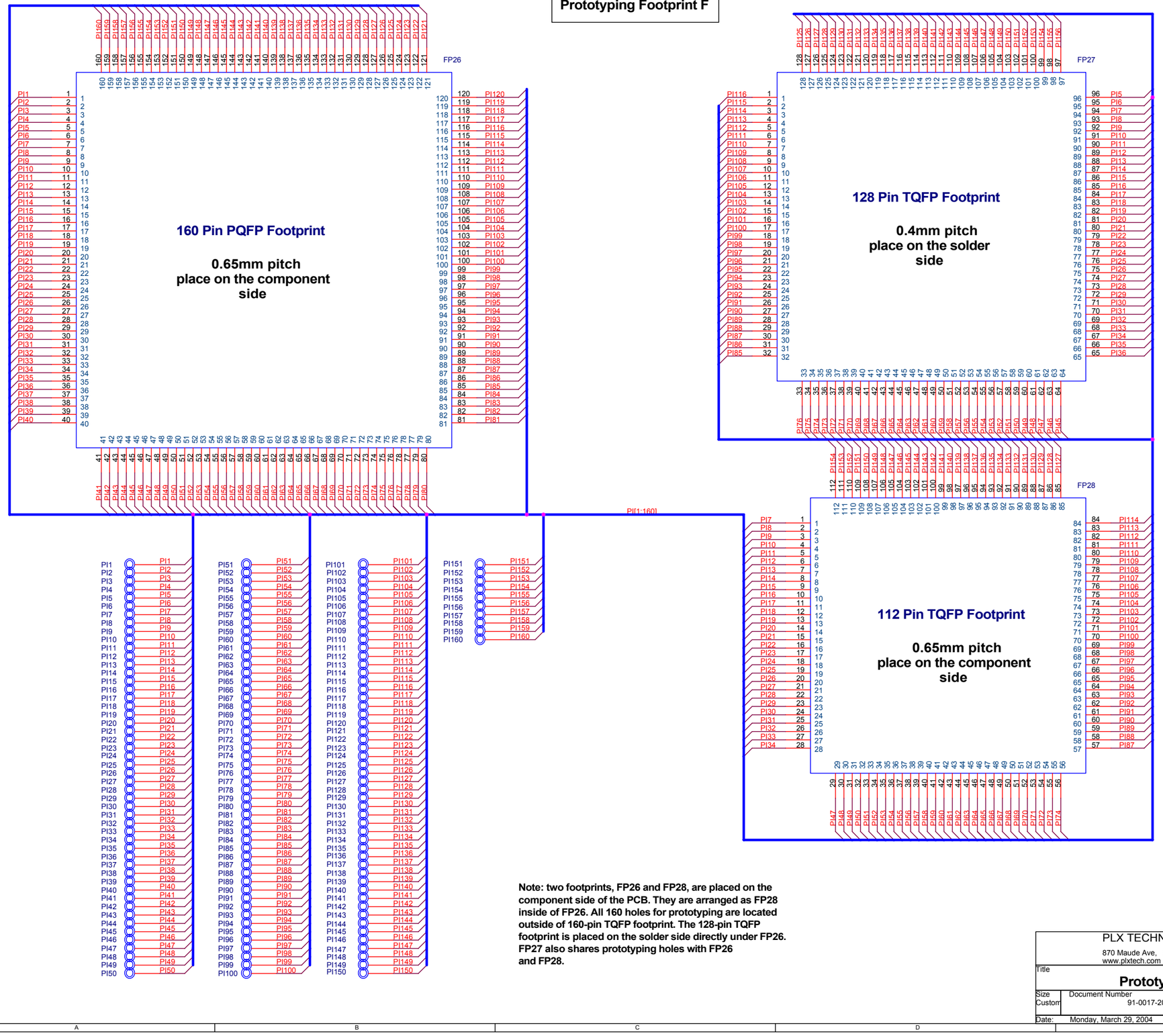
PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title: **Prototyping Footprint E**

Size: Custom | Document Number: 91-0017-200-A | Rev: 203

Date: Monday, March 29, 2004 | Sheet 11 of 13

Prototyping Footprint F



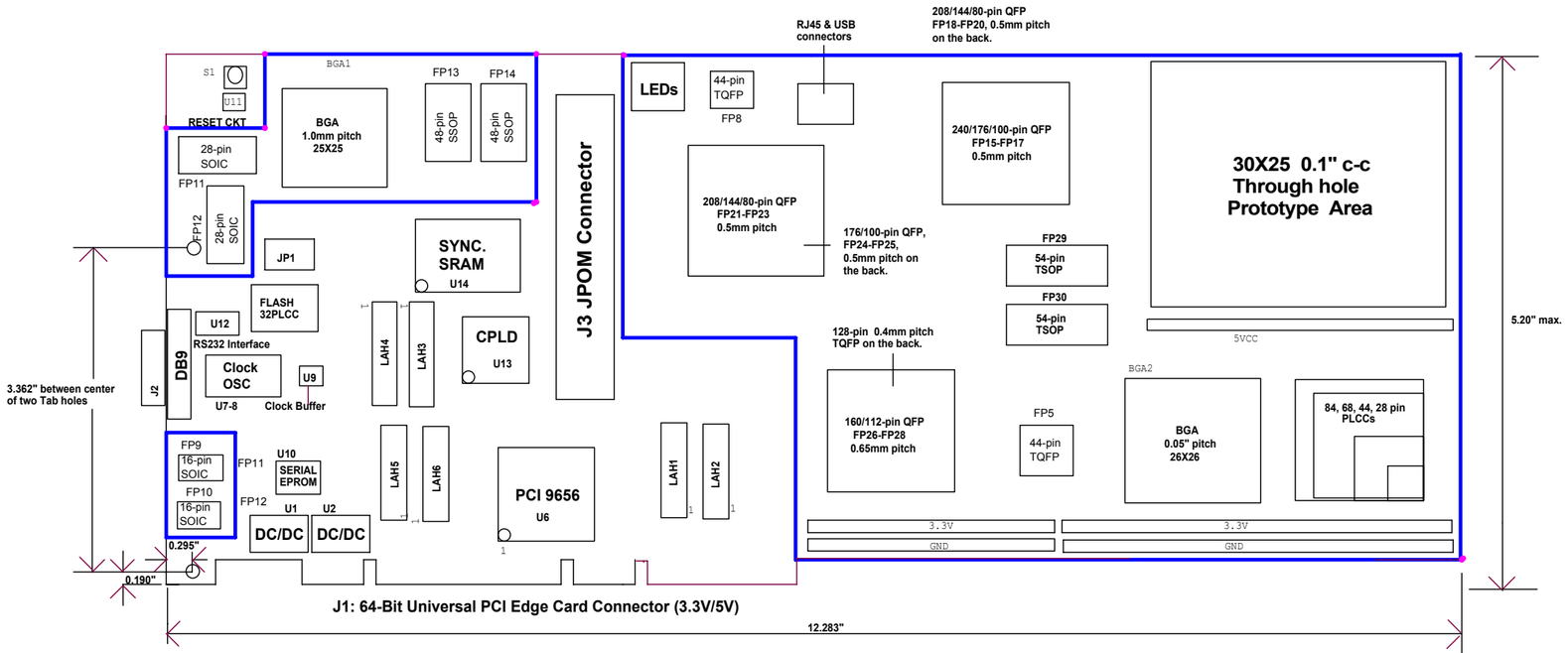
Note: two footprints, FP26 and FP28, are placed on the component side of the PCB. They are arranged as FP28 inside of FP26. All 160 holes for prototyping are located outside of 160-pin TQFP footprint. The 128-pin TQFP footprint is placed on the solder side directly under FP26. FP27 also shares prototyping holes with FP26 and FP28.

PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title: **Prototyping Footprint F**

Size	Document Number	Rev
Custom	91-0017-200-A	203

Date: Monday, March 29, 2004 Sheet 12 of 13



Note:

1. Control Signal Connector (LAH5)
2. Control Signal Connector (LAH6)
3. Data Bus Connector (LAH3)
4. Data Bus Connector (LAH4)
5. Address Bus Connector (LAH1)
6. Address Bus Connector (LAH2)
7. Marked as [ ] is prototyping area

PLX TECHNOLOGY, INC.

870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

Title: **Suggested Board Layout**

Size	Document Number	Rev
Custom	91-0017-200-A	203

Date: Monday, March 29, 2004 Sheet 13 of 13