PCI 9656AD➔PCI 9656BA Conversion Documentation

This document details changes that designers must be aware of as they convert their PCI 9656AD silicon-based designs to use the latest generation PCI 9656BA. Technical assistance is available at the PLX technical support web page (http://www.plxtech.com/support/default.htm).

Related Documentation

Document	Revision	Description	Publication Date
PCI 9656 Data Book	0.90b	Preliminary Data Book	February 2002
PCI 9656 Data Book r.90 Corrections	0.94	Data Book Corrections	June 2002
PCI 9656BA Errata Documentation	0.90	PCI 9656BA Errata	September 2002
PCI 9656AD Errata Documentation	0.96	PCI 9656AD Errata	September 2002

1. Package Marking

The following table details the package marking changes between the PCI 9656AD and the PCI 9656BA.

Table 1-1. PCI 9656AD & PCI 9656BA Package Markings

PCI 9656AD Package Marking	PCI 9656BA Package Marking
PCI 9656-AD66BI YYWW D XXXXXXXXXX KOREA	PCI 9656-BA66BI YYWW D XXXXXXXXXX MALAYSIA

Note. For each chip, **XXXXXXXXXX** is the lot number.

2. Errata Fixes

The PCI 9656BA fixes several PCI 9656AD errata. Refer to the documents “PCI 9656AD Errata Documentation” and “PCI 9656BA Errata Documentation” for details.

3. Pin Types

Description:

The following table details the pin type changes from the PCI 9656AD to the PCI 9656BA.

Table 3-1. PCI 9656AD➔PCI9656BA Pin Type Changes

Ball Number	Symbol	AD Pin Type	BA Pin Type
B18	**C/J Mode** **LHOLD** **M Mode** **BR#**	O TP 24 mA	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.
D14	**C/J Mode** **DMPAF** **EOT#** **M Mode** **MDREQ#** **DMPAF** **EOT#**	*If ((DMAMODE0[14]=1)* *or* *(DMAMODE1[14]=1))* I *else* O TP 24 mA	*If ((DMAMODE0[14]=1)* *or* *(DMAMODE1[14]=1))* I *else* O TP 24 mA **Note for 2nd case:** *If ((HOSTEN# not asserted & RST# asserted* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.
W2	V_{DDA}	I	I **Note:** Changes from V_{DDA} to V_{RING}.
W3	V_{BB}	I	I **Note:** Changes from V_{BB} to V_{SS}.
Y1	V_{SSA}	I	I **Note:** Changes from V_{SSA} to V_{SS}.

4. AC Timing

Description:

The following tables detail the AC timing of the PCI 9656AD and the PCI 9656BA.

Table 4-1. C Mode Local Bus Input AC Timing Specifications

Signals (Synchronous Inputs) V_{CC} = 3.0V, T_a = 85°C	T_{SETUP}		T_{HOLD}	
	AD	BA	AD	BA
ADS#	4.8 ns	2.1 ns	1 ns	1 ns
BIGEND#	4.8 ns	4.0 ns	1 ns	1 ns
BLAST#	4.0 ns	3.4 ns	1 ns	1 ns
BREQi	1.7 ns	0.3 ns	1 ns	1 ns
BTERM#	4.8 ns	4.0 ns	1 ns	1 ns
CCS#	1.7 ns	2.9 ns	1 ns	1 ns
DMPAF/**EOT#**	4.7 ns	4.2 ns	1 ns	1 ns
DP[3:0]	2.0 ns	2.9 ns	1 ns	1 ns
DREQ[1:0]#	4.4 ns	3.3 ns	1 ns	1 ns
LA[31:2]	4.0 ns	3.4 ns	1 ns	1 ns
LBE[3:0]#	4.6 ns	3.6 ns	1 ns	1 ns
LD[31:0]	4.9 ns	3.1 ns	1 ns	1 ns
LHOLDA	4.2 ns	2.5 ns	1 ns	1 ns
LW/R#	5.0 ns	3.5 ns	1 ns	1 ns
READY#	4.7 ns	4.0 ns	1 ns	1 ns
USERi/LLOCKi#	2.4 ns	2.9 ns	1 ns	1 ns
WAIT#	4.7 ns	4.0 ns	1 ns	1 ns
Input Clocks	**Min**		**Max**	
Local Clock Input Frequency	0 MHz		66 MHz	
PCI Clock Input Frequency	0 MHz		66 MHz	

Table 4-2. C Mode Local Bus Output AC Timing Specifications

Signals (Synchronous Outputs) C_L = 50pF, V_{CC} = 3.0V, T_a = 85°C	Output T_{VALID} (Worst Case)	
	AD[1]	BA[2]
ADS#	7.6 ns	6.3 ns
BLAST#	7.6 ns	6.3 ns
BREQo	9.5 ns	6.8 ns
BTERM#	8.3 ns	6.8 ns
DACK[1:0]#	7.6 ns	6.3 ns
DMPAF/EOT#	8.5 ns	6.6 ns
DP[3:0]	7.9 ns	6.8 ns
LA[31:2]	8.0 ns	6.8 ns
LBE[3:0]#	7.6 ns	6.3 ns
LD[31:0]	7.8 ns	6.4 ns
LHOLD	7.5 ns	6.8 ns
LSERR#	10.2 ns	7.5 ns
LW/R#	7.6 ns	6.3 ns
READY#	9.0 ns	7.2 ns
USERo/LLOCKo#	7.6 ns	6.3 ns
WAIT#	7.6 ns	6.4 ns

1 On high-to-low transitions, output T_{VALID} values increase/decrease by 23 ps for each increase/decrease of 1pF.
On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

2 On high-to-low transitions, output T_{VALID} values increase/decrease by 16 ps for each increase/decrease of 1pF.
On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

On high-to-low transitions, the slew rate at 50 pF loading is 1.93 V/ns typical; .94 V/ns worst case.
On low-to-high transitions, the slew rate at 50 pF loading is 1.15 V/ns typical; .70 V/ns worst case.

Table 4-3. J Mode Local Bus Input AC Timing Specifications

Signals (Synchronous Inputs) V_{CC} = 3.0V, T_a = 85°C	T_{SETUP} (Worst Case)		T_{HOLD} (Worst Case)	
	AD	BA	AD	BA
ADS#	4.9 ns	2.1 ns	1 ns	1 ns
ALE	4.5 ns	1.7 ns	1 ns	1 ns
BIGEND#	4.8 ns	4.0 ns	1 ns	1 ns
BLAST#	4.0 ns	3.4 ns	1 ns	1 ns
BREQi	1.7 ns	0.3 ns	1 ns	1 ns
BTERM#	4.8 ns	4.2 ns	1 ns	1 ns
CCS#	1.7 ns	2.9 ns	1 ns	1 ns
DMPAF/**EOT#**	4.7 ns	4.2 ns	1 ns	1 ns
DP[3:0]	2.0 ns	2.9 ns	1 ns	1 ns
DREQ[1:0]#	4.4 ns	3.3 ns	1 ns	1 ns
LA [28:2]	4.0 ns	3.4 ns	1 ns	1 ns
LAD[31:0]	4.9 ns	3.1 ns	1 ns	1 ns
LBE[3:0]#	4.6 ns	3.6 ns	1 ns	1 ns
LHOLDA	4.2 ns	2.5 ns	1 ns	1 ns
LW/R#	5.0 ns	3.5 ns	1 ns	1 ns
READY#	4.7 ns	4.2 ns	1 ns	1 ns
USERi/LLOCKi#	2.4 ns	2.9 ns	1 ns	1 ns
WAIT#	4.7 ns	4.0 ns	1 ns	1 ns
Input Clocks	**Min**		**Max**	
Local Clock Input Frequency	0 MHz		66 MHz	
PCI Clock Input Frequency	0 MHz		66 MHz	

Table 4-4. J Mode Local Bus Output AC Timing Specifications

Signals (Synchronous Outputs) C_L = 50pF, V_{CC} = 3.0V, T_a = 85°C	Output T_{VALID} (Worst Case)	
	AD[1]	BA[2]
ADS#	7.6 ns	6.3 ns
ALE	8.0 ns	See item 5.
BLAST#	7.6 ns	6.3 ns
BREQo	9.5 ns	6.8 ns
BTERM#	8.3 ns	6.8 ns
DACK[1:0]#	7.6 ns	6.3 ns
DEN#	7.9 ns	6.4 ns
DMPAF/EOT#	8.5 ns	6.6 ns
DP[3:0]	7.9 ns	6.8 ns
DT/R#	7.9 ns	6.3 ns
LA[28:2]	8.0 ns	6.4 ns
LAD[31:0]	7.8 ns	6.4 ns
LBE[3:0]#	7.6 ns	6.3 ns
LHOLD	7.5 ns	6.8 ns
LSERR#	10.2 ns	7.5 ns
LW/R#	7.6 ns	6.3 ns
READY#	9.0 ns	7.2 ns
USERo/LLOCKo#	7.6 ns	6.3 ns
WAIT#	7.6 ns	6.4 ns

1 On high-to-low transitions, output T_{VALID} values increase/decrease by 23 ps for each increase/decrease of 1pF.
On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

2 On high-to-low transitions, output T_{VALID} values increase/decrease by 16 ps for each increase/decrease of 1pF.
On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

On high-to-low transitions, the slew rate at 50 pF loading is 1.93 V/ns typical; .94 V/ns worst case.
On low-to-high transitions, the slew rate at 50 pF loading is 1.15 V/ns typical; .70 V/ns worst case.

Table 4-5. M Mode Local Bus Input AC Timing Specifications

Signals (Synchronous Inputs) V_{CC} = 3.0V, T_a = 85°C	T_{SETUP}		T_{HOLD}	
	AD	BA	AD	BA
BB#	4.9 ns	2.7 ns	1 ns	1 ns
BDIP#	4.5 ns	3.8 ns	1 ns	1 ns
BG#	4.4 ns	2.9 ns	1 ns	1 ns
BI#	5.3 ns	4.0 ns	1 ns	1 ns
BIGEND#/WAIT#	4.8 ns	3.8 ns	1 ns	1 ns
BURST#	4.8 ns	4.1 ns	1 ns	1 ns
CCS#	1.7 ns	2.9 ns	1 ns	1 ns
DP[0:3]	2.0 ns	2.9 ns	1 ns	1 ns
DREQ[1:0]#	4.4 ns	3.3 ns	1 ns	1 ns
LA[0:31]	5.2 ns	3.6 ns	1 ns	1 ns
LD[0:31]	4.9 ns	3.1 ns	1 ns	1 ns
MDREQ#/DMPAF/ **EOT#**	4.7 ns	4.2 ns	1 ns	1 ns
RD/WR#	5.3 ns	3.5 ns	1 ns	1 ns
TA#	5.3 ns	4.1 ns	1 ns	1 ns
TEA#	5.2 ns	4.4 ns	1 ns	1 ns
TS#	4.8 ns	2.1 ns	1 ns	1 ns
TSIZ[0:1]#	5.0 ns	3.6 ns	1 ns	1 ns
USERi/LLOCK#	1.9 ns	3.2 ns	1 ns	1 ns
Input Clocks	**Min**		**Max**	
Local Clock Input Frequency	0 MHz		66 MHz	
PCI Clock Input Frequency	0 MHz		66 MHz	

Table 4-6. M Mode Local Bus Output AC Timing Specifications

Signals (Synchronous Outputs) C_L = 50pF, V_{CC} = 3.0V, T_a = 85°C	Output T_{VALID} (Worst Case)	
	AD[1]	BA[2]
BB#	9.4 ns	6.8 ns
BDIP#	7.7 ns	6.4 ns
BIGEND#/**WAIT#**	7.6 ns	6.3 ns
BR#	7.5 ns	6.8 ns
BURST#	7.6 ns	6.3 ns
DACK[1:0]#	7.6 ns	6.3 ns
DP[0:3]	7.9 ns	6.8 ns
LA[0:31]	8.0 ns	6.8 ns
LD[0:31]	7.8 ns	6.3 ns
MDREQ#/DMPAF/ EOT#	8.5 ns	6.6 ns
RD/WR#	7.6 ns	6.3 ns
RETRY#	9.5 ns	6.8 ns
TA#	9.0 ns	7.2 ns
TEA#	9.6 ns	7.5 ns
TS#	7.6 ns	6.3 ns
TSIZ[0:1]#	7.6 ns	6.3 ns
USERo/LLOCKo#	7.6 ns	6.3 ns

1 On high-to-low transitions, output T_{VALID} values increase/decrease by 23 ps for each increase/decrease of 1pF.
On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

2 On high-to-low transitions, output T_{VALID} values increase/decrease by 16 ps for each increase/decrease of 1pF.
On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

On high-to-low transitions, the slew rate at 50 pF loading is 1.93 V/ns typical; .94 V/ns worst case.
On low-to-high transitions, the slew rate at 50 pF loading is 1.15 V/ns typical; .70 V/ns worst case.

5. J Mode ALE Output Timing

Description:

The following figures detail the J Mode ALE signal output timing changes between the PCI 9656AD and PCI 9656BA. LC_{HIGH} is the time in ns that the Processor/Local Bus clock is high.

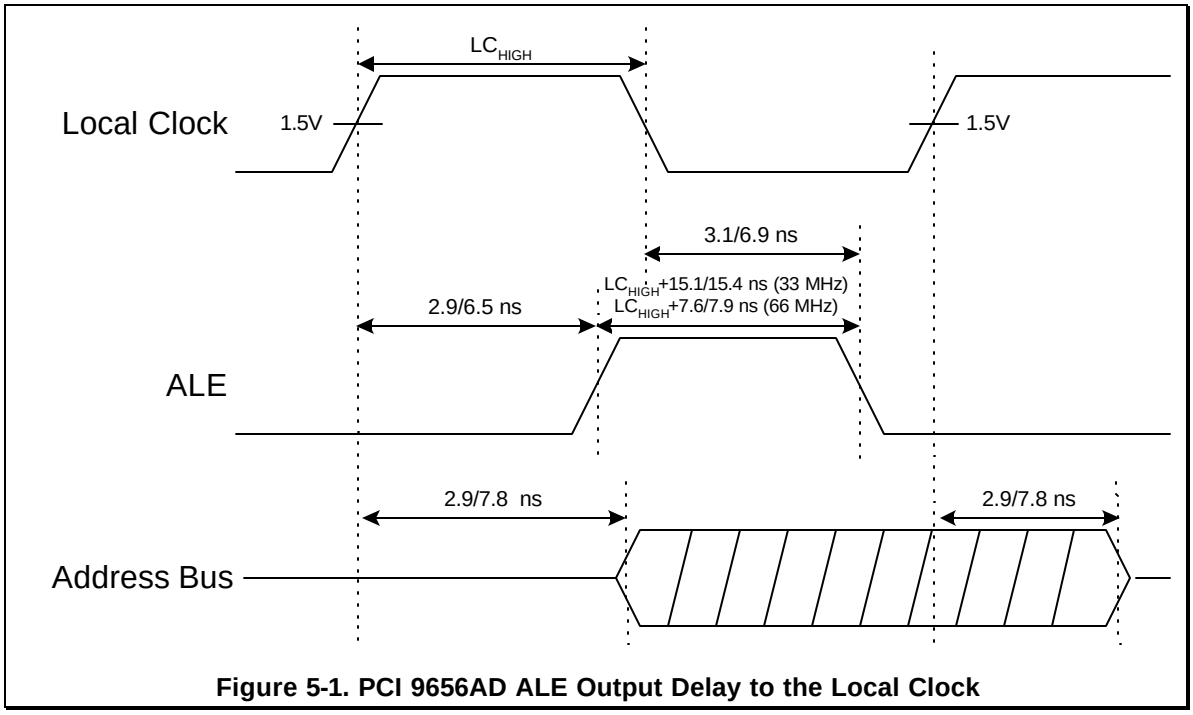

Figure 5-1. PCI 9656AD ALE Output Delay to the Local Clock

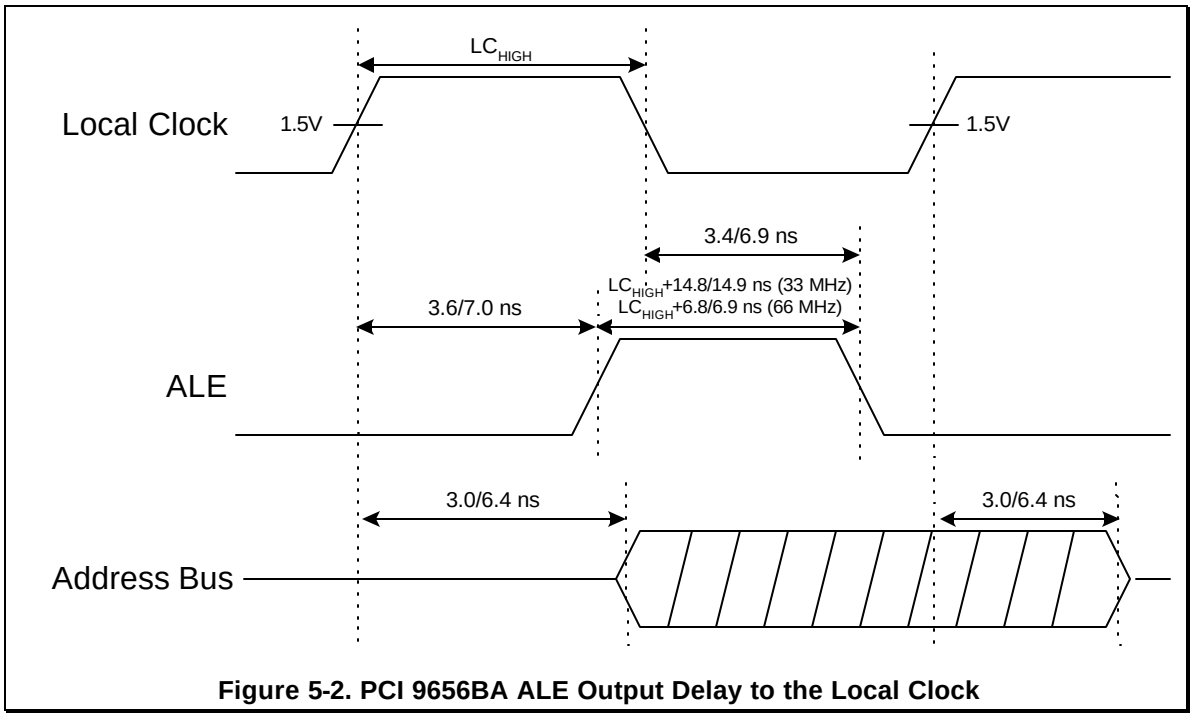

Figure 5-2. PCI 9656BA ALE Output Delay to the Local Clock

6. Register 'Value After Reset' Values

The following table details the register 'Value After Reset' changes from the PCI 9656AD to the PCI 9656BA.

Table 6-1. PCI 9656AD➔ PCI 9656BA Register 'Value After Reset' Values

Register	PCI 9656AD Value After Reset	PCI 9656BA Value After Reset
PCIREV; PCI:08h, LOC:08h	ACh	BAh
PCIHREV; PCI:74h, LOC:F4h	ADh	BAh

7. READY# Time Out Values

If the PCI 9656's READY# time out feature is enabled (LMISC2[0] = 1b), LMISC2[1] is used to determine the number of clocks to wait for a Processor/Local Bus READY# time out.

For the PCI 9656AD:

- LMISC2[1] = 0b selects a time out of **32** Processor/Local Bus clocks.
- LMISC2[1] = 1b selects a time out of **64** Processor/Local Bus clocks.

For the PCI 9656BA:

- LMISC2[1] = 0b selects a time out of **32** Processor/Local Bus clocks. (No change.)
- LMISC2[1] = 1b selects a time out of **1,024** Processor/Local Bus clocks. (Change.)

8. Extra Long EEPROM Load

If the PCI 9656AD uses an Extra Long EEPROM Load (LBRD0[25] = 1b) to overwrite the power on/reset values of its EEPROM-overwritable register bits, it reads EEPROM locations 00h through 5Ah for that purpose.

The PCI 9656BA, in addition to reading EEPROM locations 00h through 5Ah to overwrite the power on/reset values of the same register bits as the PCI 9656AD, reads EEPROM locations 5Ch through 62h to overwrite the power on/reset values of the following Power Management register bits.

Table 8-1. PCI 9656BA Additional Extra Long EEPROM Load Values

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5Ch	**PMC[15:9];** PCI address: 42h Local address: 182h													**PMC[2:0];** PCI address: 42h, Local address:182h		
5Eh																
60h	**PMDATA[7:0];** PCI address: 47h Local address: 187h															
62h		**PMCSR[14:8];** PCI address: 44h Local address: 184h														

Note. Grey bits are reserved and should be set to 0b in the EEPROM.

9. Local Bus Pause Timer Values

If the PCI 9656's Local Bus Pause Timer is enabled (MARBR[17] = 1b), MARBR[15:8] are used to determine the number of the Processor/Local Bus clocks to wait after releasing the bus before attempting to re-arbitrate for the bus.

For the PCI 9656AD, MARBR[8] must be 0b, restricting the Local Bus Pause Timer value to an even number of clocks.

For the PCI 9656BA, MARBR[8] may be 0b or 1b, removing the restriction that Local Bus Pause Timer value be even.

10. IDDQEN#

For both the PCI 9656AD and the PCI 9656BA, hold the IDDQEN# input signal (ball A10) in its asserted state to put the chip in its IDDQ state.

For the PCI 9656AD to perform normal, non-IDDQ operation, during initialization its IDDQEN# input signal must transition from its asserted state to its de-asserted state prior to PCI RST# de-assertion. This causes the PCI 9656AD to configure its PCI I/O buffers for proper bus operation. After this transition completes, hold IDDQEN# in its de-asserted state. (**Note.** For CompactPCI Hot Swap applications, IDDQEN# must be held in its de-asserted state during pre-charge. As a result, CompactPCI Hot Swap applications require that IDDQEN# transition from its de-asserted state to its asserted state after pre-charge completes, and then transition back to its de-asserted state prior to Local PCI RST# de-assertion.)

For the PCI 9656BA to perform normal, non-IDDQ operation, hold IDDQEN# in its de-asserted state. (**Note.** For applications that use the PCI 9656BA's PCI Power Management D3cold PME Generation feature, de-assert IDDQEN# by tying it directly to the 2.5V power source for Vcore. The PCI 9656BA uses IDDQEN# to sense both when Vcore is going away to prepare to enter the D3cold state and when Vcore is coming back to prepare to leave the D3cold state. Do not tie IDDQEN# to the 2.5V power source for 2.5Vaux, and do not tie it to the 3.3V power source for either Vring or Card_Vaux.)

Even though the PCI 9656BA does not require any transitioning of its IDDQEN# input signal for proper PCI bus operation, transitioning the PCI 9656BA's IDDQEN# in accordance with the PCI 9656AD requirements will have no effect on PCI 9656BA operation. As a result, the PCI 9656BA can be substituted for the PCI 9656AD in existing PCI 9656AD designs without needing to remove the external PCI 9656AD IDDQEN# transitioning logic.

11. JTAG IDCODE Instruction

The PCI 9656AD does not support the JTAG IDCODE instruction.

The PCI 9656BA supports the JTAG IDCODE instruction, and returns the following IDCODE value:

Table 11-1. PCI 9656BA JTAG IDCODE Value

MSB 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
Version				Part Number (9656 when converted to decimal)																PLX Manufacturer Identity											
0	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	0	1	1	0	1	1

12. Initializing JTAG

> **Note.** The following only applies if the chip's TRST# pin (D9) is *not* tied low (i.e., JTAG functionality is enabled).

For both the PCI 9656AD and the PCI 9656BA, if JTAG is enabled when power is applied, the chip's JTAG TAP controller comes up in a random state and must be put into the Test-Logic-Reset state.

The PCI 9656AD provides *one* way to put its JTAG TAP controller into the Test-Logic-Reset state:

1. Prior to PCI RST# de-assertion, transition the chip's TRST# pin (D9) from de-asserted to asserted and back to de-asserted.

The PCI 9656BA provides *two* ways to put its JTAG TAP controller into the Test-Logic-Reset state:

1. [Same as PCI 9656AD.] Prior to PCI RST# de-assertion, transition the chip's TRST# pin (D9) from de-asserted to asserted and back to de-asserted.

2. [New to PCI 9656BA.] Prior to PCI RST# de-assertion, hold the chip's TMS pin (B8) high while transitioning the chip's TCK pin (A8) five times from de-asserted to asserted.

13. PCI Master Abort/Target Abort During DMA

For the PCI 9656AD, if a PCI Master Abort or Target Abort occurs during a DMA transfer, all in-process or future DMA and Direct Master transfers are prevented from arbitrating for the PCI bus until the Master Abort or Target Abort status bit (PCISR[13:12]) is cleared.

For the PCI 9656BA, if a PCI Master Abort or Target Abort occurs during a DMA transfer, all in-process or future DMA transfers are prevented from arbitrating for the PCI bus until the Master Abort or Target Abort status bit (PCISR[13:12]) is cleared. However, Direct Master transfers can continue unabated.

For both the PCI 9656AD and the PCI 9656BA, if a PCI Master Abort or Target Abort occurs during a Direct Master transfer, all in process or future DMA and Direct Master transfers are prevented from arbitrating for the PCI bus until the Master Abort or Target Abort status bit (PCISR[13:12]) is cleared.