PCI 9056 Design Note

A. Affected Silicon Revisions

This document details the Interrupt design note for the following silicon:

Product	Part Number	Description	Status
PCI 9056BA	PCI9056-BA66BI	32-bit, 66MHz PCI, 32-bit, 66MHz Local, PBGA Package	Production Released

B. Silicon Documentation

The following documentation is the baseline functional description of the silicon.

Document	Revision	Description	Publication Date
PCI 9056BA Data Book	1.2	Silicon Data Book	October 2008

C. Design Note Documentation Revision History

Revision	Description
1.0	Baseline
1.1	Added Design Notes #3 and #4.
1.2	Added Design Note #5
1.3	Removed Design Note #3 (DMA Demand Mode Documentation) since it is incorporated in the PCI9056 Data Book revision 1.2.
1.4	Updated design note 5 to include ‘Design Issue #2”.

D. Design Notes Summary

#	Description
1	DMA with Local Constant Address must be Lword aligned
2	VPD Implementation
4	Local-to-PCI Demand Mode DMA DREQ# negation coincident with a Direct Slave Preemption or DREQ# negation on second data transfer leaves one Lword of data in the FIFO (C/J mode
5	VIO Power Sequencing

1. DMA with Local Constant Address must be Lword aligned

Design Issue: If the DMA Channel x Local Addressing Mode register bit is set (DMAMODEx[11] = 1, DMA with Constant Address is enabled), the DMA channel x Local Address must be Lword aligned (DMALADRx[1:0] = 00b). If a non-Lword aligned address is used (DMALADRx[1:0] ≠ 00b), the PCI 9056 initially provides a byte or word aligned Constant Address, and valid TSIZ[1:0] value (M-mode only), on the LA[1:0] for C/J-mode or LA[31:30] and TSIZ[1:0] for M-mode pins for the DMA transfer, but upon a disconnect then subsequent reconnection the silicon will drive the two lower address and TSIZ pins to 00b. Additionally, for J-Mode the LAD[1:0] pins will provide a byte or word aligned address only with the first ADS# assertion.

Recommendation: For Constant Address DMA do not use the lowest 2 address bits of the Local Address LA/LAD[1:0] (C/J-mode) or LA[30:31] (M-mode) to decode non-Lword aligned byte or word addresses. Instead always set the DMA Channel x Local Address to be Lword aligned (DMALADRx[1:0] = 00b), and use upper address lines when designing 8- or 16-bit device select decoding logic.

2. VPD Implementation

Documented Behavior: The PCI 9056 supports the Vital Product Data (VPD) optional feature detailed in PCI Specification r2.2. The PCI 9056 VPD feature supports storage of a VPD data structure within a serial EEPROM (2k- or 4k-bit, 3-wire interface). The PCI Specification defines the first element within this data structure as the Identifier String at VPD address 0h. Additionally, the PCI Specification requires that the VPD registers (in PCI Configuration Space) be used to read/write VPD data only.

At power-up reset, the PCI 9056 reads 100 bytes of configuration data from a serial EEPROM, beginning with the PCI Device ID value stored at address 0h. Although this address seemingly conflicts with VPD requirements, PLX choose to store configuration data beginning at address 0, in order to maintain compatibility with legacy devices (such as PCI 9054). Additionally, the PCI 9056 provides CNTRL[31,27:24] register bits to allow programming of configuration data within the serial EEPROM, without using the VPD registers.

Solution/Workaround: VPD data storage can be implemented with a serial EEPROM used exclusively for VPD (and not containing PCI 9056 configuration data). Because the PCI 9056 will attempt to read configuration data through the serial EEPROM interface at power-up reset, the VPD EEPROM should not be enabled until PCI 9056 initialization completes (when EECS de-asserts).

The following sample circuit includes two serial EEPROMs, one for initialization and the other for VPD, with only one EEPROM enabled at any time. The circuit initially enables the Initialization EEPROM during power-up reset. After the first EECS de-assertion, the circuit enables access to the VPD EEPROM and disables access to the Initialization EEPROM. The D flip-flop and inverter can both be replaced by a negative edge-triggered J-K flip-flop such as the 74HCT107, with its J input tied high and its K input tied low.

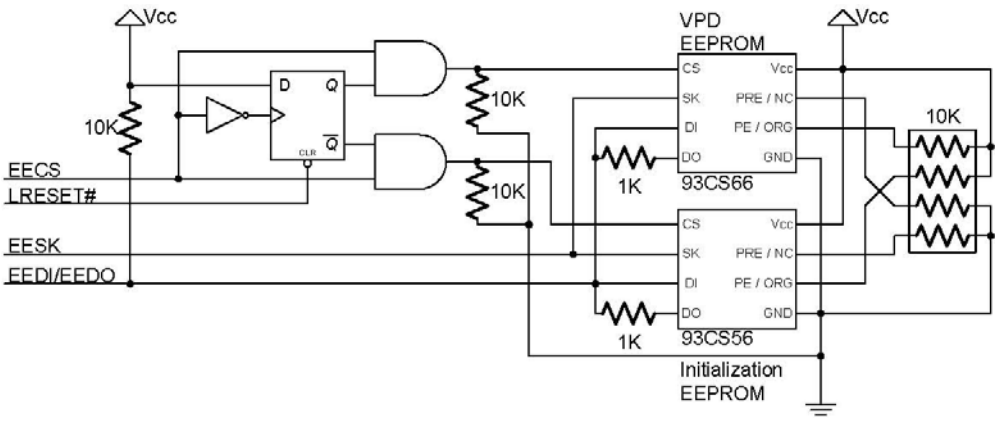

Figure 1. Sample VPD Implementation Circuit

To allow programming of the Initialization EEPROM, this circuit can be modified such that the flip-flop CLR input is driven by the output of an AND gate instead of from LRESET# directly, with LRESET# connected to one of the AND gate inputs. If any AND gate input is low, the gate output is low, which will enable the Initialization EEPROM and disable the VPD EEPROM.

The following sample circuit includes one serial EEPROM for VPD-only access, and applies to designs having a Local Bus processor that will initialize the PCI 9056, including setting of the Init Done bit (LMISC1[2] = 1).

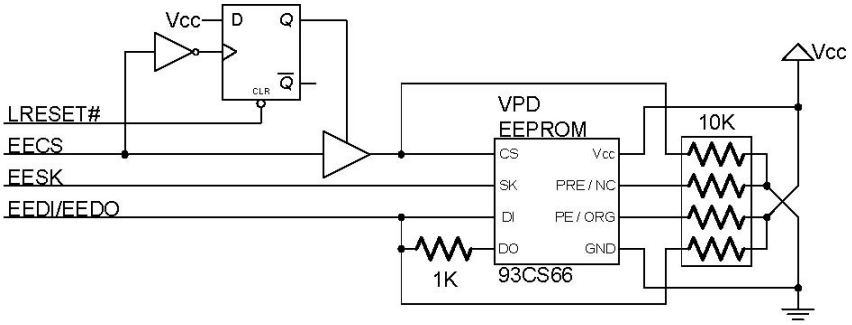

Figure 2. Sample VPD Implementation Circuit without Initialization EEPROM, and Local CPU sets PCI 9056 Init Done bit

If neither a serial initialization EEPROM nor Local CPU is present to set the Init Done bit, the EEDI/EEDO line must be pulled low with a 1K resistor (which will cause the PCI 9056 itself to set the Init Done bit). To implement VPD in such case, the EEDI/EEDO line in the above circuit would have to be switched to connect only to a pull-down (removing connection to the EEPROM) during the time that the Q output of the D flip-flop is low.

The PCI 9056 will reload its configuration registers from serial EEPROM if the Reload Configuration Registers register bit (CNTRL[29]) is transitioned from 0 to 1, or when its Power State (PMCSR[1:0]) is transitioned from D3hot to D0 state. Transitioning the Power State from D3hot to D0 state causes LRESET# assertion, and therefore the circuit will correctly access the Initialization EEPROM in such case. Prior to any setting of the Reload Configuration Registers bit (CNTRL[29]), the designer should ensure that Initialization EEPROM access is enabled, by first performing a Software Reset (CNTRL[30]) to cause LRESET# assertion, since PCI 9056 registers must be reloaded with configuration data and not VPD data.

4. Local-to-PCI Demand Mode DMA DREQ# negation coincident with a Direct Slave Preemption or DREQ# negation on second data transfer leaves one Lword of data in the FIFO (C/J mode)

Design Issue #1: Depending upon the PCI destination address, when DREQ# is asserted (to start or resume a Demand Mode DMA Local-to-PCI transfer), and where DREQ# is negated (to pause the transfer) the silicon will predictably require 1 to 2 additional Lwords to be read into the DMA FIFO. Additionally, once the data is read into the FIFO the silicon will write all of the data to the PCI bus. However, if a Direct Slave transfer preempts the DMA coincident with the de-assertion of DREQ# the silicon may not read the additional Lword it needs to assemble and write a 64-bit quantity to the PCI bus. In this case, one Lword of data will remain in the DMA FIFO until the transfer is resumed with a re-assertion of DREQ#.

Recommendation: To ensure the silicon will not leave any data in the DMA FIFO when the transfer is paused detect this condition by checking the expected Lword count (even or odd depending upon the PCI starting or resuming address) when BLAST# is asserted by the silicon in response to a DREQ# negation. If the condition is detected and one additional Lword is needed, assert DREQ# for one clock cycle on the second clock cycle after the BLAST# assertion. Once the Direct Slave transaction(s) are completed the silicon will read the additional Lword and transfer a 64-bit quantity of data to the PCI bus.

Design Issue #2: If DREQ# is asserted (to start or resume a Demand Mode DMA Local-to-PCI transfer) and then DREQ# is subsequently negated (to pause the transfer) on the second data transfer one additional Lword (third data transfer) will be read into the DMA FIFO and will remain their until the transfer is resumed with a re-assertion of DREQ#.

Recommendation: Avoid this issue by not negating DREQ# as described above or use the same solution as described in recommendation for Design Issue #1.

5. VIO Power Sequencing

Design Issue #1: PCI 9056 Data Book Section 13.1 states, with respect to power sequencing requirements, the following: there are five different power sources-Vring, Card_Vaux, Vcore, 2.5Vaux, and VIO. To properly sequence power to these five sources, the only requirement is that Vcore, 2.5Vaux, and VIO must receive power no later than 10 ms after Vring and Card_Vaux receive power... **Caution:** Violating the above power sequencing requirement **will** damage the PCI 9056 device.

Each PCI pin/pad contains two clamping diodes, one to VIO and the other to ground. If the VIO voltage source is not powered and it presents a low impedance path to ground, the PCI 9056's VIO pins can source high current, which could damage the part immediately or cause undue long-term electrical stress to the part. The amount of current each PCI pin/pad will source is dependent upon the device that is driving the signal/pad, or upon the value of the pull-up resistor when the signal is not driven.

Design Issue #2: An issue has been seen on certain PCI platforms in which at power-on, VIO is driven to 5.0 V before Vring and Vcore supplies receive power. In these systems, it was discovered that during this time, the VIO balls of the PCI 9x56 may sink high current, causing

stress and/or damage to the PCI 9x56 device. This problem does not affect platforms where the VIO rail is powered at 3.3V. Analysis has shown that as VIO voltage increases above approximately 4.0V, VIO balls begin to sink high current until Vring and Vcore have power.

Engineering Change: For designs and add-in cards that have an independent voltage source for VIO for which proper power sequencing cannot be guaranteed, a resistor **MUST** be used between the VIO voltage source and PCI 9056 VIO pins to limit the current and protect the device from damage or long term undue stress. Use the following guidelines to determine the value of this required resistance.

A 40-200 ohm resistance between the VIO voltage source and PCI 9056 VIO pins is recommended if VIO will be a maximum of 3.6 Volts (3.3 Volt signaling environments only). For designs that can operate in either 3.3 or 5.0 Volt signaling environments, 40-70 ohm resistance is recommended. A single resistor can be used if the VIO pins are bused, or multiple parallel resistors can be used between the VIO voltage source and the VIO pins. The power dissipation rating of the resistor(s) depends upon the size of the resistance and the signaling environment. For example, if a single 50 ohm resistor is used in a 5V signaling environment, the worst case power dissipation would be 480mW calculated as (V*V)/R (5.5V (maximum signal amplitude plus 10%) - 0.6V (1 diode drop)) squared divided by 50 ohms = 480mW. If four 200 ohm resistors are used in parallel, each would need to be able to dissipate 120mW.

Any resistance value within the recommended ranges will prevent the part from being damaged while providing enough clamping action to keep the Input Voltage (V_{IN}) below its maximum rating. A resistance value at the lower end of the range is recommended to provide better clamping action and therefore provide more Input Voltage (V_{IN}) margin.