PCI 9054 Conversion from Rev. AB to Rev. AC

A. Affected Silicon Revisions

Product	Part Number	Description	Production
PCI 9054	PCI 9054-AB50PI	Released 176-pin PQFP Product	August 1999
PCI 9054	PCI 9054-AB50BI	Released 225-pin PBGA Product	August 1999
PCI 9054	PCI 9054-AC50PI	Released 176-pin PQFP Product	February 2002
PCI 9054	PCI 9054-AC50BI	Released 225-pin PBGA Product	February 2002

B. Documentation Revision

Document	Revision	Description	Publication Date
PCI 9054 Data Book	2.1	Data Book	January 2000
PCI 9054AB Errata	See www.plxtech.com for latest revision	Errata Documentation	
PCI 9054AC Errata	See www.plxtech.com for latest revision	Errata Documentation	
PCI 9054 Design Notes	See www.plxtech.com for latest revision	Design Note Documentation	

C. Conversion Document Summary:

The PCI 9054 revision AC is now available from PLX. The PCI 9054AC is a metal-only change to the PCI 9054 revision AB silicon, implemented to address several errata present in the AB version of the device. This Conversion Document was created to ease migration from the PCI 9054AB to the PCI 9054AC.

The impact of the errata fixes on existing designs is described in Section D of this document. The errata that exist in the PCI 9054AB silicon are also listed in Section D of this document, along with the status of these errata in the PCI 9054AC silicon. The errata fixes resulted in some signals, register definitions, and AC Electrical Characteristic that differ from those published in the PCI 9054, Data Book, revision 2.1 (see sections E and F for a description of these differences).

A summary of the sections in this document is as follows:

#	Description
D	Impact of Errata Fixes on Existing Designs
E	M-Mode AC timing changes
F	Change to Hot Swap Control/Status Register

D. Impact of Errata Fixes on Existing Designs

This section lists the errata that exist in the PCI 9054AB silicon, the corresponding status of this erratum in the AC silicon, and any hardware/software changes that would be required to make the AC silicon work in an existing AB design.

When the PCI 9054AC is operated in generic C-Mode or J-Mode, all errata fixes are completely backward compatible with existing designs. No changes are required to the existing design, however the hardware and/or software workarounds implemented for AB silicon operation may be eliminated to reduce cost or improve performance.

When the PCI 9054AC in operated in M-Mode, the AC timing characteristics of a subset of local bus signals has changed. Please refer to Section E of this document.

The following table contains a complete list all known errata that exist in the PCI 9054AB silicon. The errata numbers listed in the AB ERRATA # column coincide with the PCI 9054 errata document found on http://www.plxtech.com.

AB ERRATA #	DESCRIPTION	AC FIX STATUS
1	LOCK# negation during an idle phase	Not an Errata
2	Unaligned transfers with EOT# asserted on last data transfer fail	Not fixed
3	DMA Channel 0 Almost Full Threshold Value of Zero on Local-to-PCI transfers	Fixed
4	PCI Target Abort during DMA Transfer	Not an Errata
5	M-mode Direct Master Burst Read may cause improper RETRY# assertion if FIFO preempts Burst	Fixed
6	Vital Product Data (VPD) Transfer Status Flag update	Fixed
7	Simultaneous Write to Queue Register in Messaging Unit	Not Fixed
8	M-mode DMA Local-to-PCI Burst Transaction with DMA FIFO full	Fixed
9	Power Management State Change from D_{3hot} to D_0	Fixed
10	DMA PCI-to-Local Transfer with MWI Feature Enabled	Fixed
11	Backoff (BREQo) or RETRY# assertion for PCI Initiator Read transactions	Fixed
12	Direct Master Read with PCI Initiator Cache enabled	Not Fixed
13	PCI Device ID value	Not Fixed
14	M-mode Burst Inhibit (BI#) input qualification	Fixed
15	DMA fails when the DMA channel abort bit (DMACSRx[2]) is set from the PCI bus	Fixed
16	BREQo asserted without LHOLD after a Direct Master read is backed-off if WAIT# and READY# are asserted together	Fixed
17	Cannot perform a new read or write after backoff – Must resume with last address	Not Fixed
18 (A-E)	M-mode TEA# pin/signal can be asserted improperly	Fixed
18 (F)	Critical Issue – PCI 9054AB behavior to a TEA# assertion	Not Fixed
19	Local Bus Upper Byte Lane Parity Checking	Fixed
20	PCI 9054AB asserts ENUM# twice during Hot Swap insertion, causing driver to be loaded twice	Fixed
21	Local Parity Error Status Bit and Interrupt Assertion	Not Fixed
22	C/J-mode DMA Burst-4 Mode with Constant Address	Not Fixed
23	J-mode DMA with Constant Address	Not Fixed
Design Note 12	PCI 9054 will occasionally drive LSERR# output in Test mode	LSERR# output no longer driven in Test Mode

E. M-Mode AC Timing Changes

As a result of the enhancements made from the PCI 9054 AB to AC silicon, some M-Mode output timings in the PCI 9054AC differ from the AC Electrical Characteristics that are published in the PCI 9054, Data Book, revision 2.1, Table 13-8. The PCI 9054 Data Book, revision 2.2, will reflect these changes. The M-Mode timing differences are as follows:

Signal (Synchronous Outputs) C_L = 50 pF, Vcc = 3.0V, Ta = 85 °C	**Clock to Out Worst Case (ns) T_{VALID} (Max) PCI 9054 Revision AC** (Data Book Rev 2.2)	**Clock to Out Worst Case (ns) T_{VALID} (Max) PCI 9054 Revision AB** (Data Book Rev 2.1)
BDIP#	13.2	10.5
LA[0:31]	10.2	10.0
DMPAF	N/A*	13.0
TEA#	9.3	8.5

* Note that the DMPAF signal is an asynchronous signal; therefore, it will be captured on the next clock edge.

F. Hot Swap Control/Status Register Change

As a result of the enhancements made from the PCI 9054 AB to AC silicon, the Hot Swap Control/Status register (HS_CSR: PCI:4Ah, LOC:18Ah) Board Insertion ENUM# Status Indicator, bit 7 reset value differs from AB to AC silicon. For this register, PCI 9054AB silicon returns a value of 1 after reset, and the AC silicon returns a value of 0.

Device	Value After Reset
PCI 9054AB	1
PCI 9054AC	0

This change will be transparent to software for most systems. When a board containing the PCI 9054 is inserted into a live system, engaging of the Hot Swap Switch triggers Bit 7 to a “1” and informs the system of the Hot Swap insertion. Bit 7 is then read as a “1” by the ENUM# interrupt service routine.

If the PCI 9054 is powered up at the same time that the system is powered up, no ENUM# interrupt is generated for the system. The bit won’t be read until the Hot Swap Switch is engaged, triggering Bit 7 to a “1” and informing the system of the Hot Swap insertion.