# PCI 9054RDK-LITE

Errata Revision 1.1
March 2003

# Errata Documentation

## 1. The Reset Button Does Not Function

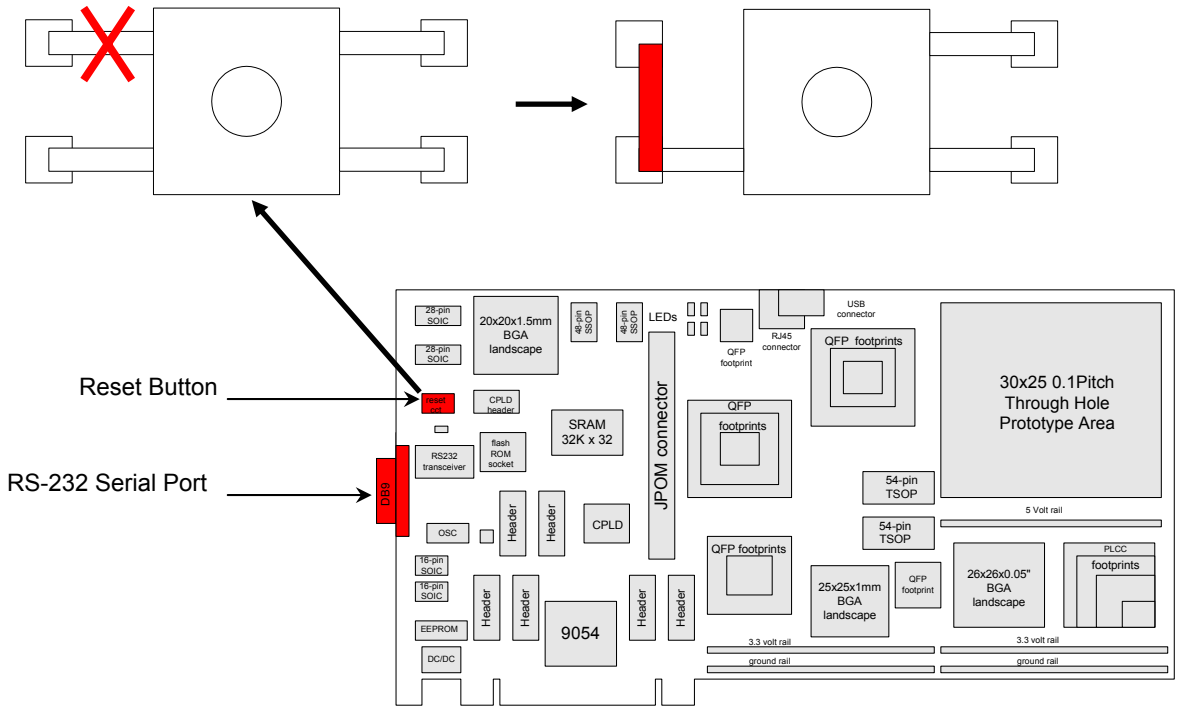
**Note.** This erratum pertains to all revisions of the PCI 9054RDK-LITE.

### Description:

Due to a board layout error, Pin 3 of the reset button (U8) is improperly grounded, which prevents the reset circuit from functioning.

### Workaround (execute the following three steps in order):

1. Face the board component side to you and place the RS-232 serial port to your left side. The reset button is at the top-left corner of the board.
2. Disconnect the top left pin of the reset button from the board pad.
3. Wire the bottom left pin of the reset button to the top left pin board pad.



## 2. PCI 9054's PME# Pin Connects Directly to PCI Connector's PME# Pin

**Note.** This erratum pertains to all revisions of the PCI 9054RDK-LITE.

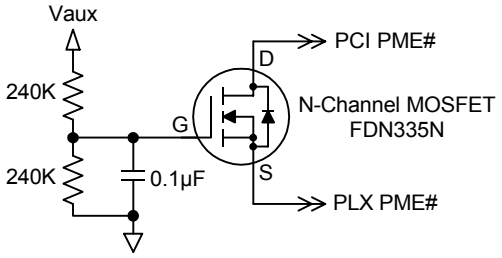
### Description:

On the PCI 9054RDK-LITE, the PCI 9054's open collector PME# pin (167) connects directly to the PCI connector's PME# pin (A19). This violates the PME# electrical requirements detailed in the *PCI Bus Power Management Interface Specification, Revision 1.1, December 18, 1998*, Chapter 7, Power Management Events, paragraph 7 of page 55 through all of page 57. As a result, inserting the RDK into a PCI slot while the system is in a low-power state could cause the system to detect an unintentional PME# assertion and consequently wake up.

### Workarounds (do one of the following):

1. If the application does not require that the RDK generate power management events (i.e., PME# assertions are not required), cut the trace between the PCI 9054's PME# pin (167) and the PCI connector's PME# pin (A19). This trace is accessible on the RDK's solder side, where the trace can be cut between two test points in the circuit, TP4 and TP312.

2. If the application requires that the RDK generate power management events (i.e., PME# assertions are required), to add the required isolation of the PCI 9054's PME# pin from the PCI Connector's PME# pin, refer to the circuit diagram in the Implementation Note on page 57 of the PCI *Bus Power Management Interface Specification, Revision 1.1, December 18, 1998* (also re-printed as Figure 23-17 on page 534 of *PCI System Architecture, Fourth Edition,* by Tom Shanley and Don Anderson). If you use an FDN335N N-channel MOSFET for this circuit, since this MOSFET has an internal protection diode between its source (diode anode) and drain (diode cathode), the source and drain must be reversed from those shown in the circuit diagram. The following circuit diagram illustrates this:




## 3. R18 is not needed

**Note.** This erratum pertains to revisions of the PCI 9054RDK-LITE that use the AB or AC revisions of the PCI 9054 silicon.

### Description:

On the PCI 9054RDK-LITE, R18 is a 510 ohm pull-up resistor connected to the PCI 9054 BREQo/RETRY# output pin (149). The BREQo/RETRY# pin is adjacent to the BREQi/BB# input pin (150). The RDK was originally designed using PCI 9054 revision AA silicon, which required a 510 ohm pull-up on the BREQi/BB# input pin when configured for M Mode (BB#) operation. For the PCI 9054 AB and AC silicon revisions, the BREQi/BB# buffer type changed from Open Drain

to DTS (upon de-assertion driven inactive for ½ clock then floated). Due to this change, the recommended resistor value for the BREQi/BB# input is 4.7k ohms for the AB and AC silicon revisions. The PCI 9054RDK-LITE now ships with revision AC silicon configured in C Mode. With R18 connected to BREQo/READY#, the PCI 9054 needlessly sources current through this resistor. While this does not cause failure, this aspect of the reference design should not be copied to other designs.

### Workarounds (do one of the following):

1. If the PCI 9054RDK-LITE is used in its default C Modes configuration, or it is modified for J Mode operation, remove R18. In either case, if BREQi is not used, either connect the BREQi/BB# input pin (150) to a pull-down resistor, or tie it directly to ground. This will prevent possible input buffer oscillation since no internal pull-down resistor is provided.

2. If the PCI 9054RDK-LITE is modified for M Mode operation, remove R18 and connect a 4.7k ohm pull-up to the BREQi/BB# input pin (150).

## 4. CLK trace length

**Note.** This erratum pertains to all revisions of the PCI 9054RDK-LITE.

### Description:

Section 4.4.3.1 of the *PCI Local Bus Specification, Revision 2.2, December 18, 1998,* requires that the CLK signal trace length on expansion boards must be 2.5" ± 0.1". On the PCI 9054RDK-LITE, the CLK trace length is less than the required value.

### Workaround:

Designs based upon the PCI 9054RDK-LITE should ensure that the PCI CLK trace complies with the *PCI Local Bus Specification, Revision 2.2, December 18, 1998* trace length requirement.