PCI 9052RDK-LITE
Hardware Reference Manual

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PREFACE

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ABOUT THIS MANUAL

This document describes the PLX PCI 9052RDK-LITE, a Rapid Development Kit, from a hardware perspective. It contains a description of all major functional circuit blocks on the board and also is a reference for the creation of software for this product. This manual also includes complete schematics and bill of materials.

REVISION HISTORY

Date	Version	Comments
June 2001	0.50	Yellow Book initial release.
November 2001	1.0	Hardware Reference Manual release
June 2002	1.1	Section 2.2: Clarified PCI 9052 feature set. Table 3-2: Changed offset 28h register value description and clarified offset 5Ch register value description. Section 3.4.1: Added exceptions to ISA compatibility. Section 4.1.2: Clarified how to enable a local address space. Section 4.2.4.1: Changed LASxBRD register settings for 8-bit and 16-bit ISA operation. Section 4.2.4.2: Added CNTRL[18] value for PCI v2.1 compatible systems. Section 4.2.5: Added recommendation that disabled LINTix pins should not be left floating. Section 6: Updated BOM and changed schematic to reflect BOM update.
March 2003	1.2	Updated Schematic and Bill of Materials.
October 2004	1.3	Add Notes 2 and 3 at Table 3-4 Configuration Jumper Settings. Add Note to Section 1.2 RDK Installation. Update Bill of Materials. Add Section 4.4, ISA Interface AEN Signal

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1. General Information

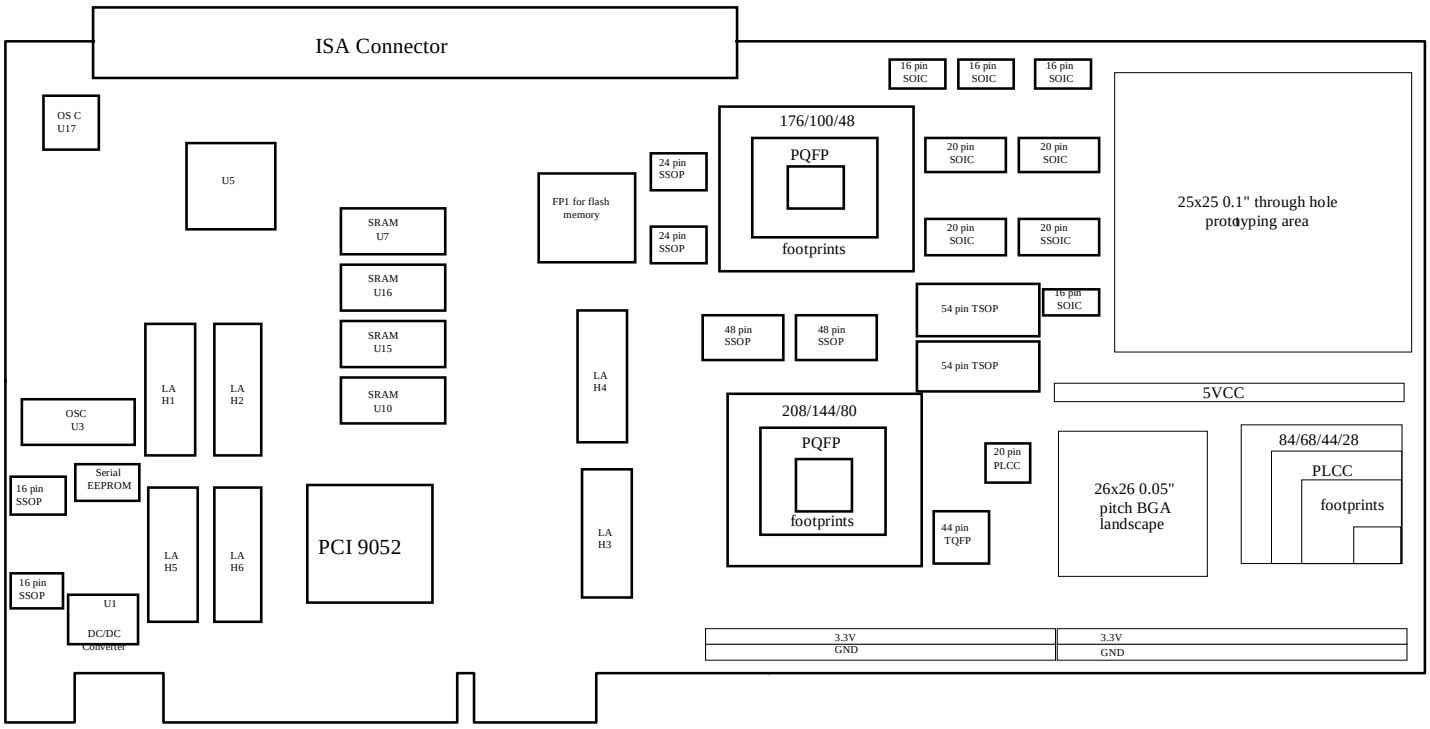


Figure 1-1. PCI 9052RDK-LITE Layout Diagram

The PCI 9052RDK-LITE (RDK-LITE) is a flexible Rapid Development Kit for designs using the PLX PCI 9052 bus target device. It features 1 BGA and 28 surface-mount QFP/PLCC/SSOP/SOIC prototyping footprints for hardware designers to easily add memory, FIFO, I/O devices etc. These allow designers to test, simulate, and debug their designs without fabricating their own boards, saving considerable time and money in the development process and shortening time to market. The RDK-LITE also contains an ISA connector that connects directly to the PCI 9052 ISA bus interface, allowing designers to plug an ISA board onto the RDK board to immediately test the data transfer between ISA and PCI buses. The RDK-LITE kit comes with the PLX Software Development Kit CD-ROM that provides a complete Windows host side software development environment.

1.1 Features

The PCI 9052RDK-LITE Rapid Development Kit (RDK-LITE) board is a versatile PCI bus target development platform. It contains a 12.28" L x 5.20" W, four-layer, assembled PC board with the following features:

- PLX PCI 9052 PCI Target interface chip with direct ISA interface
- ISA bus interface connector
- Socketed serial EEPROM for PCI 9052 configuration
- Support for 16-bit ISA and 32-bit multiplexed and non-multiplexed local bus modes
- CPLD with spare capacity for additional prototyping logic
- Twenty-eight surface-mount QFP/PLCC footprints and one 0.05" pitch BGA landscape for memory, FIFO, I/O devices, logic devices, etc.
- 32-pin PLCC socket for expansion ROM
- On-board 128KB of SRAM and associated logic for PCI 9052 continuous burst read/write accesses
- Socketed 32 MHz oscillator for local bus clock
- 5V to 3.3V voltage regulator
- Six logic analyzer headers with standard HP footprint to allow easy probing of local bus signals
- 25x25, 0.1" through-hole prototyping grid

1.2 RDK Installation

To install the RDK into your computer, please refer to your computer's instruction manual for the correct preparation and installation of add-in cards.

Note: The 9052RDK-Lite card edge connector is constructed using Universal keying (as shown in PCI Specification r2.1, Figure 5-28) which allows insertion into either a 3.3V or 5V PCI slot, rather than being keyed for use only in a 5V slot. Because the PCI 9052 generates 5V signaling, operation in a 3.3V system could damage devices on the bus that are not 5V-tolerant. The RDK will not damage systems that use 5V keyed or universal keyed slots but extreme care should be taken if the RDK is plugged into a system that is only keyed for 3.3V operation.

2. PCI 9052 Overview

2.1 PCI 9052 Introduction

The PLX PCI 9052 provides a compact, high-performance PCI bus target (slave) interface for adapter boards. It is designed to connect a wide variety of local bus designs to the PCI bus and allow them to achieve high data rate burst transfers on the PCI bus.

The PCI 9052 can be programmed to connect directly to an 8- or 16-bit local ISA bus as well as to 8-, 16-, or 32-bit multiplexed or non-multiplexed local busses.

The PCI 9052 contains read and write FIFOs to speed-match a 32-bit wide, 33 MHz PCI bus to a local bus, which may be a different width and/or speed. Up to five local address spaces and up to four local chip selects are supported.

2.2 PCI 9052 Feature Set

- **PCI v2.1 compliance:** The PCI 9052 is compliant with PCI Specification v2.1, supporting low cost slave adapters. It facilitates the simple conversion of ISA adapters to PCI target adapters.
- **Direct slave (Target) data transfer mode.** The PCI 9052 supports burst memory-mapped and single-cycle I/O mapped accesses from the PCI bus to the local bus. The read and write FIFOs enable high performance bursting on the local and PCI bus. When the PCI bus is bursting, the local bus can either perform burst accesses or multiple single-cycle accesses.
- **Interrupt generator.** The PCI 9052 can generate a PCI interrupt from two local bus interrupt inputs or by software writing to an internal register bit.
- **Clock.** The PCI 9052 local bus runs from a local TTL clock and generates necessary internal clocks. This clock runs asynchronously to the PCI clock allowing the local bus to be run at an independent rate. The buffered PCI bus clock output (BCLKO) may be connected to the local bus clock (LCLK) input through a 50-Ohm series resistor if desired.
- **Programmable local bus configurations.** The PCI 9052 supports 8-, 16-, or 32-bit local buses, which may be multiplexed or non–multiplexed. The PCI 9052 has four byte enables (LBE[3:0]#), 26 address lines (LA[27:2]) and up to 32 data lines (LAD[31:0]).
- **Read ahead mode.** The PCI 9052 supports Read Ahead mode, where pre-fetched data can be read from the PCI 9052 internal FIFO instead of from the local bus. Addresses must be sequential and 32-bit aligned (next address = current address +4).
- **Bus drivers.** All control, address and data signals generated by the PCI 9052 drive the PCI and local buses, without the need for external drivers.
- **Serial EEPROM interface.** The PCI 9052 contains a serial EEPROM interface, used to load configuration information. This is useful for loading information unique to a particular adapter (such as Device ID, Vendor ID, and local bus configuration information).
- **Four local chip selects.** The PCI 9052 provides up to four local bus chip selects (CS[3:0]#). The base address and range of each are independently programmable from the serial EEPROM or host.
- **Five local address spaces.** The base address, range, bus width and timing of each local address space are independently programmable from the serial EEPROM or host.
- **Big/Little Endian byte swapping.** The PCI 9052 supports local bus Big and Little Endian byte ordering. The PCI 9052 also supports Big Endian byte lane mode to redirect the current word/byte lane during 16- or 8-bit local bus operation.

- **Read/write strobe delay and write cycle hold.** Read and Write (RD# and WR#) signals can be delayed from the beginning of a local bus cycle to allow the local bus timing to be tailored to the requirements of specific peripherals. The Write Cycle Hold option extends the data valid time for additional clock cycles beyond WR# strobe de-assertion.
- **Local bus wait states.** In addition to the LRDY# (local ready input) handshake signal for variable wait state generation, the PCI 9052 has an internal wait state generator to allow the local bus timing to be tailored to the requirements of specific peripherals. Wait states may be inserted to adjust the R/W address to data, R/W data to data and R/W data to address times.
- **Programmable pre-fetch counter.** The local bus pre-fetch counter can be programmed for 0 (no pre-fetch), 4, 8, 16 or Continuous Pre-fetch Mode (pre-fetch counter turned off). The pre-fetched data can be used as cached data if consecutive long-word aligned addresses are read.
- **PCI Read/Write request timeout timer.** The PCI 9052 has a programmable PCI Target Retry Delay Timer, which when expired, generates a RETRY to the PCI bus.
- **On-chip ISA interface logic.** The PCI 9052 local bus supports single cycle reads/writes for 8- or 16-bit Memory and I/O access cycles on the ISA bus. Local Address Space 0 is used for ISA Memory space accesses and Local Address Space 1 is used for ISA I/O space accesses.
- **PCI LOCK mechanism.** The PCI 9052 supports PCI target LOCK sequences. A PCI master can obtain exclusive access to the PCI 9052 device by locking to the PCI 9052.

3. RDK Hardware Architecture

3.1 Architecture Overview

A block diagram of the PCI 9052RDK-LITE board is shown in Figure 3-1. The board is designed to support the product development of 32-bit, 33 MHz PCI target adapters. It features a PLX PCI 9052 device that interfaces user logic to a 32-bit, 33 MHz PCI bus. An on-board serial EEPROM contains the data that is loaded into the PCI 9052 configuration registers during board boot-up. A socketed 32 MHz oscillator drives the local bus side of the RDK. The local bus can be programmed to operate as an 8- or 16-bit ISA bus, or as an 8-, 16-, or 32-bit multiplexed or non-multiplexed address/data bus. A glue-less ISA bus connector is provided on the board to facilitate the rapid conversion of ISA bus designs to PCI bus designs. An unpopulated 512KB 8-bit wide ROM socket is provided for memory expansion. The board supports continuous PCI 9052 burst read/write accesses to 128 Kbytes of SRAM provided in a 32-bit wide format. An inexpensive 64-macrocell CPLD is used to generate various control signals for the RDK board. While not required to interface the PCI 9052 to the ISA bus, using a small CPLD makes the RDK as flexible as possible as a development platform. Additional logic capacity is available in the CPLD for prototyping. The local bus is brought out to test headers to facilitate the debugging of user designs. A large prototyping area is provided as well.

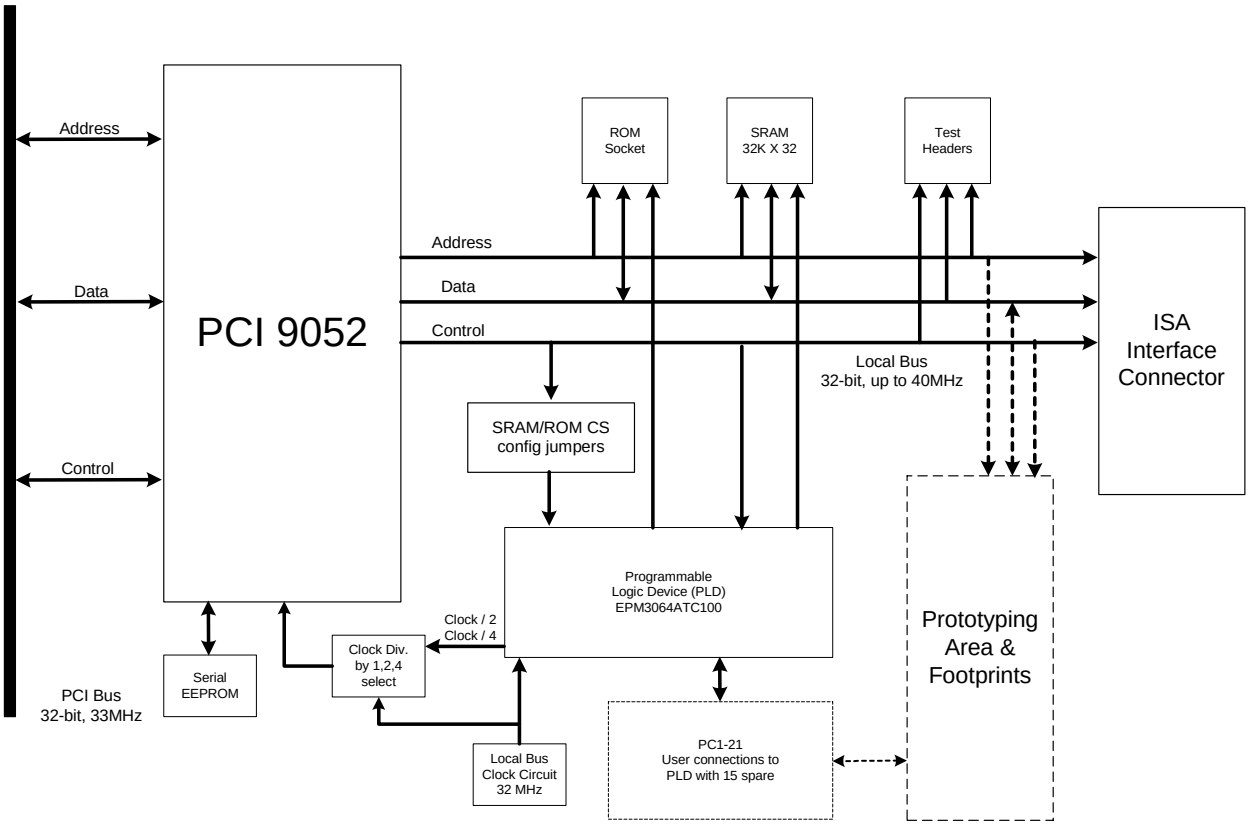


Figure 3-1. PCI 9052RDK-LITE Hardware Block Diagram

3.2 Hardware Memory Map

Table 3-1. PCI 9052RDK-LITE Default Memory Map

Address Range	Device	Chip Select	Comments
0FFF FFFF 0300 0000	Unused	Unused	Unused
020F FFFF 0200 0000	ROM Socket	CS3#	
0101 FFFF 0100 0000	SRAM	CS2#	
000F FFFF 0000 0000	ISA Memory space	CS0# & CS1#	In ISA mode the CS0# & CS1# pins are redefined as MEMRD# and MEMWR#, respectively
0000 000F 0000 0000	ISA I/O space		

The address range over which each CSn# is active can be changed by reprogramming the on-board serial EEPROM. Refer to Table 3-2 Serial EEPROM Contents for a description of the PCI 9052 address space registers. The SRAM and ROM chip selects can be driven by any PCI 9052 chip select signal. Refer to Table 3-4 Configuration Jumper Settings to choose a different chip select signal for ROM and SRAM accesses.

3.3 Serial EEPROM

A 1Kbit serial EEPROM is used for RDK board configuration and PCI 9052 initialization. The serial EEPROM is connected to the PCI 9052 without any glue logic. The preprogrammed data in the EEPROM is used to configure the RDK board during boot up. The data includes device and functional information for plug-and-play (PnP), PCI memory resource allocation and initial values of PCI 9052 internal registers. Once the RDK initialization is completed, designers can use PLXMon® to change the contents in the serial EEPROM or reprogram it with user defined data files.

If the Local Clock (LCLK) frequency is set to 8 MHz (JP1[1:2]), rather than to 16-, 32-, or 33-MHz, a programmed serial EEPROM is required in order to boot the system. If the serial EEPROM is either missing or blank, PCI 9052 default register values are loaded, and these values enable Expansion ROM memory and disable delayed reads. At boot time, the BIOS will access the Expansion ROM space; however, with LCLK at 8 MHz, the PCI 9052RDK-Lite cannot complete the Expansion ROM access prior to expiration of the Retry Delay Clocks counter. With the programmed EEPROM, the Expansion ROM request is disabled and delayed reads are enabled to allow booting at reduced LCLK frequency.

Table 3-2. Serial EEPROM Contents

Serial EEPROM Offset	Register Offset	Register Description	Register Bits Affected	Register Values	Register Value Description
00h	PCI 02h	Device ID	PCIIDR [31:16]	5201	Device ID for PCI 9052RDK-LITE
02h	PCI 00h	Vendor ID	PCIIDR [15:0]	10B5	PLX Vendor ID
04h	PCI 0Ah	Class Code	PCICCR [23:8]	0680	Other bridge type
06h	PCI 08h	Class Code / Revision	PCICCR [7:0] / PCIREV [7:0]	0002	PCIREV = current 9052 revision
08h	PCI 2Eh	Subsystem ID	PCISID [15:0]	9050	Default 9052 Subsystem ID
0Ah	PCI 2Ch	Subsystem Vendor ID	PCISVID [15:0]	10B5	PLX Subsystem Vendor ID
0Ch	PCI 3Eh	(Maximum Latency and Minimum Grant are not loadable)	***Reserved***	0	
0Eh	PCI 3Ch	Interrupt Pin / (Interrupt Line Routing is not loadable)	PCIIPR [7:0] / PCIILR [7:0]	0100	Interrupt pin = INTA#
10h	Local 02h	MSW of Range for PCI-to-Local Address Space 0	LAS0RR [31:16]	FFF0	1MB local address space for the ISA Memory space access, mapped into PCI memory space.
12h	Local 00h	LSW of Range for PCI-to-Local Address Space 0	LAS0RR [15:0]	0000	
14h	Local 06h	MSW of Range for PCI-to-Local Address Space 1	LAS1RR [31:16]	FFFF	16-byte local address space for the ISA I/O space access, mapped into PCI I/O space.
16h	Local 04h	LSW of Range for PCI-to-Local Address Space 1	LAS1RR [15:0]	FFF1	
18h	Local 0Ah	MSW of Range for PCI-to-Local Address Space 2	LAS2RR [31:16]	FFFE	128KB local address space for the RDK memory mapped SRAM, mapped into PCI memory space.
1Ah	Local 08h	LSW of Range for PCI-to-Local Address Space 2	LAS2RR [15:0]	0000	
1Ch	Local 0Eh	MSW of Range for PCI-to-Local Address Space 3	LAS3RR [31:16]	FFF0	1MB local address space for the RDK memory mapped ROM, mapped into PCI memory space.
1Eh	Local 0Ch	LSW of Range for PCI-to-Local Address Space 3	LAS3RR [15:0]	0000	
20h	Local 12h	MSW of Range for PCI-to-Local Expansion ROM	EROMRR [31:16]	0	No Expansion ROM range set
22h	Local 10h	LSW of Range for PCI-to-Local Expansion ROM	EROMRR [15:0]	0	
24h	Local 16h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA [31:16]	0000	This space is active from local address 0 for ISA Memory space accesses.
26h	Local 14h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA [15:0]	0001	
28h	Local 1Ah	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA [31:16]	0000	This space is active from local address 0 for ISA I/O space accesses.
2Ah	Local 18h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA [15:0]	0001	
2Ch	Local 1Eh	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 2	LAS2BA [31:16]	0100	This space is active from local address 01000000h for RDK SRAM accesses.
2Eh	Local 1Ch	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 2	LAS2BA [15:0]	0001	
30h	Local 22h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 3	LAS3BA [31:16]	0200	This space is active from local address 02000000h for RDK ROM accesses.
32h	Local 20h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 3	LAS3BA [15:0]	0001	
34h	Local 26h	MSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA [31:16]	0000	No Expansion ROM enabled – see EROMRR
36h	Local 24h	LSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA [15:0]	0000	

Serial EEPROM Offset	Register Offset	Register Description	Register Bits Affected	Register Values	Register Value Description
38h	Local 2Ah	MSW of Bus Region Descriptors for Local Address Space 0	LAS0BRD [31:16]	0040	Sets bus width to 16 for ISA Memory space accesses. No prefetching.
3Ah	Local 28h	LSW of Bus Region Descriptors for Local Address Space 0	LAS0BRD [15:0]	0022	
3Ch	Local 2Eh	MSW of Bus Region Descriptors for Local Address Space 1	LAS1BRD [31:16]	0000	Sets bus width to 8 for ISA I/O space accesses. No prefetching.
3Eh	Local 2Ch	LSW of Bus Region Descriptors for Local Address Space 1	LAS1BRD [15:0]	0022	
40h	Local 32h	MSW of Bus Region Descriptors for Local Address Space 2	LAS2BRD [31:16]	0080	Enables bursting & sets bus width to 32 for RDK SRAM. Prefetch enabled.
42h	Local 30h	LSW of Bus Region Descriptors for Local Address Space 2	LAS2BRD [15:0]	0001	
44h	Local 36h	MSW of Bus Region Descriptors for Local Address Space 3	LAS3BRD [31:16]	5421	Sets timing & bus width to 8 for RDK ROM. Burst enabled, Prefetch enabled, Prefetch count=1, NRAD=3, NRDD=3, NXDA=1, NWAD=2, NWDD=2, RSD=1, WSD=1, WCH=1
46h	Local 34h	LSW of Bus Region Descriptors for Local Address Space 3	LAS3BRD [15:0]	38E9	
48h	Local 3Ah	MSW of Bus Region Descriptors for Expansion ROM	EROMBRD [31:16]	0	No Expansion ROM enabled
4Ah	Local 38h	LSW of Bus Region Descriptors for Expansion ROM	EROMBRD [15:0]	0	
4Ch	Local 3Eh	MSW of Chip Select (CS) 0 Base and Range	CS0BASE [31:16]	0008	As a default this CS is not active as its pin is used as an ISA bus signal. The local address range is set from 00000000 to 000FFFFFh to allow correct ISA Memory space accesses.
4Eh	Local 3Ch	LSW of Chip Select (CS) 0 Base and Range	CS0BASE [15:0]	0001	
50h	Local 42h	MSW of Chip Select (CS) 1 Base and Range	CS1BASE [31:16]	0000	As a default this CS is not active as its pin is used as an ISA bus signal. The local address range is set from 00000000 to 0000000Fh to allow correct ISA I/O space accesses.
52h	Local 40h	LSW of Chip Select (CS) 1 Base and Range	CS1BASE [15:0]	0009	
54h	Local 46h	MSW of Chip Select (CS) 2 Base and Range	CS2BASE [31:16]	0101	This CS is active from local address 01000000 to 0101FFFFh for RDK SRAM
56h	Local 44h	LSW of Chip Select (CS) 2 Base and Range	CS2BASE [15:0]	0001	
58h	Local 4Ah	MSW of Chip Select (CS) 3 Base and Range	CS3BASE [31:16]	0208	This CS is active from local address 02000000 to 020FFFFFh for RDK ROM
5Ah	Local 48h	LSW of Chip Select (CS) 3 Base and Range	CS3BASE [15:0]	0001	
5Ch	Local 4Eh	MSW of Interrupt Control/Status Register	INTCSR [31:16]	0000	Local interrupt 1 enabled, active high level sensitive. Local interrupt 2 enabled, active high level sensitive. ISA mode.
5Eh	Local 4Ch	LSW of Interrupt Control/Status Register	INTCSR [15:0]	115B	
60h	Local 52h	MSW of Serial EEPROM, control and miscellaneous control register	CNTRL [31:16]	007C	CS and User pin configuration, ISA I/O pin configuration, CS2 & CS3 active, RDK occupies PCI memory & I/O space, PCI 2.1 features enabled, PCI Write release enabled, PCI Direct Slave Retry Delay = Fh.
62h	Local 50h	LSW of Serial EEPROM, control and miscellaneous control register	CNTRL [15:0]	4252	

3.4 Local Bus Operating Modes

The PCI 9052 local bus can be programmed to operate in 8- or 16-bit ISA bus mode, 8-,16-, or 32-bit non-multiplexed address/data bus mode (C-Mode) or 8-, 16-, or 32-bit multiplexed address/data bus (J-Mode). Programming of the PCI 9052 local bus operation is controlled by the value on the device's MODE pins and INTCSR[12] during power-up.

Byte and word local bus accesses are supported in ISA mode, allowing the bus to be populated with 8- and 16-bit wide devices. Byte, word and long word access are supported in C-Mode and J-Mode, allowing the bus to be populated with 8-, 16-, and 32-bit wide devices. The local bus ROM and SRAM can be accessed in all operating modes.

The board ships in ISA mode, allowing customers to connect their own ISA cards to the PCI 9052RDK-LITE. This facilitates the rapid conversion of ISA bus designs to PCI bus designs. Refer to Table 3-4 Configuration Jumper Settings to reconfigure the local bus operating mode. When operating in ISA mode, Local Address Spaces 0 and 1 are used for ISA memory and ISA I/O accesses respectively and the local bus control signals reflect this. However, any accesses to Local Address Spaces 2 and 3 will result in a normal C mode transaction on the local bus. If Local Address Spaces 2 and 3 are disabled then only the ISA interface is available on the local bus.

3.4.1 ISA Interface

The PCI 9052RDK-LITE board includes a single ISA socket to allow ISA cards to be accessed via the PCI bus. The PCI 9052 is connected to this socket without any glue logic. If the designer has an existing ISA card design that needs to be migrated to PCI, the designer can plug the existing ISA card into the ISA socket on the RDK and immediately begin developing software on a familiar hardware platform.

The reader should note that there are a few minor exceptions to ISA compatibility. The PCI 9052RDK-LITE board does not provide –5V to the ISA interface connector. Also, the PCI 9052 does not support ISA mastering nor ISA DMA operations.

Later in the development cycle, when designing the new PCI card hardware, the designer can choose whether to use the 'ISA' mode of the local bus or the multiplexed or non-multiplexed modes. The standard multiplexed and non-multiplexed PCI 9052 local bus modes are very simple to interface to and may result in a much simpler solution than using the ISA mode of the local bus and ISA interface logic from the original ISA card.

3.5 Static RAM (SRAM)

Four 5V, 9ns, 32Kx8 Static RAMs (U7, U10, U15 and U16) are used on the RDK board. The SRAM is accessible through the local bus. By default, CS2# is used to access the SRAM but the RDK can be configured by JP2 to use any CS# for the SRAM socket. Refer to Table 3-4 Configuration Jumper Settings to use another chip select signal to access the SRAM.

The SRAM can also be accessed by a local bus master by driving the XCSRAM# signal on the CPLD (prototyping pad PC6) in conjunction with the local bus address, data, control and bus arbitration signals.

The PLXMon software can be used to read and write the SRAM. Refer to the PLXMon User's Manual on the SDK CD-ROM for more details. PLXMon allows the designer to view and modify data contents without writing any code.

3.6 ROM Socket

A 32-pin PLCC socket is provided on the RDK. This can be used to install a 3.3V or 5V, 512Kx8 ROM or Flash ROM memory device for storing code, either for an expansion ROM or to boot a microprocessor. The socket is pre-connected to address, data and control lines, GND & VCC. By default, CS3# is used to access the ROM socket but the RDK can be configured by JP2 to use any CS# for the ROM socket. Refer to Table 3-4 Configuration Jumper Settings to use another chip select signal to access the SRAM.

The ROM can also be accessed by a local bus master by driving the XCSROM# signal on the CPLD (prototyping pad PC7) in conjunction with the local bus address, data, control and bus arbitration signals.

Note: When a 3.3V device is used in the ROM socket, please make sure it has 5V-tolerant I/O.

3.7 Test Headers

Six logic analyzer headers are implemented with the standard 0.1", 2x10 Hewlett Packard configuration. These headers can be used for signal probing or prototype area expansion. All PCI 9052 local bus, configuration and status signals are well arranged within these headers. Headers LAH1 and LAH2 contain local bus address signals. Headers LAH3 and LAH4 contain local bus data signals (or multiplexed address/data signals in the multiplexed mode). Headers LAH5 and LAH6 contain local bus control and status signals. Designers can use these headers to connect to a standard prototyping board for additional prototyping. The headers do not provide any power source; therefore, VCC must be connected separately for prototyping daughter-boards.

3.8 CPLD Functionality

The PCI 9052RDK-LITE includes an Altera EPM3064ATC100 CPLD (U5). This CPLD is used to generate various control signals for the RDK board. While not required to interface the PCI 9052 to the ISA bus, using a small CPLD makes the RDK as flexible as possible as a development platform. It performs the following functions:

- Clock division to generate 16 MHz and 8 MHz signals for LCLK
- Memory strobe generation
- ORing of multiple ISA IRQ lines to generate a single interrupt, minimizing the number of jumpers that would be required to route multiple IRQ lines to the PCI 9052 LINTi1 local interrupt pin
- Logic to allow optional local bus masters to access the on-board memory

The rest of the device (over 50%) is available to the user for prototyping purposes. There are 15 spare pins on the CPLD connected to prototyping pads PC1 and PC8-PC21 for linking to other components or local bus signals.

The CPLD can easily be reprogrammed via the JTAG ISP header J7. The design is provided on the HDK CD-ROM in the Altera® MAX+PLUS® II graphic design file (.gdf) format. The easiest way to customize the PLD design is to import the .gdf file into the MAX+PLUS II software and modify the design. The MAX+PLUS II Baseline version is available free of charge from Altera. Please refer to the Altera website (www.altera.com) or contact an Altera representative for further details.

For a graphical representation of the program contained within the CPLD, refer to the schematics contained later in this manual.

3.9 Prototyping Area

The RDK board contains a large prototyping area that contains 28 surface mount footprints, one 0.05" pitch BGA landscape, a 25x25 0.1" grid through-hole prototyping area and 5 power rails.

Table 3-3. PCI 9052RDK-LITE Board Prototyping Area Footprints

Package	Qty.	Width & Pitch	Destination	Comments
32-pin PLCC	1	0.05" pitch	FP1	Populated with PLCC socket
84-pin PLCC	1	0.05" pitch	FP2	FP2 to FP5 co-exist at an 84-pin PLCC area
68-pin PLCC	1	0.05" pitch	FP3	
44-pin PLCC	1	0.05" pitch	FP4	
28-pin PLCC	1	0.05" pitch	FP5	
20-pin PLCC	1	0.05" pitch	FP6	
16-pin SOIC narrow	4	.150"wide, 0.05" pitch	FP7, 8, 15, 16	
54-pin TSOP	2	0.8mm pitch	FP9, 10	
48-pin SSOP	2	.300"wide, 0.025" pitch	FP23, 24	
20-pin SOIC wide	4	.300"wide, 0.05" pitch	FP17, 18,19,20	
24-pin SSOP	2	.150"wide, 0.025" pitch	FP21, 22	
44-pin TQFP	1	0.8mm pitch	FP25	
16-Pin SSOP	2	.150" wide, 0.025" pitch	FP26, 27	
208-pin PQFP	1	0.5mm pitch	FP28	FP28, 29, 30 co-exist in a 208-pin PQFP area
144-pin TQFP	1	0.5mm pitch	FP29	
80-pin TQFP	1	0.5mm pitch	FP30	
176-pin PQFP	1	0.5mm pitch	FP31	FP31, 32,33 co-exist in a 176-pin PQFP area
100-pin TQFP	1	0.5mm pitch	FP32	
48-pin TQFP	1	0.5mm pitch	FP33	
26x26 BGA matrix	1	0.05" pitch		
25x25 0.1" through hole area				
2 @ 1x30 0.1" through hole rails for 3.3VCC				
2 @ 1x30 0.1" through hole rails for GND				
1 @ 1x30 0.1" through hole rail for 5VCC				

3.9.1 BGA Prototyping

This RDK features a 26x26 @ 0.05” pitch BGA landscape with a plated-hole size of 0.022” diameter +/- 0.001”. Users can prototype with BGA devices by using BGA to PGA adapters.

Referring to Figure 3-2, designers can use one of two methods to prototype with BGA devices. Both methods require soldering the BGA device to a BGA Land Socket. The Land Socket can then be soldered directly to the PC board or, optionally, a Minigrid Socket can be soldered to the board and the Land Socket plugged into the Minigrid Socket.

These sockets are available from Ironwood Electronics (web site: www.ironwoodelectronics.com).

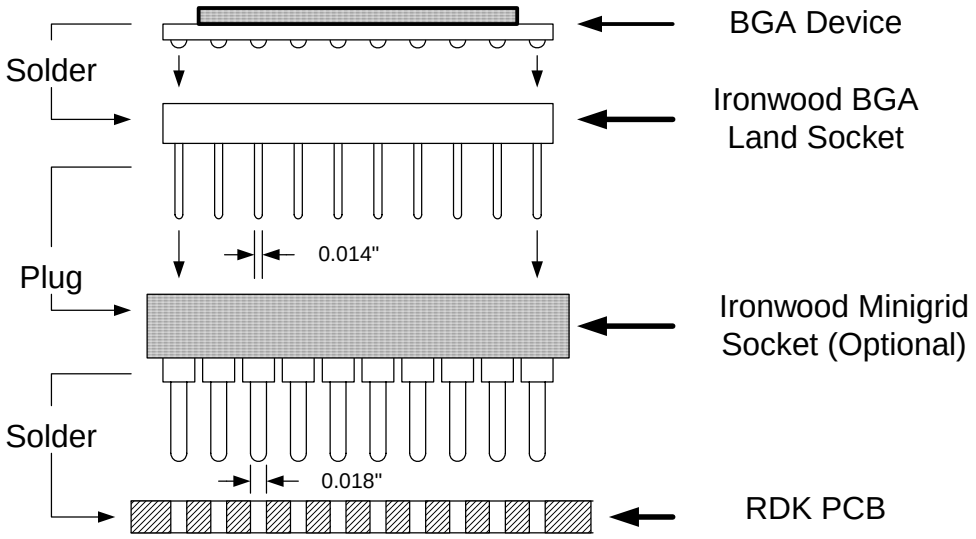


Figure 3-2. BGA to PGA Conversion

3.10 RDK Board Configuration

Table 3-4 Configuration Jumper Settings explains how to set the jumpers to configure the board. An “X” in the Default Jumper column denotes the default jumper setting. The serial EEPROM is programmed to enable Space 0 and Space 1 to operate in ISA mode by default.

Table 3-4. Configuration Jumper Settings

Function	Option	Jumper Location	Jumper Setting	Jumper Default
Local Bus Operation	ISA [1]	JP5	2-3	X
	Non-Multiplexed		2-3	
	Multiplexed		1-2	
Local Interrupt 1 (LINTi1) Termination	LINTi1 Active High	JP3	2-3	X
	LINTi1 Active Low		1-2	
Local Interrupt 2 (LINTi2) Termination	LINTi2 Active High	JP4	2-3	X
	LINTi2 Active Low		1-2	
Local Interrupt 1 (LINTi1) Routing	ISA_INT to LINTi1	JP1	9-10	X
	XINT1 to LINTi1		11-12	
	CHCHK# to LINTi1		13-12	
	XINT2 to LINTi1		15-12	
Local Interrupt 2 (LINTi2) Routing	ISA_INT to LINTi2	JP1	9-14	
	XINT1 to LINTi2		11-14	
	CHCHK# to LINTi2		13-14	
	XINT2 to LINTi2		15-16	
Local Clock Source	BCLKo	JP1	7-8	X
	8 MHz		1-2	
	16 MHz		3-4	
	32 MHz		5-6	
Chip Select Routing	CS0# to CSRAM#	JP2	1-10	
	CS0# to CSROM#		1-14	
	CS1# to CSRAM#		5-10	
	CS1# to CSROM#		5-14	
	CS2# to CSRAM#		9-10	X
	CS2# to CSROM#		9-14	
	CS3# to CSRAM#		13-10	
	CS3# to CSROM#		13-14	X
ROM Socket VCC	Vcc = 5 V	JP6	1-2	
	Vcc = 3.3 V		2-3	
NOWS# Delay	Disabled	JP7	1-2	X
	Enabled		2-3	

Note 1. ISA Mode is selected by setting Jumper JP5 2-3 and programming INTCSR[12]=1 in the EEPROM. The board ships with INTCSR[12]=1.

Note 2. If the jumper between pins 9 and 10 of JP2 is removed, the CSRAM# input to the CPLD will be floating without an external pull-up resistor. That may cause the CPLD to generate incorrect RCS[3:0]# chip select signals to the local bus SRAM. Similarly, if the jumper between pins 13 and 14 of JP2 is removed, the CSROM# input to the CPLD will be floating without an external pull-up resistor. That may cause the CPLD to generate an incorrect CSROMO# chip select signal to the Local bus ROM socket.

Note 3. When operating the 9052 with local clock below 16MHz (for example 8MHz) ensure that either CNTRL[14]=1 and/or CNTRL[22:19]=Fh in the EEPROM. Failure to do so may result in the card failing to boot in some systems.

4. ISA to PCI Migration

This chapter explains how to use the PCI 9052RDK-LITE to migrate ISA bus designs to PCI bus designs.

4.1 ISA Register Configuration

The PCI 9052 uses a re-mapping process to map an ISA card into PCI space. Local address spaces 0 and 1 are used for memory accesses and I/O space accesses, respectively. During boot up, the PC BIOS reads the amount of memory or I/O space requested by the PCI 9052 and allocates this within the PCI memory map. The base addresses of the various regions are written back into the PCIBAR registers.

4.1.1 Range Register

The Range Registers LAS0RR and LAS1RR are used to store memory range and I/O space range, respectively. In order to allocate the correct amount of memory in PCI, the two's complement of the amount of ISA memory and/or ISA I/O space required is stored into the appropriate LASxRR registers. The range for a local address space must be a power of 2. In addition, the least significant bit of the LAS1RR register must be set to 1 to ensure it is mapped into the I/O space.

4.1.2 Base Address Re-map Register

The Base Address Re-map Registers LAS0BA and LAS1BA are used to store ISA card memory and I/O base addresses, respectively.

To enable a local address space, and allow it to be mapped into PCI space, LASxBA register bit-0 should be set to "1". If only I/O space is required, then it is not necessary to enable LAS0BA register bit-0.

The base address programmed into the LASxBA register must be a multiple of the appropriate range or 0. This restriction may require lowering the base address and increasing the range to ensure that both the ISA base address and range are covered.

4.1.3 Chip Select Register

The Chip Select Registers CS0BASE and CS1BASE should be configured to map directly over Local Address Spaces 0 and 1, respectively.

There are several descriptions in the PCI 9052 data book and on the PLX web site (www.plxtech.com) explaining how to program the CSxBASE registers. For occasional use the simplest method is to write the powers of 2 down on a sheet of paper, placing 1's in the appropriate places and then converting this to a hex number. For example, if you wanted a chip select with a range of 16 bytes and a base address of 0x100h, then you would do the following:

1. Place a 1 in bit 0 (to enable the chip select).
2. Place a 1 in the column immediately to the right of the range required. In this example, the required range is 16; therefore a 1 is placed in the 8 column.
3. Set the appropriate bits for the base address to the left of the range bit. In this example, the desired base address is 0x100h, therefore a 1 is placed in the 256 column. The completed table should look like this:

2048	1024	512	256	128	64	32	16	8	4	2	1
0	0	0	1	0	0	0	0	1	0	0	1

4. Convert the binary value to hex. In this example the CSxBASE register would be loaded with 0x00000109h

Using this method will always force the base address to be a multiple of the range.

4.2 ISA Register Configuration Example

Assume that the ISA card requires 1K bytes of memory space starting at address 0x1000h on the ISA bus and 16 bytes of I/O space starting at address 0x308h.

4.2.1 ISA Memory Mapping

Starting with the memory space first, LAS0RR must be set to the inverse of the 1K bytes. 1K is 0x3ffh (if location 0 is included), the inverse is 0xfffffc00h and this is the number to be placed into LAS0RR.

The base address required (0x1000h) is a multiple of the range so there is no need to modify it or the range. The LAS0BA register is set to 0x00001001h - remember to set the least significant bit to 1 to enable the local address space.

4.2.2 ISA I/O Mapping

For the I/O space things are a little more complicated. The base address in this example is not a multiple of the range. Therefore, to ensure that the I/O space of the card is covered, reduce the base address value and increase the range to compensate. [When migrating the design from ISA to PCI, reducing or removing the decoding such that the base address starts at 0 would simplify the register settings and the design considerably.]

Lower the base address to 0x300h. Therefore, the LAS1BA register must be set to 0x00000301h.

To ensure that the adapter's I/O range is covered (0x308h to 0x317h), increase the range to 32 bytes i.e. 0x1fh. Therefore, the LAS1RR register is set to 0xfffffffe1h. The least significant bit is set to map Local Address Space 1 into I/O space.

4.2.3 Chip Select Configuration

Now set up the chip select registers. The CS0BASE register has to be set to cover the memory-mapped region in Local Address Space 0. Based on the method described in section 4.1.3, the CS0BASE register value should be 0x00001201h. Similarly, the CS1BASE register has to cover the I/O-mapped region set up in Local Address Space 1. The value for CS1BASE should be 0x00000311h.

4.2.4 Other Local Settings

4.2.4.1 Bus Region Descriptor

The Bus Region Descriptor registers LAS0BRD and LAS1BRD can be used to select either 8- or 16-bit ISA operation. For 8-bit ISA operation, the LASxBRD registers should be set to 0x00000022h; for 16-bit ISA operation, the LASxBRD registers should be set to 0x00400022h.

If pre-fetching is not required, it can be disabled by enabling the pre-fetch counter (LASxBRD[5]=1) and setting the counter to 0 (LASxBRD[4:3]=00b). e.g. LASxBRD should be set to 0x00000022h for 8-bit ISA operation with pre-fetching disabled.

Pre-fetching can be used to improve the read data transfer rate, especially if this is combined with "PCI Read No Flush mode" (CNTRL[16]=1). However, care should be taken to ensure that prefetching is only used when reading from devices with non-volatile data - such as memory devices. If prefetching is used when connected to devices with volatile data – such as a FIFO – then a single cycle read may result in multiple accesses to the FIFO. This may result in the loss of data if a PCI Initiator reads from non-sequential addresses. If there is any doubt about the volatility of the data on the ISA card then prefetching should be disabled. By default, the PCI 9052RDK-LITE has pre-fetching disabled for accesses to ISA Memory regions. It will never pre-fetch from ISA I/O regions.

4.2.4.2 Initialization Control Register

The Initialization Control Register CNTRL must be set to 0x007X0X12h where X represents the appropriate values for the specific adapter. For PCI v2.1 compatible systems, set CNTRL[18] = 0 and CNTRL[14] = 1, in which case CNTRL[22:19] become Don't Cares.

4.2.4.3 Interrupt Control/Status Register

The Interrupt Control/Status Register bit (INTCSR[12]) must be set to 1 to enable ISA interface mode. If interrupts are desired, enable the appropriate local interrupts in the INTCSR register and also enable the PCI interrupt (INTCSR[6]).

4.2.5 Interrupts

PCI interrupt lines are allocated in a different manner to ISA interrupt lines (IRQs). On ISA cards there are jumpers to select the appropriate IRQ for the application. In single function PCI devices there is only one interrupt, INTA#, and it may be shared among other PCI devices. To allow the ISA card to generate PCI interrupts, route the ISA card IRQ to one of the PCI 9052 local interrupt input (LINTix) pins. Once the INTCSR register has been enabled, the active high assertion of the local interrupt will generate the PCI INTA# signal.

LINTix pins should not be left floating. A pull up or pull down resistor should be used to pull the interrupt to its inactive state and ensure that the interrupt is not generated before the driver is loaded.

4.2.6 Serial EEPROM

A serial EEPROM is required when using the PCI 9052 in ISA mode. The EEPROM must be used to set all the local registers mentioned above. The PCI 9052 will not function in ISA mode unless a correctly programmed EEPROM is present.

4.2.7 PCI Access to Local ISA Bus

PCIBAR 0 and 1 are the addresses of the PCI 9052 registers in the PCI memory and I/O spaces, respectively. PCIBAR 2 and 3 are the addresses in the PCI memory and I/O spaces that are mapped to the ISA memory and I/O spaces, respectively.

Taking the example used before:

Local address space 0 = memory mapped from 0x00001000h to 0x000013ffh

Local address space 1 = I/O mapped from 0x00000300h to 0x0000031fh

Assume that the BIOS places the following values in the PCIBARs;

PCIBAR2 = 0xffcf0000h

PCIBAR3 = 0x0000fc01h

An access to address 0xffcf0014h will then result in an access on the local bus at location 0x00001014h.

However, Windows uses virtual memory addressing. If Windows software such as PLXMon is used, then the designer will have to know the Windows address that maps to the appropriate physical PCI address. PLXMon provides predefined variables that tell the user the appropriate Windows address. For example, the variable *s0* refers to Local Address Space 0. To read a byte from Local Address Space 0 with an offset of 8 bytes from the base, type the following in the lower pane of PLXMon:

db s0 +8

A complete list of variables can be obtained by typing *vars* in the lower pane of PLXMon. Refer to the PLXMon User's Manual for more information.

The I/O space is a little more complicated. The least significant bit in PCIBAR3 is only used to show that this location exists in I/O space. Therefore, the real base address is 0x0000fc00h, not 0x0000fc01h. In the original example the I/O region base was lowered and the range increased because the original base

address was not a multiple of the range. The I/O region for the ISA device was from 0x308h to 0x317h. To write to the first I/O location in the ISA card, care has to be taken. An access to location 0x0000fc08h will map to location 0x308h on the local bus.

When accessing the I/O space, remember to use I/O read and write commands, not memory reads and writes.

4.3 ISA NOWS# Delay Option

ISA protocol allows zero wait state operation for 16-bit memory only. At least one wait state is required for 16-bit I/O accesses and all 8-bit accesses. However, the PCI 9052 can support zero wait states for all accesses.

ISA protocol uses the ISA card's NOWS# output to reduce the number of wait states (from the default of four wait states for 8-bit transfers or one wait state for 16-bit transfers). During 16-bit memory accesses, the protocol specifies that the NOWS# output is sampled halfway through the first data valid time, permitting zero wait state operation. During 16-bit I/O accesses, the protocol specifies that the NOWS# output be ignored, thus 16-bit I/O cycles have one wait state. During 8-bit accesses, the protocol specifies that the NOWS# output is sampled halfway through the *second* data valid time as well as halfway through each subsequent data valid time, thus at least one wait state is inserted into each 8-bit access.

The PCI 9052 samples its NOWS# input halfway through the first data time and halfway through each subsequent data time *for all accesses*. This allows all accesses to be truly "zero wait state" even though ISA protocol allows zero wait state transfers for 16-bit memory accesses only. Sampling of NOWS# during the first data time may cause conflict with ISA designs that expect the signal to be first sampled during the second data time for all 8-bit accesses, or which expect NOWS# to be ignored during 16-bit I/O accesses.

Usually there is no conflict, as ISA designs typically generate NOWS# from the command strobe along with the address, and the PCI 9052 command strobe assertion occurs after the first NOWS# sampling for 16-bit I/O and all 8-bit accesses.

If there is a conflict, the CPLD can be used to delay the assertion of the PCI 9052 NOWS# input by one clock cycle, ensuring that at least one wait state is inserted into all accesses, even formerly zero wait state memory accesses.

The delay circuit is enabled by moving jumper JP7 from 1-2 to 2-3, as shown in Table 3-4 Configuration Jumper Settings. Before configuring the NOWS# delay, determine whether the ISA card asserts the NOWS# signal prior to the ISA command strobe (MEMRD#, MEMWR#, IORD# or IOWR) assertion. If it does and it is an 8-bit card, or a 16-bit card which uses I/O accesses, then the NOWS# delay should be enabled.

4.4 ISA Interface AEN Signal

The PCI 9052 floats the Local Address (LA) bus during reset, and drives the LA bus when it owns the Local Bus and is idle. If during initialization a Local Bus device were to respond to an address on the idle Local Bus, the device could subsequently assert an interrupt, which could hang the system since the driver that knows how to clear the interrupt is not yet loaded.

Accordingly, ISA devices interfaced to the PCI 9052RDK-Lite ISA interface must not decode the ISA address bus during initialization, nor do they need decode it between PCI 9052 transfers while the PCI 9052 owns the bus. However, many ISA cards decode the address bus whenever AEN is de-asserted (by an ISA master). Since the PCI 9052RDK-Lite ISA interface does not support ISA masters, AEN is tied to ground, and this does not disable AEN-gated address decoding during initialization, nor while the bus is idle.

If the ISA card to be inserted into the PCI 9052RDK-Lite ISA connector relies solely on AEN toggling to enable decoding of the address, the following solution can be applied.

Drive AEN (on the ISA connector) using the Chip Select CS3# output, and program the CS3BASE register value in EEPROM, to assert the Chip Select for the ISA address range(s). Since CS3# and USER3 signals are multiplexed onto the same pin 141, with USER3 being the PCI 9052 default configuration, CS3# functionality must be enabled by setting the CNTRL[9] bit value in EEPROM to 1. PCI 9052RDK-Lite default EEPROM values enable CS3#.

On the RDK, cut the short trace connecting AEN (ISA connector pin A11) to a via (ground). Solder a wire to connect CS3# (at JP2-13) to ISA connector pin A11. Remove any jumper connecting CS3# (JP2-13) to either CSROM# (JP2-14) or CSRAM# (JP2-10).

The RDK default configuration maps CS3# to the ROM socket, with CS3BASE programmed for a 1 MB range starting at Local address 2000000h. If only one of ISA memory (Space 0) or ISA I/O (Space 1) is used, the CS3BASE register can be programmed with the same value used in the CS0BASE or CS1BASE register. If both ISA memory and ISA I/O are used, CS3# can be programmed to include both Spaces by setting the encoded Range to a high enough power of 2, and the Base Address to a low enough multiple (such as 0) of that range, to include all Local Bus addresses used for both Spaces 0 and 1.

5. Customer Support & References

5.1 Customer Support

Prior to contacting customer support, please ensure you are sitting close to the computer that has the PCI 9052RDK-LITE and have the following information:

1. Serial Number of the PLX PCI 9052RDK-LITE
2. Operating System and type
3. Description of problem

You may contact PLX Technology, Inc. Customer Support at:

Address:	PLX Technology, Inc. 870 Maude Avenue Sunnyvale, CA 94085
Phone:	408-774-9060
	800-759-3735
Fax:	408-774-2169
Email:	USA; http://www.plxtech.com/support/ Europe, Middle East and South Africa; euro-apps@plxtech.com Asia Pacific, China and Australia; asia-apps@plxtech.com
Website:	http://www.plxtech.com

5.2 References

1. PCI 9052 Data Book, Version 2.0
   PLX Technology, Inc.,
   870 Maude Avenue,
   Sunnyvale, CA 94085 USA
   http://www.plxtech.com

6. Bill of Materials / PLD & Circuit Schematics

The following pages contain the Bill of Materials, the PLD Schematics and the Schematics for the PCI 9052RDK-LITE circuit board.

Table 6-1. Bill of Materials

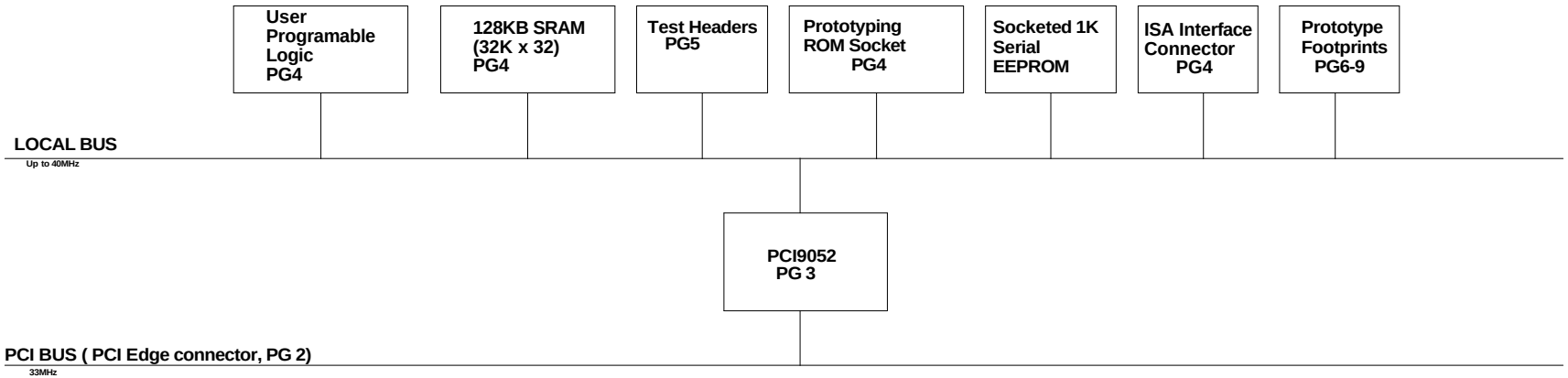
Item#	Qty	Mfg	Mfg Part Number	Description	Package	Source	Part Reference
Surface mount components							
1	1	Murata	NFM40P12C223	0.022uF, 50V, 20%, 2A capacitor	SMT, 1206	HB Eurodis	CF1
2	5	Kemet	C0805C473M5UAC	0.047uF, 50V, 20% capacitor	SMT, 0805	Electrosonic	C1-C5
3	35	Kemet	C0805C103M5UAC	0.01uF, 50V, 20% capacitor	SMT, 0805	Electrosonic	C6-C20, C24, C42-C51, C87-C90, C100, C102, C104, C106, C107
4	9	Panasonic	ECS-T1DC106R	10uF, 20V, Tantalum capacitor	SMT, C case	Newark	C21, C23, C27, C91-C96
5	23	Kemet	C0805C104M5UAC	0.1uF, 50V, 20% capacitor	SMT, 0805	Electrosonic	C22, C26, C28-C37, C39, C83-C86, C97-C99, C101, C103, C105
6	1	Kemet	C0805C101K5XAC	100pF, 50V, 10% capacitor	SMT, 0805	Electrosonic	C25
7	1	Samtec	PLCC-032-F-N	PLCC-32 pin socket	SMT	FAI	FP1
8	2	Samtec	TSM-108-01-T-DV	8x2 header, dual row	SMT	FAI	JP1, JP2
9	1	Sullins Electronics	EZC49DCMN-S526	49X2 ISA connector, .100", straddlemount	SMT	Sullins 760-744-0125	J6
10	6	Samtec	TSM-110-01-T-DV	10x2 header, dual row	SMT	FAI	LAH1-LAH6
11	2	Steward	LI0805 H400R	Inductor 500mA	SMT, 0805	Kemtron	L1, L2
12	20	CTS	742-08-3-103-J-BK	10K, 5%, isolated res. Network	SMT, C case	Digi-key	RN1-RN19, RN23
13	3	CTS	742-08-3-102-J-BK	1K, 5%, isolated res. Network	SMT, C case	Digi-key	RN20-RN22
14	17	Panasonic	ERJ-6GEYJ103V	10K, 1/8W, 5% resistor	SMT, 0805	Digi-key	R1, R2, R11-R14, R16-R20, R26, R31, R32, R66, R74, R75
15	1	Pansonic	ERJ-6GEY470V	47 ohm, 1/8W, 5% resistor	SMT, 0805	Digi-key	R3
16	1	Panasonic	ERJ-6GEYJ472V	4.7K, 1/8W, 5% resistor	SMT, 0805	Digi-key	R15
17	2	Panasonic	ERJ-6GEYJ102V	1K, 1/8W, 5% resistor	SMT, 0805	Digi-key	R59, R77
18	3	Panasonic	ERJ-6GEYJ220V	22 ohm, 1/8W, 5% resistor	SMT, 0805	Digi-key	R76, R78, R79
19	1	Linear Technology	LT1587CM-3.3	3A, 5V to 3.3V Voltage regulator	M-pack, 3-lead DD PAK	Marshall	U1
20	1	PLX	PCI 9052	PCI Bridge	PQFP-160	PLX	U2
21	1	Samtec	ICF-314-T-O	14 pin dip 300 mil socket	SMT	FAI	U4
22	1	Altera	EPM3064ATC100-4	Programmable logic device	TQFP-100 pin	Arrow	U5

Item#	Qty	Mfg	Mfg Part Number	Description	Package	Source	Part Reference
23	4	Alliance	AS7C256-15JC	SRAM, 32Kx8	SOJ-28 pin	FAI	U7, U10, U15, U16
24	1	Samtec	ICF-308-T-O	8-pin socket, 300mil	SMT	FAI	U6
25	1	PLX	90-0023-001-A	PCB, PCI9052RDK-LITE (Use schematic 91-0023-002-A r002)			
Through hole components							
26	1	Aries Electronis	1108800	4 pin half size Osc socket	Thru hole	Digi-key	U17
27	5	Harwin	M20-9990305	3x1 header, single row	Thru hole	Harwin	JP3-JP7
28	1	Harting	9195107324	5x2 male connector, IDC 10	Thru hole	Harting	J7
Manually inserted components							
29	1	Microchip	93LC46B/P	1K Serial EEPROM	Thru hole	Digi-key	U6
30	1	CTS	MXO45HS-14.318Mhz	14.318Mhz Osc, DIP-8	Thru hole	Digi-key	U17
31	1	CTS	MXO45HS-32.000Mhz	32.000 Mhz Osc, DIP-8	Thru hole	Digi-key	U4
Miscellaneous components							
32	1	Keystone	9203	PCI bracket		Keystone	
Alternate Vendors' List							
9	1	Twin Industries	CSTE-S420	ISA saddle connector	SMT	Twin Industries 408-358-2505	J6
PLX Part #	91-0023-004-A						

ECN HISTORY

ECN NUMBER	DATE	NOTE
000	1/11/2000	Started the project
001	18/04/2001	First Production
002	7/08/2002	Update RN20, RN21, RN22 from 10K to 1K on sheet 4 to reflect the BOM Update U6 from 93CS46L to 93LC46B to reflect the BOM Update the BOM and schematic document number Changed LRESET# to LRESET for ISA interface Mode

PCI9052RDK-LITE BLOCK DIAGRAM

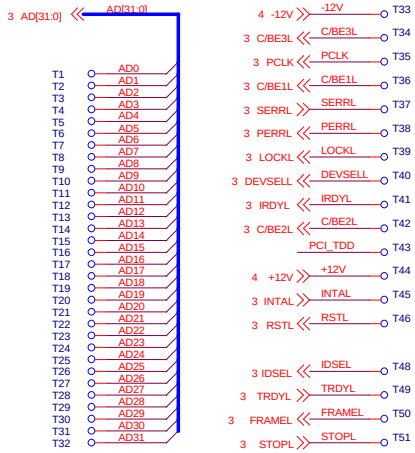


PLX TECHNOLOGY, INC.
870 Maude Ave, Sunnyvale, CA 94085
www.plxtech.com

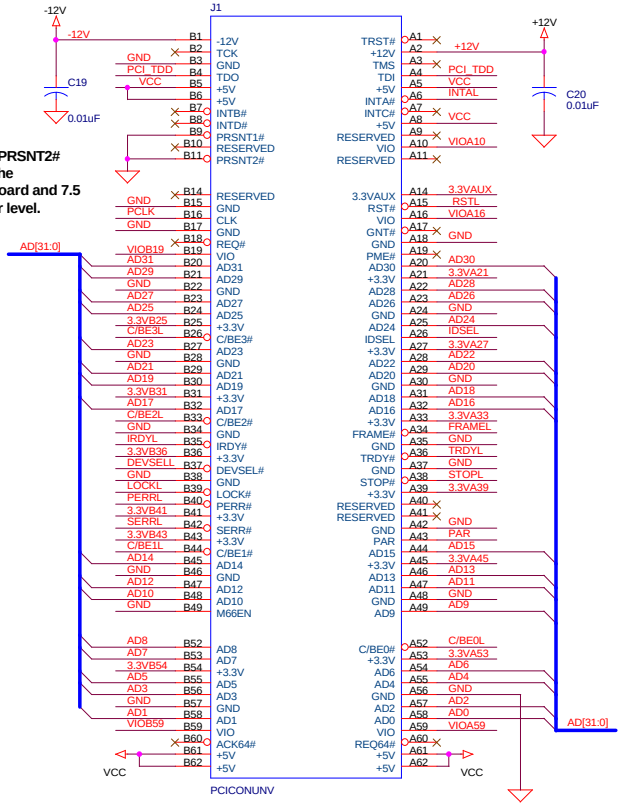
Title: **Electrical Block Diagram**

Size	Document Number	Rev
Custom	91-0023-002-A	002

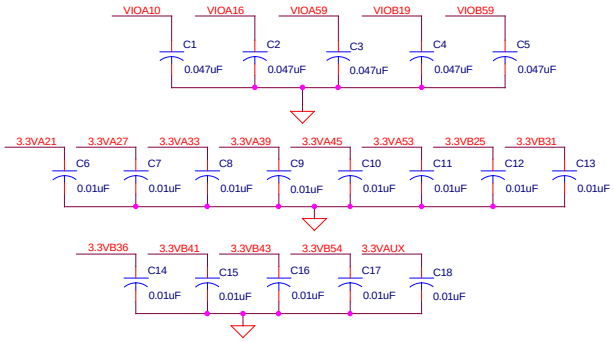
Date: Friday, July 12, 2002 Sheet 1 of 9

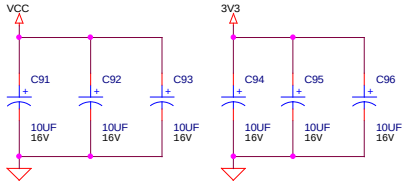


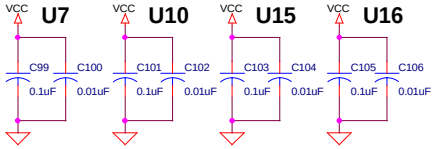
PCI Card Edge Connector



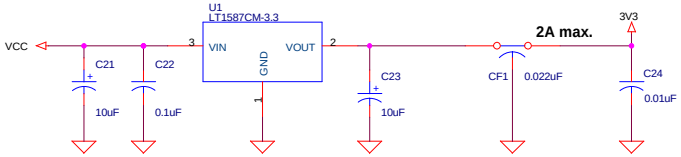
Decoupling Capacitors

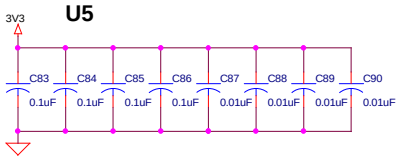






5V to 3.3V Voltage Conversion





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Title: **PCI Card Edge Connector**

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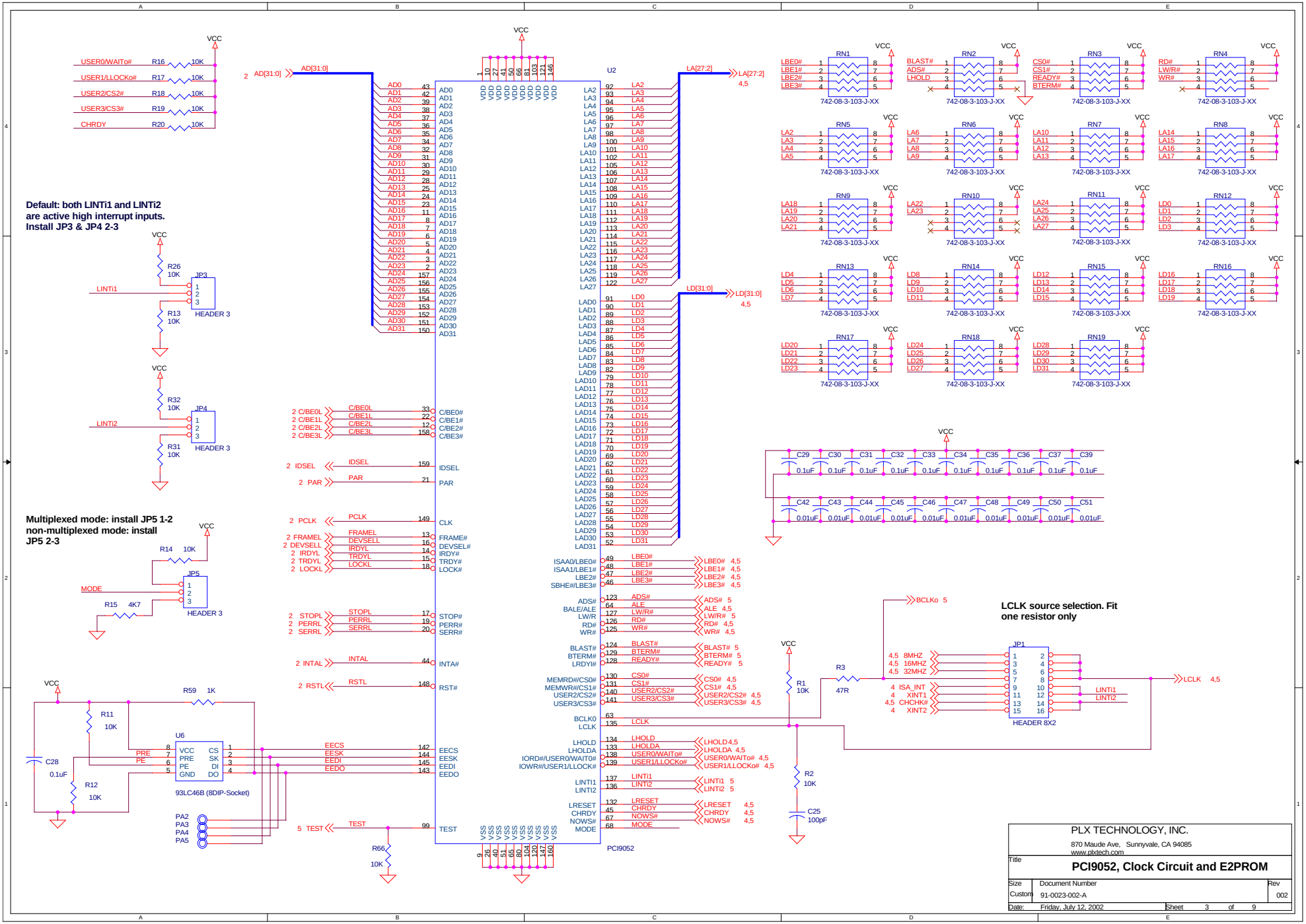
USER0/WAITo# R16 10K
USER1/LLOCKo# R17 10K
USER2/CS2# R18 10K
USER3/CS3# R19 10K
CHRDY R20 10K
Default: both LINTi1 and LINTi2 are active high interrupt inputs. Install JP3 & JP4 2-3
LINTi1
LINTi2
JP3
JP4
HEADER 3
R26 10K
R13 10K
R32 10K
R31 10K
Multiplexed mode: install JP5 1-2 non-multiplexed mode: install JP5 2-3
MODE
R14 10K
R15 4K7
JP5
U2
PCI9052
AD[31:0]
LA[27:2]
LD[31:0]
C/BE0L
C/BE1L
C/BE2L
C/BE3L
IDSEL
PAR
PCLK
FRAMEL
DEVSELL
IRDYL
TRDYL
LOCKL
STOPL
PERRL
SERRL
INTAL
RSTL
TEST
LBE0#
LBE1#
LBE2#
LBE3#
ADS#
ALE
LW/R#
RD#
WR#
BLAST#
BTERM#
READY#
CS0#
CS1#
USER2/CS2#
USER3/CS3#
BCLK0
LCLK
LHOLD
LHOLDA
USER0/WAITo#
USER1/LLOCKo#
LINTi1
LINTi2
LRESET
CHRDY
NOWS#
MODE
RN1
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
RN10
RN11
RN12
RN13
RN14
RN15
RN16
RN17
RN18
RN19
742-08-3-103-J-XX
C29 C30 C31 C32 C33 C34 C35 C36 C37 C39 0.1uF
C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 0.01uF
LCLK source selection. Fit one resistor only
BCLKo 5
JP1
HEADER 8X2
4,5 8MHZ
4,5 16MHZ
4,5 32MHZ
4 ISA_INT
4 XINT1
4,5 CHCHK#
4 XINT2
R3 47R
R1 10K
R2 10K
C25 100pF
R59 1K
R11 10K
R12 10K
C28 0.1uF
R66 10K
U6
93LC46B (8DIP-Socket)
PA2
PA3
PA4
PA5
EECS
EESK
EEDI
EEDO
R67 10K
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Title
PCI9052, Clock Circuit and E2PROM
Size Document Number Rev
Custom 91-0023-002-A 002
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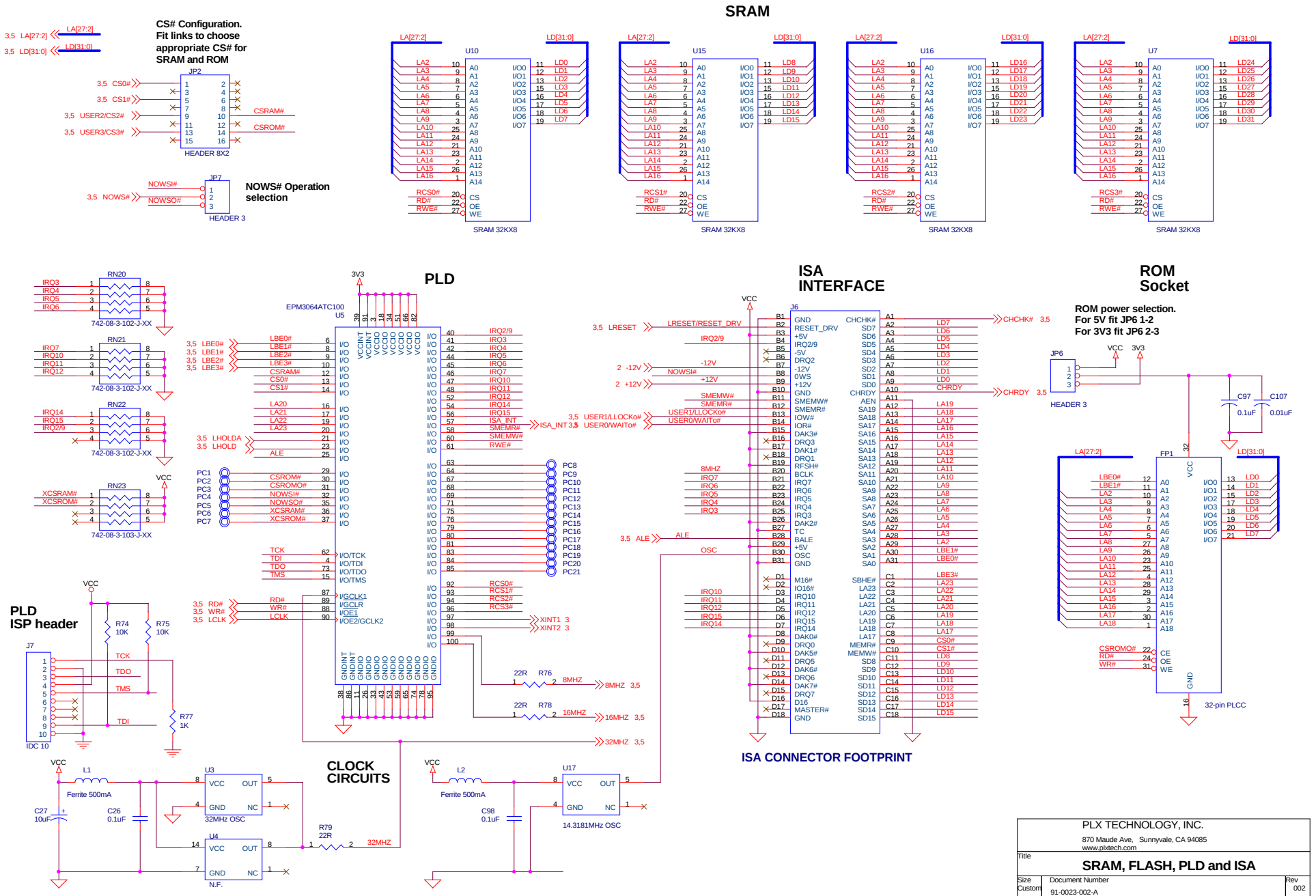
SRAM
CS# Configuration.
Fit links to choose appropriate CS# for SRAM and ROM
NOWS# Operation selection
SRAM 32KX8
PLD
EPM3064ATC100
PLD ISP header
CLOCK CIRCUITS
ISA INTERFACE
ISA CONNECTOR FOOTPRINT
ROM Socket
ROM power selection.
For 5V fit JP6 1-2
For 3V3 fit JP6 2-3
32-pin PLCC
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SRAM, FLASH, PLD and ISA
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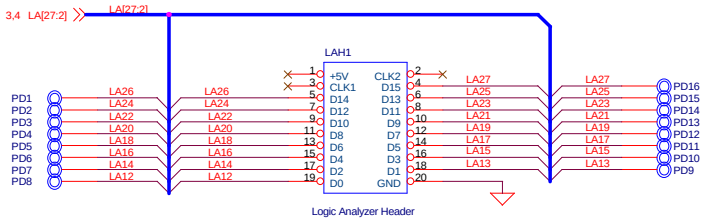
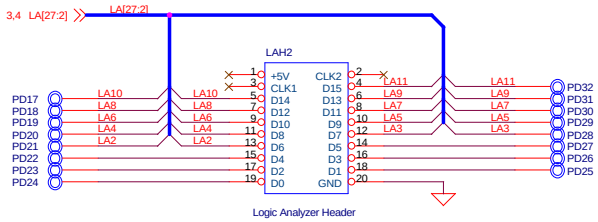
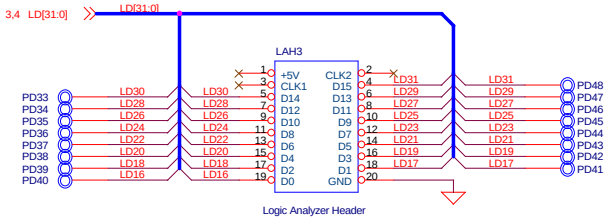
Local Address Bus -Upper Addresses



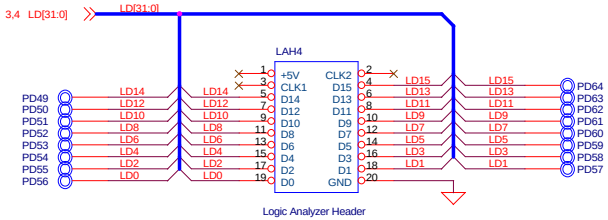
Local Address Bus - Lower Addresses



Local Data Bus - Upper Half



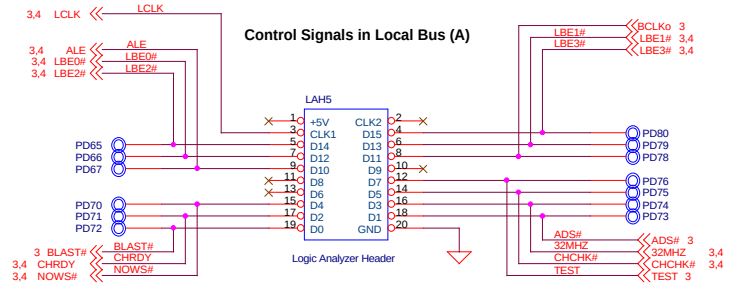
Local Data Bus - Lower Half



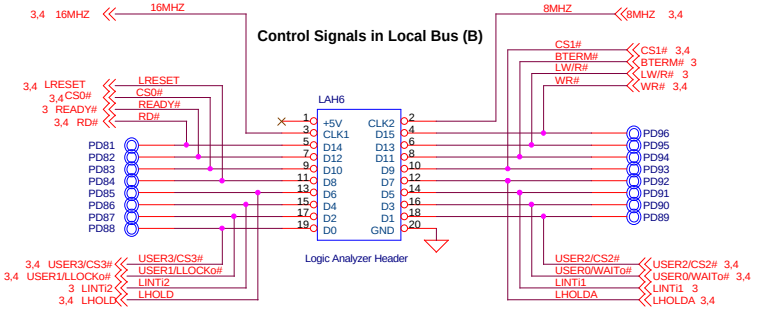
Test Headers

Note: these are designed to hook up directly to HP logic analyzer termination adapter 01650-63203.

Control Signals in Local Bus (A)



Control Signals in Local Bus (B)



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Title: **Logic Analyzer Test Headers**

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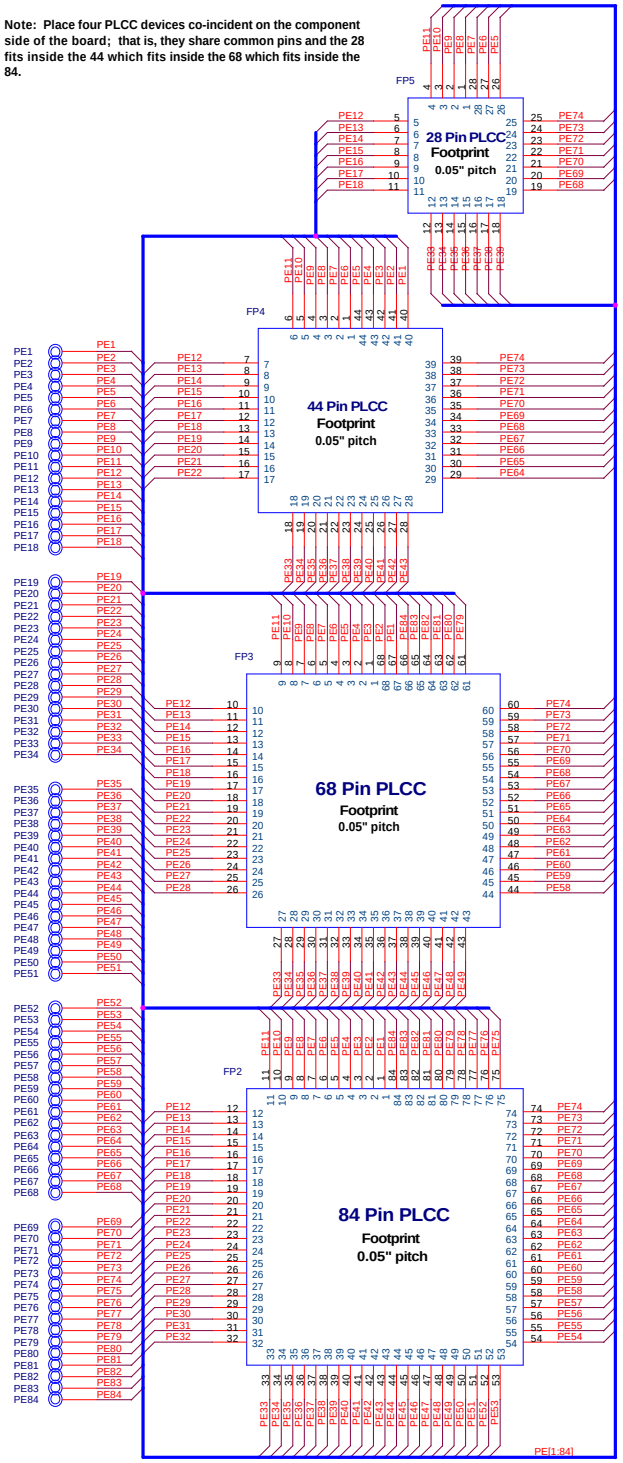
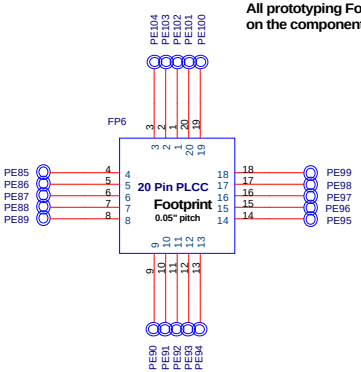
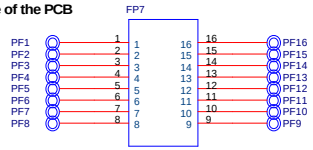
Note: Place four PLCC devices co-incident on the component side of the board; that is, they share common pins and the 28 fits inside the 44 which fits inside the 68 which fits inside the 84.



Prototyping Footprint A

All prototyping Footprints are located on the component side of the PCB





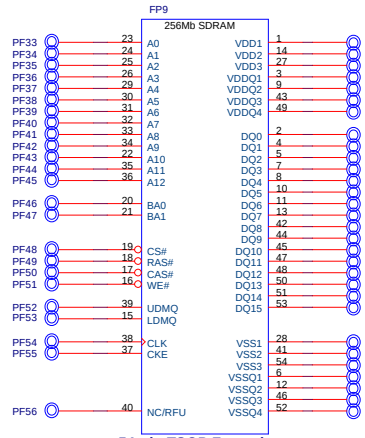
16-pin SOIC Narrow Footprint

0.150" wide, 0.05" pitch

16-pin SOIC Narrow Footprint

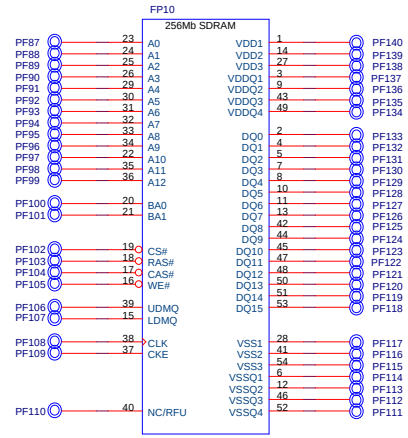
0.150" wide, 0.05" pitch

Power & Ground Rails



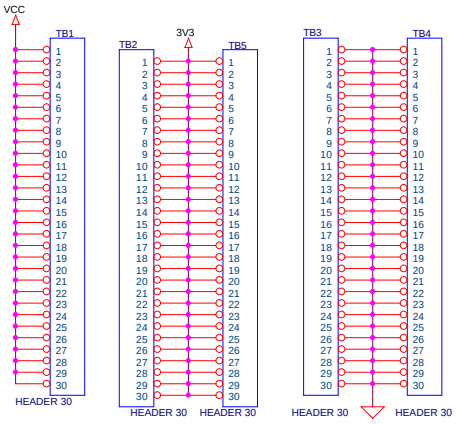
54-pin TSOP Footprint

0.8mm



54-pin TSOP Footprint

0.8mm



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Title: Prototyping Footprint A		
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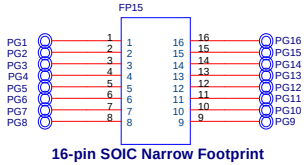
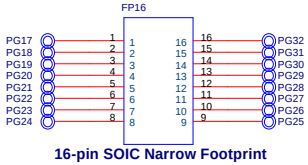
Prototyping Footprint B

All prototyping footprints are located on the component side of the PCB.



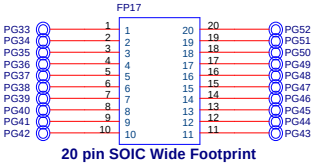
16-pin SOIC Narrow Footprint

0.150" wide, 0.05" pitch



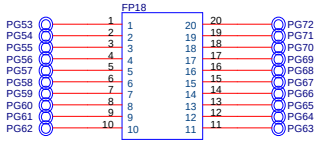
16-pin SOIC Narrow Footprint

0.150" wide, 0.05" pitch



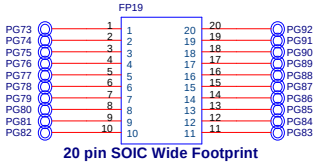
20 pin SOIC Wide Footprint

0.300" wide, 0.05" pitch



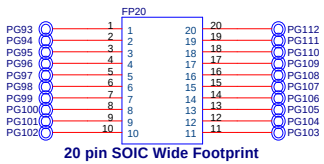
20 pin SOIC Wide Footprint

0.300" Wide, 0.05" pitch



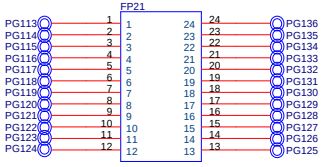
20 pin SOIC Wide Footprint

0.300" wide, 0.05" pitch



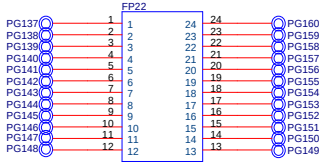
20 pin SOIC Wide Footprint

0.300" wide, 0.05" pitch



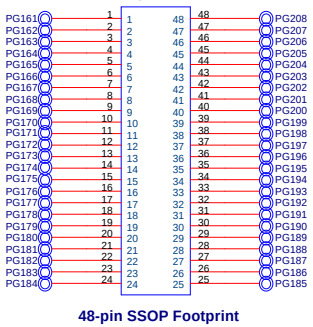
24 pin SSOP Footprint

0.150" wide, 0.025" pitch



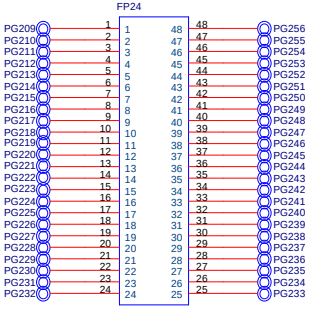
24 pin SSOP Footprint

0.150" wide, 0.025" pitch



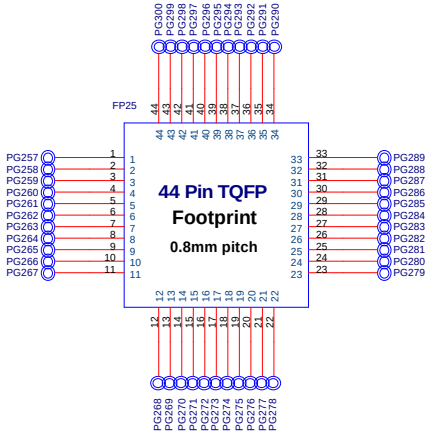
48-pin SSOP Footprint

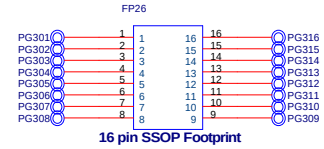
0.300" wide, 0.025" pitch



48-pin SSOP Footprint

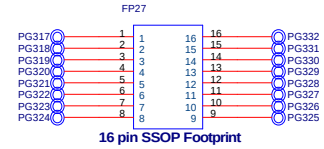
0.300" wide, 0.025" pitch





16 pin SSOP Footprint

0.150" wide, 0.025" pitch



16 pin SSOP Footprint

0.150" wide, 0.025" pitch

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Title: **Prototyping Footprint B**

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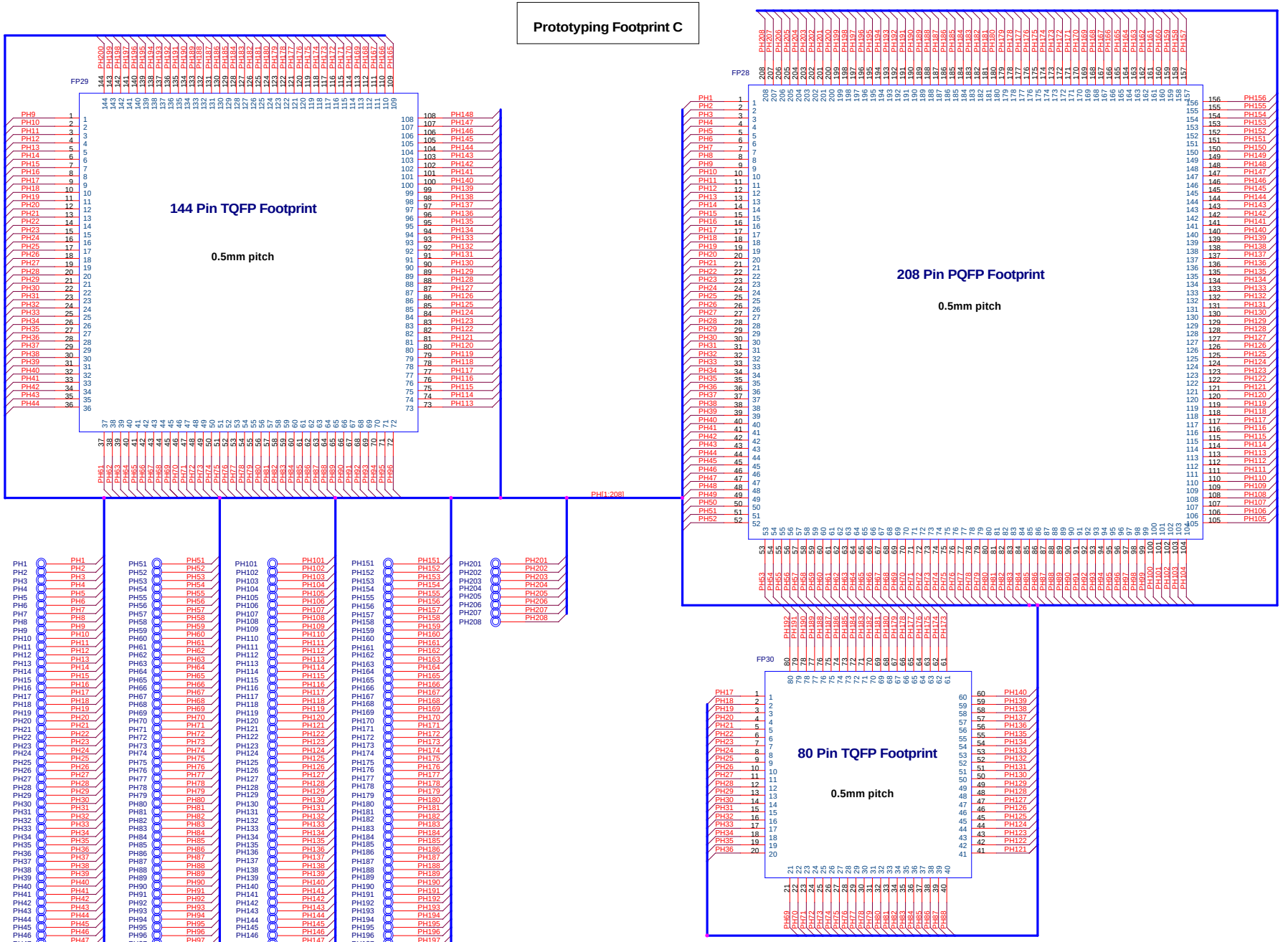
Prototyping Footprint C



Note: three footprints are placed on the component side of the PCB. They are arranged as FP30 inside of FP29 and FP29 insde of FP28. All 208 holes for prototyping are located outside of 208-pin PQFP footprint.

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Title: **Prototyping Footprint C**

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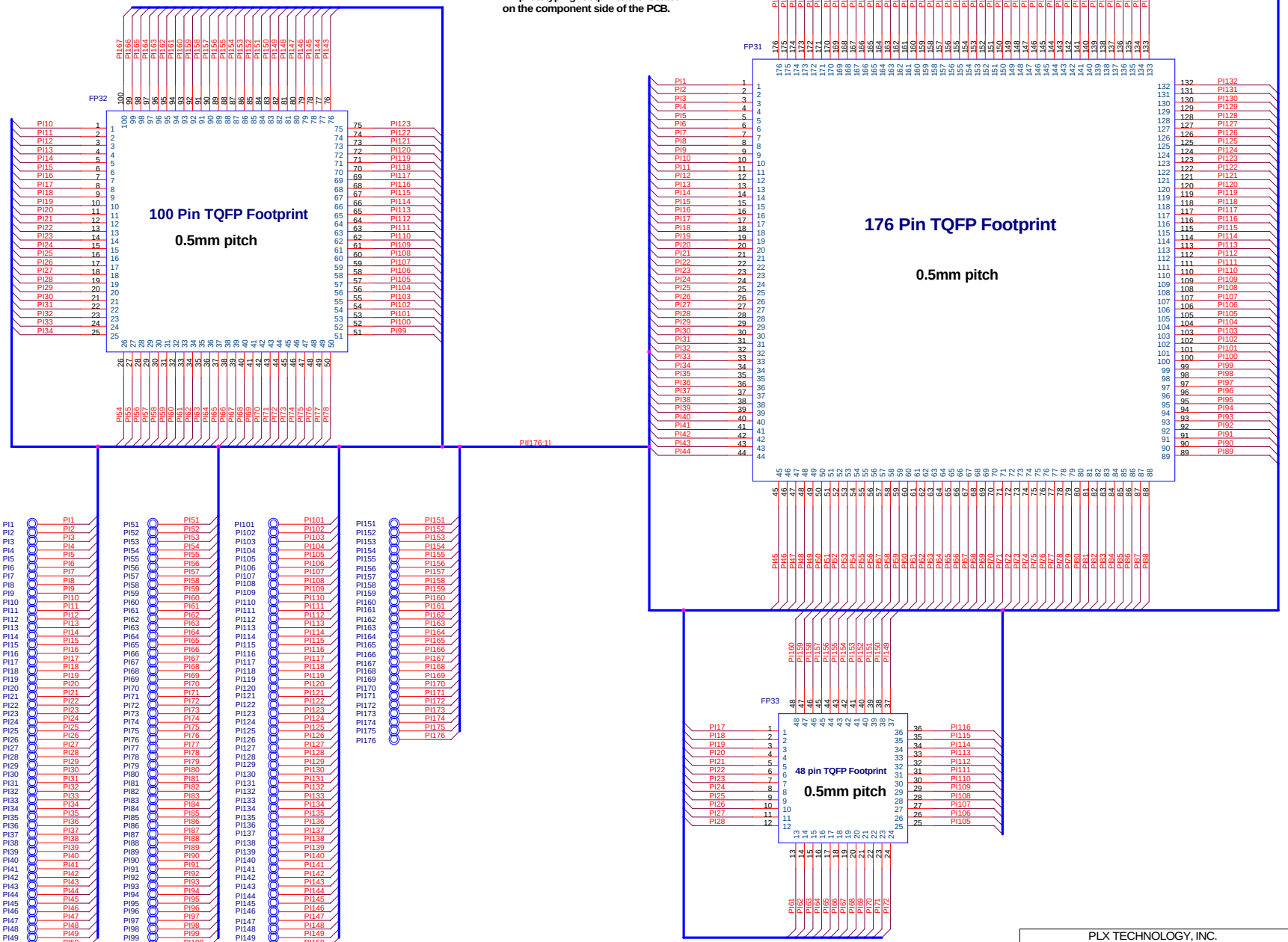
Prototyping Footprint D

All prototyping footprints are located on the component side of the PCB.



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Title: **Prototyping Footprint D**

Size	Document Number	Rev
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