Errata Documentation

A. Affected Silicon Revision

This document details errata in the following silicon:

Product	Part Number	Description	Status
PCI 9030	PCI9030-AA60PI	176-pin PQFP Package	Production Released Silicon
PCI 9030	PCI9030-AA60BI	180-pin μBGA Package	Production Released Silicon

B. Documentation Revision

The following documentation is the baseline functional description of the silicon. Errata are defined as behaviors in the affected silicon that do not match behaviors detailed in this documentation.

Document	Revision	Description	Publication Date
PCI 9030 Data Book	1.4	Data Book	May 2002

C. Errata Documentation Revision History

Revision	Date	Description
1.0	April 2000	Errata #1.
1.3	March 2001	Errata #1 to #4.
1.4	August 2001	Added Errata #5 to #6.
1.5	October 2001	Added Errata #7 to #9.
1.6	Dec. 2001	Revised Errata #7.
1.7	June 2002	Revised Errata # 2.
1.8	March 2003	Added Errata #10.
1.9	May 2005	Added Errata #11, revised Errata #9.
2.0	July 2005	Corrected v1.9 errata numbering; #5 - #9 were mislabeled #4 - #8.

D. Errata Summary:

#	Description
1	Vital Product Data (VPD) Transfer Status Flag update
2	GPIO (General Purpose Input/Output) pins configured as Outputs are driven only when the PCI 9030 owns the Local Bus and LREQ = 0
3	In PCI 9030 Data Book version 1.0, pin assignments for pins 52 and 53 of the PQFP package are switched
4	LA[27:24] / GPIO[4:7] multiplexed I/O pins, and Non-multiplexed Mode LD[31:0] data or Multiplexed Mode LAD[31:0] address/data I/O pins, are driven low during PCI reset
5	JTAG Test Reset input (TRST#) is not optional
6	JTAG Bypass Mode
7	Power Management Interface Specification version support
8	TDI is incorrectly shifted into the PCI 9030 JTAG Boundary Scan Register while in BYPASS Mode when the TAP Controller is in the Shift-DR State
9	Capabilities Pointer (CAP_PTR, PCI:34h) register value must be 40h, and Power Management Next Capability Pointer (PMNEXT, PCI:41h) register value must be 48h, for the PCI 9030 to function correctly (both are byte default values, over-writable only by serial EEPROM)
10	CS[3:2]#, LA[27:24], WAITo#, and LLOCKo# float prior to LGNT output assertion if LREQ input is asserted
11	PME# Pin Isolation

E. Errata Details:

1. Vital Product Data (VPD) Transfer Status Flag update

Problem: To perform a VPD write, data is written to the PVPDATA register, followed by a write of the VPD address with bit 31, the VPD Flag (PVPDAD[15]) set, after which the bit clears when the write completes. For a VPD read, the address is written with the VPD Flag (PVPDAD[15]) clear, after which the Flag is set when the read completes. However, during VPD Write/Read transfers the status completion Flag (PVPDAD [15]) intermittently fails to update. The system could hang if the Flag is not set to the appropriate value after the transaction, with the initiator waiting for the Flag to be set. This problem does not affect reads of the EEPROM during PCI 9030 initialization.

Solutions/Workarounds: (either/both)

1. If the flag is not set within 500 μsec time frame, the executed transaction needs to be restarted, to guarantee successful completion of the VPD transaction.
2. Use CNTRL[27:24] bits rather than VPD to read/write from/to the Serial EEPROM.

2. GPIO (General Purpose Input/Output) pins configured as Outputs are driven only when the PCI 9030 owns the Local Bus and LREQ = 0

Problem: GPIO (General Purpose Input/Output) pins configured as outputs are driven only when the PCI 9030 owns the Local bus and LREQ input is low. If another Local bus master requests the bus by asserting LREQ (high), the GPIO pins configured as outputs are floated.

Solutions/Workarounds: If GPIO pin output functionality is needed and another local master will be granted the local bus:

1. Latch the GPIO pin output(s) when a local bus master asserts LREQ to the PCI 9030 to request Local bus ownership.
2. If the design does not use CompactPCI Hot Swap, use LEDon# instead of a GPIO pin that is configured as an output. LEDon# is controlled by the LED Software On/Off Switch bit (HS_CSR[3] in PCI Configuration Space) and is also asserted during PCI reset. The LEDon# state is the inverse of the HS_CSR[3] value.
3. Use EEDI and/or EESK instead of a GPIO pin that is configured as an output. Although EEDI and EESK outputs connect to the EEPROM DI and SK inputs, typically these EEPROM inputs are Don't Care when the EEPROM CS input is low. The PCI 9030 uses these signals when accessing the EEPROM, and therefore any use as GPIO signals should be gated by EECS.

3. In PCI 9030 Data Book version 1.0, pin assignments for pins 52 and 53 of the PQFP package are switched

Problem: In The PCI 9030 Data Book version 1.0, pin assignments for pins 52 and 53 of the PQFP package are switched. The correct assignments are, LEDon# is pin 52 and $V_{I/O}$ is pin 53. The assignments specified in Table 11-2 (Power and Ground Pins (176-Pin PQFP)), Table 11-7 (Local Bus Mode Independent Interface Pins), and Figure 13-3 (Physical Specification) in version 1.0 of the Data Book are not correct and should instead indicate LEDon# is pin 52 and $V_{I/O}$ is pin 53.

Note that during PCI reset (RST# asserted), LEDon# is asserted. If the LEDon# and $V_{I/O}$ signals are switched, LEDon# will sink short circuit current from the $V_{I/O}$ source during PCI reset.

Solution: The PCI 9030 Data Book has been updated from version 1.0, and all later versions of the Data Book, including the current version available on the www.plxtech.com web site, show the correct pin assignments.

4. LA[27:24] / GPIO[4:7] multiplexed I/O pins, and Non-multiplexed Mode LD[31:0] data or Multiplexed Mode LAD[31:0] address/data I/O pins, are driven low during PCI reset

Problem: The PCI 9030 drives the LA[27:24] address pins (which can be configured as GPIO[4:7] pins after PCI reset completes), and Non-multiplexed mode LD[31:0] data or Multiplexed mode LAD[31:0] address/data I/O pins, low during PCI reset rather than to high impedance state. This may result in bus contention if other devices use these signals during PCI reset. The remaining address bus signals, LA[23:2], as well as the LBE[3:0]# byte enables, are floated during PCI reset.

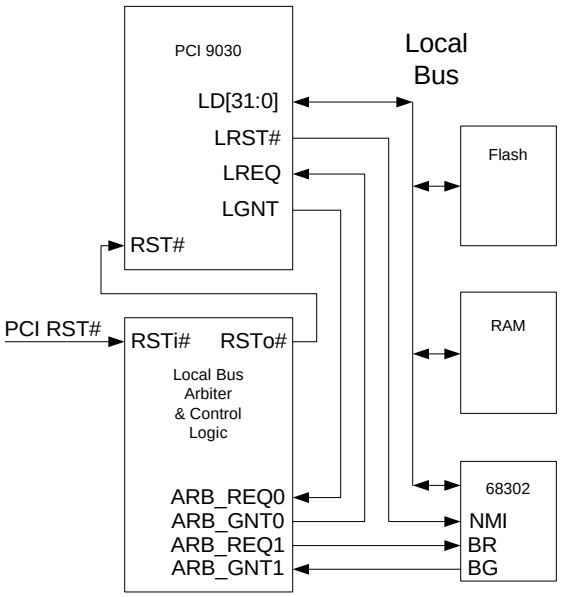
Solutions/Workarounds: (any)

1. If the LA[27:24] pins must be floated during PCI reset, isolate these address outputs with a three-state bus switch such as a Pericom PI3C3126A (3.3V, 5V-tolerant 4-bit active high bus switch), using LRESETo# to drive the bus switch Enable inputs.
2. If the Non-multiplexed mode LD[31:0] data bus, or Multiplexed mode LAD[31:0] multiplexed address/data bus must be floated during PCI reset, isolate the bus with a three-state bus switch such as a Pericom PI3C34X245 (3.3V, 5V-tolerant 32-bit bus switch), using LRESETo# to drive an inverter that has its output connected to the active low bus switch Enable inputs.
3. If both LA[27:24] and LD/LAD[31:0] buses must be floated during PCI reset, isolate these buses with a three-state bus switch such as a Pericom PI3C34X461 (3.3V, 5V-tolerant 40-bit bus switch), using LRESETo# to drive an inverter that has its output connected to the active low bus switch Enable inputs.
4. Create external logic that controls the local bus arbitration and captures PCI RST# to provide a conditioned RST# signal to the PCI 9030. The basic concept is to always request the local bus from the PCI 9030 and only grant the bus to PCI 9030 when it informs the system that it needs the bus by negating its LGNT pin. Below is a detailed description of this workaround.

Block Diagram, Workaround concept

Below is a block diagram of one possible implementation, showing only the relevant signals. The necessity of this workaround is required only if the user does not want PCI reset to generate a system/board reset. Because the PCI 9030 drives the LA[27:24], LD/LAD[31:0], and LRST# pins low as long its RST# is asserted, bus contention will occur on the local bus if other local bus devices are using the bus at that time. The workaround concept is as follows:

- Capture the PCI RST#,
- "give" the local bus to the PCI 9030;
- assert a reset pulse on the PCI 9030 RST# pin for a minimum of 2 rising PCI clock edges;
- wait for the PCI 9030 to process its RST#;
- "take" local bus control back from the PCI 9030, resume normal local bus activity, prepare for the next PCI RST# after it negates



Block Diagram of one possible work around implementation

Using the PCI 9030 with other Local Masters

Because the PCI 9030 contains only Direct Slave functionality, the Local Bus Arbiter was designed to assume it owns the local bus at all times except when it gives it up (by asserting LGNT). Therefore, (under this assumption) it is acceptable to drive the local bus anytime, including during PCI reset, except when Local bus ownership is granted to another Local bus device during normal operation. If LGNT and LREQ are negated, bus contention will occur if another Local Master tries to drive control and data signals on the Local bus.

To allow another device or devices to be a master on the local bus, an external arbiter needs to be designed such that it takes the local bus from the PCI 9030 and only gives it back to the PCI 9030 when it needs it. This can be done by setting register CNTRL[7] = 0 and asserting LREQ (as early as power up). Then the only time the PCI 9030 gets the local bus back is when it negates LGNT (preempt condition, indicating it has a pending command - only if CNTRL[7] = 0), and the external arbiter grants the PCI 9030 the Local bus by negating LREQ. The arbiter can then reassert LREQ a minimum of one clock after it was negated and wait for LGNT to be asserted before taking the Local bus back over. Depending upon the system, the user may want to customize their solution to allow windows of access depending upon expected activity.

Workaround to avoid Local Bus contention during PCI reset assertion

The workaround requires the PCI 9030 RST# signal to be asserted for a minimum of two PCI rising clock edges. If you only have access to the Local clock then you would need to determine the minimum frequency of PCI operation. A close approximation is - Minimum PCI frequency = 2.01 x 1/period, where period is the amount of time you assert RST#. If the PCI clock is available for use, the design can be constructed to ensure RST# is asserted for two rising edges, and using the PCI clock will allow the design to work down to 0.0 MHz. LREQ may be asserted before, during and/or after RST# and LRST# assertion.

5. JTAG Test Reset input (TRST#) is not optional

Problem: If TRST# is not asserted during PCI RST# assertion, the PCI 9030 could initialize into an undefined state, precluding normal chip logic operation.

Solutions/Workarounds for a Non-JTAG system:

Keep TRST# asserted by pulling it low using a 1K to 10K resistor to ground. This will keep the JTAG logic in a reset state and will enable normal chip logic operation.

Solutions/Workarounds for a system with JTAG or Hot Swap:

Buffer PCI RST# and use the output to drive both the TRST# and RST# pins on the PCI 9030 simultaneously.

Notes about JTAG implementations:

1. Please refer to both the PCI specification and the JTAG specification (IEEE 1149.1) for JTAG pin requirements.
2. The JTAG specification requires pull-ups on TDI, TMS and TRST#. To stay compliant with the PCI Specification, no internal pull-ups are provided on the JTAG pins in the PCI 9030. Therefore the designer must add these pull-ups externally.

6. JTAG Bypass Mode

Problem: According to Rule 9.1.1 (b) of the JTAG specification "the shift-register stage shall be set to a logic zero on the rising edge of TCK following entry into the *Capture-DR* controller state." If the PCI 9030 TDI pin is set to a logic 1 one TCK before entry into the *Shift-DR* state, the first value clocked out of the PCI 9030 TDO pin will be a 1 instead of the required 0.

Solutions/Workarounds: (any)

1. Put the PCI 9030 at the end of the boundary scan chain and, when using the Bypass command, either mask out the first value of TDO or expect the first value out of TDO to be a 1.
2. If the PCI 9030 is not at the end of the chain, use software to modify the scan pattern such that parts further down the chain will not be affected if the first value out of the Bypass register is a 1.

7. Power Management Interface Specification version support

The previously published erratum is retracted and the issue is republished as PCI 9030 Design Notes #1.

8. TDI is incorrectly shifted into the PCI 9030 JTAG Boundary Scan Register while in BYPASS Mode when the TAP Controller is in the Shift-DR State

Description: While in Bypass mode, bypassed data will be incorrectly shifted into the PCI 9030 JTAG Boundary Scan Register. The JTAG Boundary Scan Register shifts each Boundary Scan Register location and TDI into its first Register location on each rising edge of TCK while in Shift-DR state. The new (unwanted) Boundary Scan Register values will be applied to the PCI 9030 pins when the tap controller passes through the Update-DR State. TDI is correctly shifted to TDO during this time in Bypass mode.

Solutions/Workaround(s) #1: Do not put the PCI 9030 into Bypass Mode. Always shift in the Data Register values needed into the PCI 9030.

Solutions/Workaround(s) #2: Disconnect the PCI 9030 Tap Controller and create separate control logic to Bypass the PCI 9030 JTAG logic when needed.

9. Capabilities Pointer (CAP_PTR, PCI:34h) register value must be 40h, and Power Management Next Capability Pointer (PMNEXT, PCI:41h) register value must be 48h, for the PCI 9030 to function correctly (both are byte default values, over-writable only by serial EEPROM)

Description: PCI Status register (PCISR, offset 06) bit 4 is the Capabilities List bit, which indicates whether a Capabilities linked list is implemented. A value of 0 indicates that no Capabilities linked list is available. A value of 1 (default) indicates that the value read from the Capabilities Pointer (CAP_PTR) register at Configuration offset 34h is a pointer in Configuration Space to the first item in a linked list of Capabilities. The default values are PCISR[4] = 1 and CAP_PTR = 40h which points to the Power Management Interface Capability registers at offset 40h. Each Capability in the list includes an 8-bit pointer to the next Capability, and in the PCI 9030 Power Management Interface Capability registers, this pointer is the value in the PMNEXT register (offset 41h) with default value 48h which points to the Hot Swap Capability resisters at offset 48h. PCISR[4], CAP_PTR and PMNEXT are writable only by serial EEPROM.

Problem: Regardless of the setting of PCISR[4], the values in CAP_PTR and PMNEXT are used to point to internal registers inside the PCI 9030. If either/both of these bytes is programmed by the serial EEPROM to a value other than the default values for these bytes, PCI Configuration Write accesses to the PCI 9030 will incorrectly write over the Capabilities registers in addition to writing the intended configuration register. For example, if one or both of these bytes are not programmed to their default values, a PCI Configuration Write could additionally write to the VPD Capability registers, causing a VPD write to the serial EEPROM, corrupting the configuration data. When a serial EEPROM is programmed for PCI 9030 configuration data, the CAP_PTR and PMNEXT values in EEPROM must be the default byte values of 40h and 48h, respectively, for the silicon to function properly.

Solutions/Workarounds:

1. If any of the Capabilities List functions (Power Management, Hot Swap, and/or VPD) are to be enabled, the Power Management capability must be enabled. To enable any of the Capabilities List functions, set PCISR[4] = 1 and CAP_PTR = 40h (default values). PMNEXT (PCI:41h) must be set to 48h (default pointing to Hot Swap). All values must be programmed in EEPROM. If no EEPROM is present then default register values enable all three Capabilities.
2. If it is desirable to disable the Hot Swap capability, set HS_CNTL (Hot Swap ID, PCI:48h) to 0 in EEPROM. HS_NEXT (PCI:49h) must be set to the default value 4Ch if VPD is to be enabled, otherwise to 0.
3. If it is desirable to disable the VPD capability (see Errata #1), set HS_NEXT (PCI:49h) to 0 in EEPROM.

4. Always set PVPD_NEXT (PCI:4Dh) to 0 in EEPROM.
5. If it is desirable to disable all Capabilities List functions, set PCISR[4] = 0, CAP_PTR = 40h, and PMNEXT = 48h in the EEPROM.

10. CS[3:2]#, LA[27:24], WAITo#, and LLOCKo# float prior to LGNT output assertion if LREQ input is asserted

Documented Behavior: If LREQ input is asserted by a Local Master to request Local bus ownership, the PCI 9030 continues to drive Local bus signals until it asserts LGNT output to grant Local bus ownership. When the PCI 9030 asserts LGNT, it floats Local bus I/O signals including CS[3:2]#, LA[27:24]#, WAITo#, and LLOCKo#.

Problem: The PCI 9030 floats CS[3:2]#, LA[27:24], WAITo#, and LLOCKo# upon LREQ assertion.

Solutions/Workarounds:

1. Use CS[1:0]# instead of CS[3:2]# and/or do not implement designs that use LA[27:24], WAITo#, and LLOCKo#.
2. Use either of CS[1:0]# to gate LREQ input such that the PCI 9030 will see LREQ assertion only when it is not performing or about to perform a Local bus transfer. Using an AND gate, connect the CSx# output and the LREQ output from the Local bus master to the AND gate inputs, and connect the AND gate output to the PCI 9030 LREQ input.

   Program the corresponding CS0BASE or CS1BASE register to assert the Chip Select (CS0# or CS1#) for all Direct Slave accesses to any of the implemented Local Address Spaces (0, 1, 2, 3 and Expansion ROM), by setting the Range encoding and the Base Address within the CSxBASE register to include all Local bus addresses accessible through Direct Slave transfers. The Chip Select will assert only for Local bus addresses that are mapped within any of the Local Address Spaces as defined by the LASxRR (Range) and LASxBA (Base Address, or Remap) registers.

   Example: programming the CS0BASE or CS1BASE register with the value 08000001h will enable the Chip Select to assert for any Direct Slave access within the 256 MB address map.

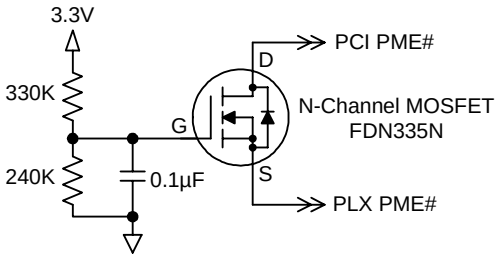
11. PME# Pin Isolation

Documented Behavior: Add-in card components that support PCI Power Management and implement PME# must ensure that whenever power is removed, the non-powered PME# output does not present a low impedance path to ground. Otherwise, there could be an accidental system wake up event.

Actual Behavior: The silicon does not ensure such protection and does present a low impedance path to ground when in the D3cold state, essentially causing an accidental wake up event every time the add-in card is inserted.

Workaround:

If PME# is to be implemented, an external FET must be inserted between the silicon's PME# signal pin and the PCI Slot. Suggested circuit:



If PME# is not implemented, since the open-drain output is constructed using a PCI I/O buffer, termination such as an external pull-up resistor is recommended to prevent input buffer oscillation.