A. Affected Silicon Revision

This document details known errata for the following silicon:

Product	Revision	Description	Status
PEX8605	AA	4-Lane, 4-Port PCI Express Switch	Full Production
PEX8605	AB	4-Lane, 4-Port PCI Express Switch	Full Production

B. Affected Documentation Revision

This document details known errors, corrections and additions for the following device documentation:

Document	Version	Description	Publication Date
PEX8605 Data Book	1.3	Data Book	November, 2012

Documentation changes described herein will be included in the next major release of the data book. Any new documentation issues discovered before that time will be added to this list on a timely basis.

C. Errata List Revision History

Revision	Publication Date	Description
1.0	1 August 2011	• Initial Publication
1.1	31 August 2011	• Documentation changes from 1.0 version Errata List have been rolled into v 0.85 data book release
1.2	7 October 2011	• Added Erratum #3 • Changes to DC specifications, 3.3V signaling now supported.
1.3	5 January 2012	• Added Erratum #4 • Added documentation changes
1.4	6 March 2012	• ***Important Documentation Correction:*** Device Pin Descriptions Updated. (See section F for details)
1.5	8 March 2012	• Correction updated.
1.6	8 May 2012	• Added Erratum #5

Revision	Publication Date	Description
1.7	10 October 2012	• Added Sightings Issues 1, 2 • Added Documentation Updates
1.8	30 November 2012	• Added AB version information

D. Errata Summary

Errata are known problems with the silicon for which root cause has been determined. Workaround options are provided where possible. Detailed descriptions of each are given in Section F.

Erratum #	Description	Risk Category	Silicon Rev Affected
Err_1	Enabling ASPM L0s (and L1) on PCI Express ports causes spurious ERR_CORR messages to be transmitted.	Low	AA, AB
Err_2	At the 5.0 GT/s signaling rate, PEX8605 transmitters apply 0 dB de-emphasis when they should apply -6 dB de-emphasis	Med	AA
Err_3	AC-JTAG instructions are non-functional	Med	AA
Err_4	Port 0 BAR0 address decode range is larger than requested	Low	AA
Err_5	PEX_REFCLK_OUT buffered output clocks not valid until 900 usec after PEX_PERST# input is de-asserted.	Low	AA, AB

E. Sightings Summary

Sightings are issues with the silicon that are currently being investigated, or any other issues found in the field that designers should be aware of. See Section H for details.

Issue #	Description	Risk Category	Silicon Rev Affected
Issue_1	MSI Mask register bits 58h[3:1] are not writeable in default case.	Low	AA, AB
Issue_2	Slot Status and Control register Command Completed Interrupt Enable bit (80h[4]) is not writeable in any case.	Low	AA, AB

F. Documentation Changes Summary

At the time of this writing, the current data book version is 1.2. All documentation changes listed below apply to this version of the data book, and will be incorporated in the next data book release.

Item #	Description
Doc_1	**IMPORTANT DOCUMENTATION UPDATE (v 1.1 and Earlier)** Table 3-10: Device Pins **A26** and **B19** are incorrectly labeled as VDD_IO, where they should be labeled as VAUX_IO. The v 1.2 and later data book (and related technical documentation) has been corrected as follows: VAUX_IO supply consists of 4 pins: A18, A26, A64, B19 VDD_IO supply consists of 5 pins: A30, A43, B3, B31, B41 **IMPACT:** - Designs implementing D3cold power state (Vaux) will be affected by this change. Designers please take note. Designs that do not implement Vaux supply are not affected, as these designs connect VDD_IO and VAUX_IO pins to the same supply.
Doc_2	**EE_DI Signal Requires External Pull-Up Resistor when External EEPROM is used.** EE_DI signal, when external serial EEPROM is implemented, requires an external pull-up resistor (4.7K-10K ohms). While this IO cell has an internal pull-up, it is not strong enough to guarantee fast rise time of the signal.

G. Erratum Details

Err_1. Enabling ASPM L0s (and L1) on PCI Express Ports Causes ERR_CORR Messages to be Transmitted

Description

When L0s ASPM feature is enabled, spurious false errors could be logged which could result in ERR_CORR messages being transmitted to the PCI Express host.

Workaround

When L0s ASPM is enabled, set the Correctable Error Mask bits, FC8h[7,6,0] = 111b to prevent unwanted ERR_CORR messages due to false errors.

Impact

Spurious ERR_CORR messages could be received and the Correctable Error Detected status bit (72h[0]) may be set when L0s (and L1) ASPM is enabled

Err_2. At the 5.0 GT/s signaling rate, PEX8605 transmitters apply 0 dB de-emphasis when they should apply -6 dB de-emphasis

Description

For a typical Gen 2 device during link-up, in the Recovery.Speed sub-state, if the new data rate is 5.0 GT/s, -6 dB de-emphasis must be selected for operation if the ***select_deemphasis*** variable (TS1 and TS2 Ordered Set, symbol 4, bit 6) is 0b. PEX8605, however, applies 0 dB de-emphasis in this case.

Also, for compliance testing, in the Polling.Compliance sub-state, the data rate and de-emphasis level should go through the following progression, depending on how many times the link has entered Polling.Compliance sub-state before.

1. Data Rate = 2.5 G, De-emphasis level = -3.5 dB
2. Data Rate = 5.0 G, De-emphasis level = -3.5 dB
3. Data Rate = 5.0 G, De-emphasis level = -6 dB

PEX8605, however, goes through the following progression:

1. Data Rate = 2.5 G, De-emphasis level = -3.5 dB
2. Data Rate = 5.0 G, De-emphasis level = -3.5 dB
3. Data Rate = 5.0 G, De-emphasis level = **0 dB**

Workarounds

There are two options for workarounds. Workaround is only needed in cases where the link partner is incurring receiver errors, DLLP errors or TLP errors.

1. From EEPROM or I2C, program register bit 98h[6] = 1 in the affected port prior to link-up. When set, this bit causes the PEX8605 to advertise ***select_deemphasis*** = 1, which will cause the link to operate at -3.5 dB de-emphasis always when at 5.0 GT/s speed.
2. From EEPROM, I2C, or at run-time via Port 0, program register bits B80h[23:20]=1b in Port 0 (one bit per lane, bit 20 is lane 0, bit 23 is lane 3). When Set, this register bit forces the selected lane to operate at -6dB de-emphasis. Note that this setting may not be desirable for a Gen 1 (2.5 GT/s) link partner.

Impact

1. For PCI Express links with long trace runs (approximately 10” or more), a 5.0 GT/s link partner may incur receiver errors, DLLP errors and TLP errors.
2. PCI Express compliance tests may fail because the link progresses to 0 dB instead of -6 dB as expected.

Err_3. AC-JTAG Instructions Are Non-Functional

Description

AC-JTAG instructions EXTEST_TRAIN and EXTEST_PULSE are non-functional because SerDes receiver channels are disabled by default when JTAG test mode is enabled. Expected behavior is for the receivers to be enabled when JTAG test mode is enabled.

Workaround

SerDes receiver channels must be explicitly enabled prior to performing JTAG testing by programming the sequence of registers listed below from serial EEPROM or I2C. Note that this register programming is specific only to JTAG testing, and that the EEPROM entries below must be cleared for normal operation of the device.

Port 0 Register Offset	Register Data
0xB80	0x3000_0720
0xBD8	0x0000_1215
0xB80	0x3001_0720
0xBD8	0x0000_1215
0xB80	0x3002_0720
0xBD8	0x0000_1215
0xB80	0x3003_0720
0xBD8	0x0000_1215

Impact

AC-JTAG instructions EXTEST_PULSE and EXTEST_TRAIN are not supported for system designs that do not implement serial EEPROM or I2C programming access.

Err_4. Port 0 BAR0 Address Decode Range is Larger than Requested

Description

Port 0 BAR 0 register, upon PCI enumeration, claims an address range of 16K bytes, which is used to map internal registers into PCI Express memory space. However, PEX8605 will also respond to addresses up to 128K bytes above the BAR 0 address. Expected behavior is for reads to addresses above BAR0+16K to be completed with UR status.

Additionally, a downstream PCI express device attempting to read to PCI Express memory addresses in the range BAR0+16K to BAR0+128K will be completed with UR status. Write TLP's from downstream devices into this range will be discarded. Expected behavior is for these requests to be forwarded to the upstream port.

Workaround

Workaround options include:

- Do not allocate memory for downstream devices in the range BAR0 to BAR0+128K
- Disable BAR0, BAR1 by programming register bit 660h[26] = 1b from serial EEPROM. (this bit can also be set at run-time)

Impact

Failures were reported when performing Microsoft WHQL tests (unreported IO).

Err_5. PEX_REFCLK_OUTp*x*/n*x* Clock Outputs is not Guaranteed Until 900 us After PEX_PERST# De-assertion

Description

At initial power-on, valid clock may not appear at the PEX_REFCLK_OUTp*x*/n*x* output pins, even while a valid clock is present on the PEX_REFCLKp/n input pins, until 900 us after PEX_PERST# input pin is de-asserted. Because PCI Express devices attached to the downstream ports of the switch require their input clocks to be valid for 100 us prior to de-assertion of PERST# (per PCI Express specifications), it is not possible for both PEX8605 and its downstream devices to share a common reset line.

Workarounds

Workaround options may vary depending on the application. For any workaround implemented, PERST# de-assertion on the downstream device must be delayed by at least 1 ms from PEX_PERST# input.

1. Use separate signals for driving PEX_PERST# and PERST# for the downstream devices. Design the system so that PERST# on the downstream device remains asserted at least 1 ms after PEX_PERST# is de-asserted.
2. Use GPIO[3:1] output pins for driving PERST# to downstream devices. In this option, firmware must first configure the PEX8605 GPIO pins (default function for GPIO[3:0] pins is LANE_GOOD[3:0]), program the GPIO pin to toggle low then high, and then configure downstream devices.
3. Create a delayed version of PEX_PERST# using a delay circuit such as the one shown in Figure 1 below. This circuit delays the rising edge of PEX_PERST# input by approximately 1 ms. Adjust resistor/capacitor values as needed to produce the required delay.

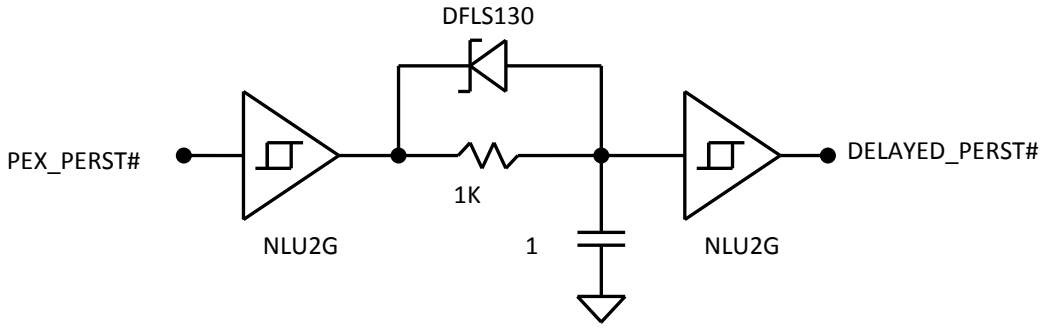

Figure 1. An example circuit to create a delayed version of PEX_PERST# for downstream devices.

Impact

Downstream PCI Express devices may not reset correctly when PEX8605 and downstream devices share a common reset line.

H. Sightings Details

Issue_1. MSI Mask Register bits 58h[3:1] are not Writeable in Default Case

Description

By default, MSI Capability register Multiple Message Capable (48h[19:17]) field returns a value of 010b, meaning the Port can request up to four Vectors. Also, by default, Multiple Message Enable (48h[22:20]) field returns a value of 000b, meaning the port is allocated one Vector. In this case, MSI Mask register bits 58h[3:1] are not writeable.

Workarounds

Do one of the following:

1. From EEPROM or I2C, prior to device enumeration, program 48h[19:17] = 000b (only one Vector), for all ports
2. From EEPROM or I2C, prior to device enumeration, or at run-time prior to running the test, for all ports, program 48h[22:20] = 010b (Port is allocated 4 Vectors).
3. For systems that do not use EEPROM, after the device is enumerated for memory mapped access (via BAR 0 register), and before the test is run, program memory mapped registers as follows:

Register Bits	Value	Description
660h[30]	1b	This is a Factory Test Only bit which enables R/W access to registers normally writeable only by EEPROM/I2C.
48h[22:20]	010b	Port 0 allocated four Vectors
1048h[22:20]	010b	Port 1 allocated four Vectors
2048h[22:20]	010b	Port 2 allocated four Vectors
3048h[22:20]	010b	Port 3 allocated four Vectors (if present)
660h[30]	0b	Clear special R/W access enable.

Impact

This issue can cause Microsoft's WHQL certification test to fail with the error message "Mask Bits register of the MSI Capability table must be read-writeable for all the values up to and including Fh."

Issue_2. Slot Status and Control register Command Completed Interrupt Enable bit (80h[4]) is not Writeable in any Case

Description

For the Downstream port to which the HP_PRSNT# pin is currently assigned (see 1E0h[17:16], Present Pin Assignment Register), the Slot Capability[Hot Plug Capable] (7Ch[6]) bit will read as 1b, as expected. In this case, Microsoft WHQL test will fail because Slot Status[Command Completed Interrupt Enable] (80h[4]) bit is not write-able (always 0b). This test failure, however, is meaningless because none of the hot-plug related functions that use this interrupt bit are implemented in this device.

Workarounds

1) From EEPROM or I2C, prior to device enumeration, for all downstream ports, program port register 7Ch[6] = 0b. This causes the port to report no support for Hot Plug, and the tests will pass.
2) For systems that do not use EEPROM, after the device is enumerated for MemoryMapped access (via BAR 0 register), and before the test is run, program memory mapped registers as follows:

Register Bits	Value	Description
660h[30]	1b	This is a Factory Test Only bit which enables R/W access to registers normally writeable only by EEPROM/I2C.
107Ch[6]	0b	Clear Hot Plug Capable bit for Port 1
207Ch[6]	0b	Clear Hot Plug Capable bit for Port 2
307Ch[6]	0b	Clear Hot Plug Capable bit for Port 3 (if present)
660h[30]	0b	Clear special R/W access enable.

Impact

This issue can cause Microsoft WHQL certification test to fail as described above.