PEX 8114BA ➔ PEX 8114BB
PEX 8114BB ➔ PEX 8114BC
PEX 8114BC ➔ PEX 8114BD
Conversion Documentation

This document details changes that designers must be aware of as they convert PEX 8114BA silicon-based designs to use the latest generation PEX 8114BB, and convert PEX 8114BB to PEX 8114BC, and convert PEX 8114BC to PEX 8114BD. Technical assistance is available at the PLX Technical Support web page (www.plxtech.com/support/).

A. Silicon Documentation

Document	Version	Description	Publication Date
PEX 8114BA Data Book	1.1	Four Lane PCI Express-to-PCI/PCI-X Bridge	August, 2006
PEX 8114BB Data Book	2.0	Four Lane PCI Express-to-PCI/PCI-X Bridge	December, 2006
PEX 8114BC Data Book	3.0	Four Lane PCI Express-to-PCI/PCI-X Bridge	January, 2007
PEX 8114BD Data Book	4.0	Four Lane PCI Express-to-PCI/PCI-X Bridge	January, 2008

B. Conversion Documentation Revision History

Revision	Publication Date	Description
1.0	February 16, 2007	Baseline.
2.0	December 18, 2007	Add conversion to PEX8114BD.

C. Conversion Documentation Summary

#	Description
1	Non-Transparent Mode Support Removed
2	Errata Fixed and Cautions Resolved in PEX 8114BB Silicon
3	Erratum Fixed in PEX 8114BC Silicon
4	Erratum Fixed in PEX 8114BD Silicon

1. Non-Transparent Mode Support Removed

Silicon Revisions BB, BC, and BD do not support Non-Transparent mode. All references to Non-Transparent mode has been removed from the *PEX 8114BB*, *PEX 8114BC,* and *PEX 8114BD Data Books*.

2. Errata Fixed and Cautions Resolved in PEX 8114BB Silicon

The PEX 8114BB fixes the following errata and resolves the following cautions in the *PEX 8114BA Errata, Revision 2.0*. Refer to the Errata document for further details.

Errata

- E9. In PCI-X Mode, Register Set Erroneously Indicates that PEX 8114 Is Medium Speed Device, Rather than Slow Speed Device
- E11. Palette Snoop Bit Can Be Set in Forward Bridge Mode
- E12. Read Completion Delivery Is Gated by Bus Master Enable Bit
- E13. PCI 64-Bit Data Corruption
- E15. PCI Express Completion Excluded Due to Pending PCI Interrupt Contending with Repetitive PCI Retries
- E16. PCI-X Immediate Read Completion Data Overflow

Cautions

- G1. Reverse Bridge Mode PCI Express Non-Fatal Errors are Translated into PCI_SERR# on PCI Bus
- G3. Single Data Phase PCI Read Requests Generate TLPs with a Size Determined by Prefetch Count and Not Limited by Single Data Phase Size

3. Erratum Fixed in PEX 8114BC Silicon

The PEX 8114BC fixes the following erratum in the *PEX 8114BB Errata, Revision 1.2*. Refer to the Errata document for further details.

- 18. Silent Data Corruption Associated with Data Bursts that Cross 4-KB Address Boundary Spaces Starting from Specific Address

4. Erratum Fixed in PEX 8114BD Silicon

The PEX 8114BD fixes the following erratum in the *PEX 8114BC Errata, Revision 1.6*. Refer to the Errata document for further details.

- 21. IDCODE instruction violates IEEE 1149.1 compliance
- 22. Transactions may be dropped or ignored after the PEX 8114 exists the L1 power state
- 24. PEX 8114 PCI-X to PCI Express buffer Overrun