Optical Interconnects for AI: Components and Co-Packaged Optics (CPO)

Broadcom

March 2024

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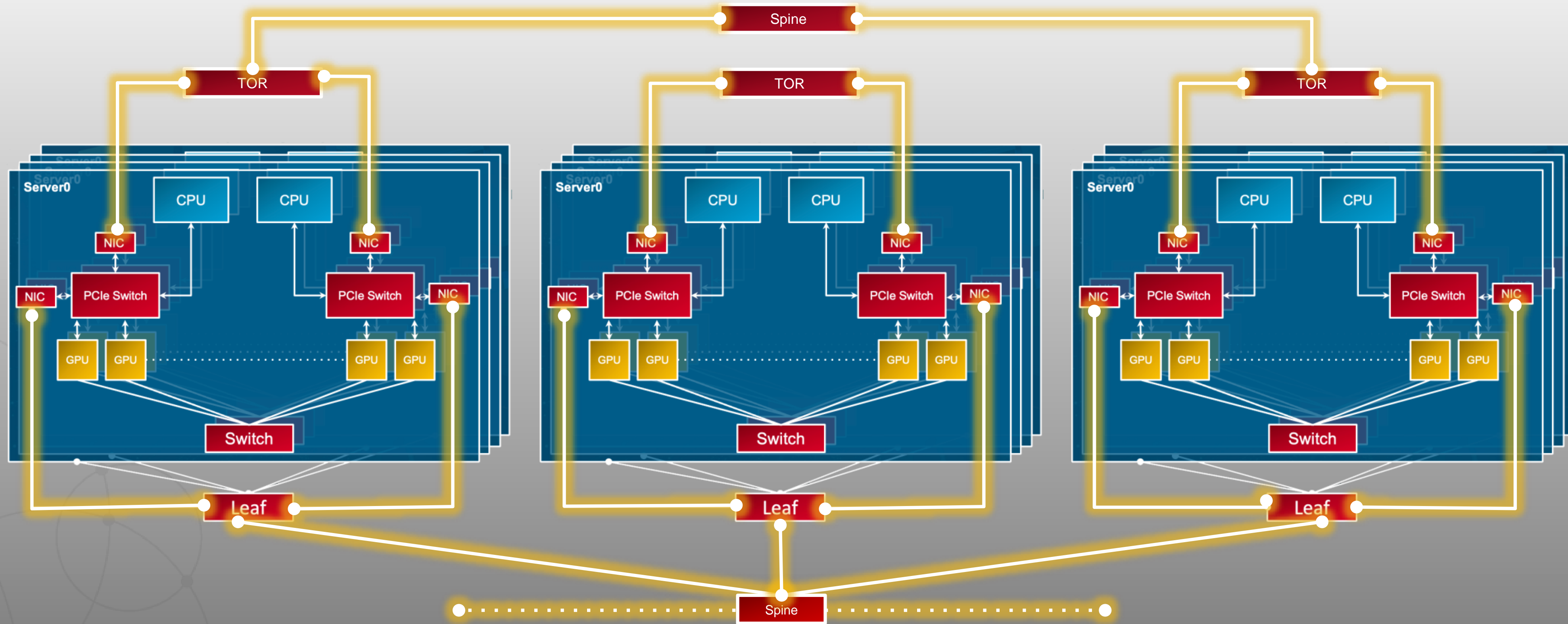
The Optical Interconnect for AI



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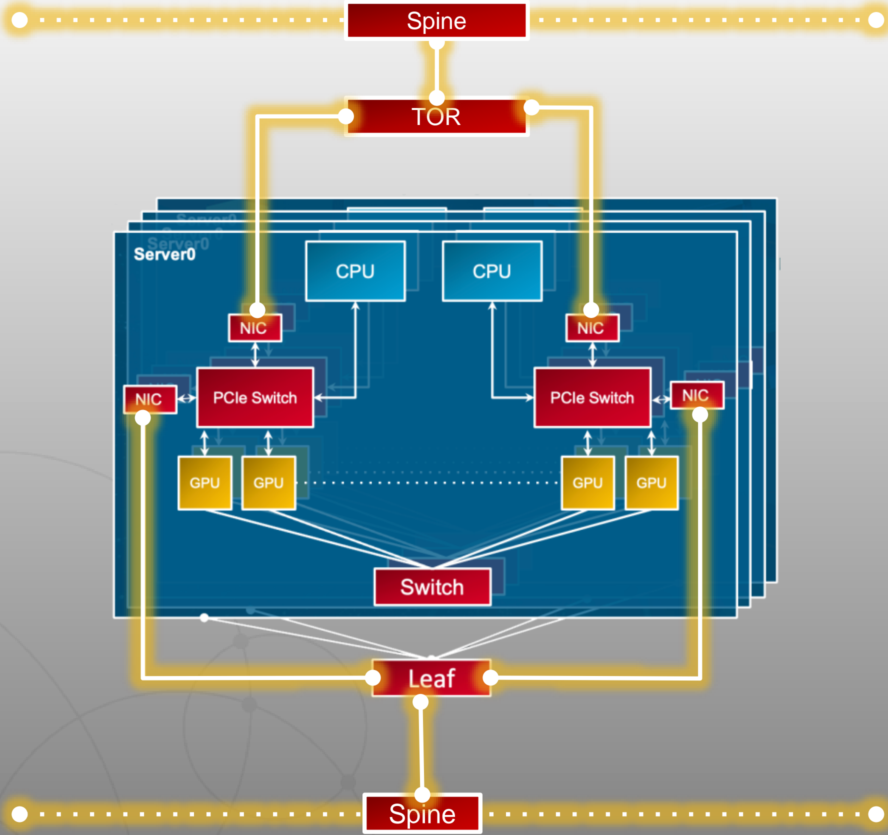
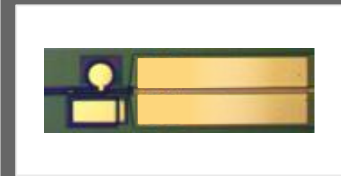
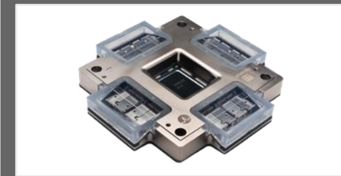


VCSEL — Multi-mode, short reach



EML — Single-mode, long reach



CPO (SiPho) — Power and cost leadership

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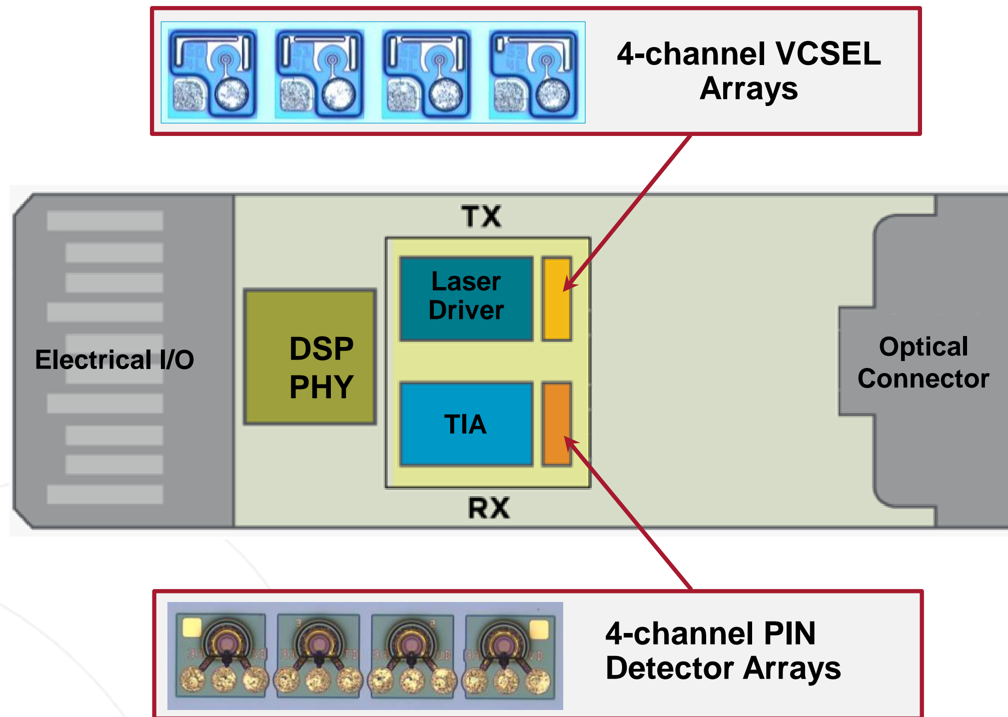
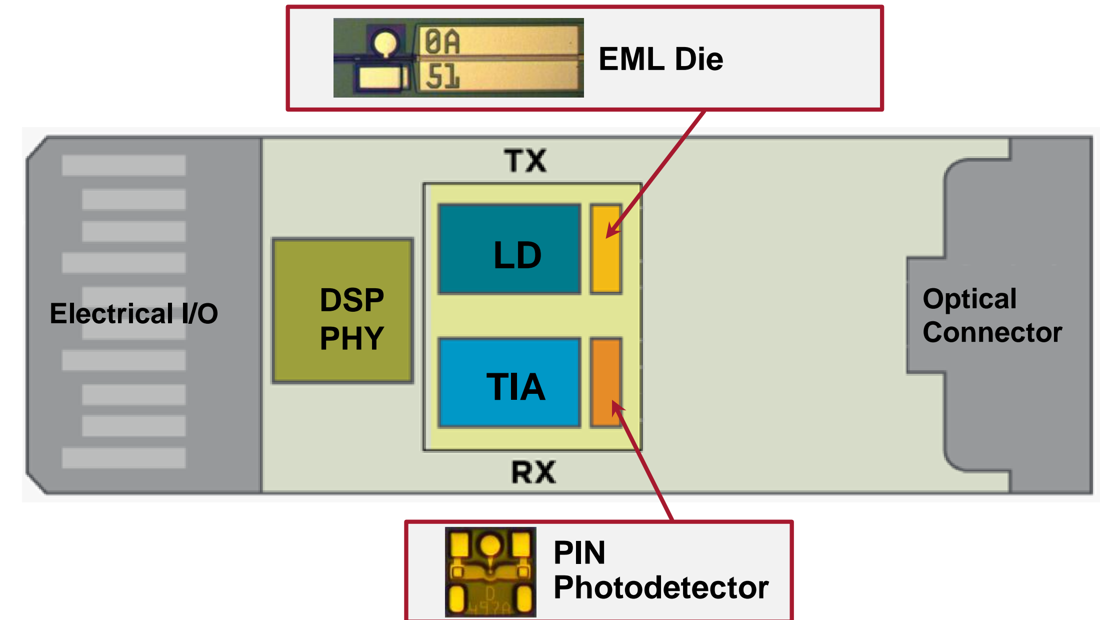
Broadcom Component Use Cases in AI Optical Transceivers



Multimode 800G and 1.6T VCSEL Based Transceivers



Singlemode 800G and 1.6T EML Based Transceiver

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100G and 200G VCSELs

4x100G: Production Now

4x200G: 2H 2024 Samples

- 4x100G and 4x200G VCSEL Arrays
- 1.6T SR8 Transceiver Enablement
- Up to 100m reach over Multi-Mode Fiber
- Lowest Optical Transceiver Packaging Cost
- Optimal for Back-End AI Network

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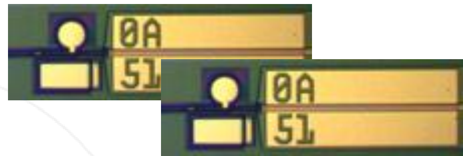
100G and 200G EMLs



Production Now

- 100G and 200G Single Channel EMLs
- 1.6T DR8 and CWDM8 Transceiver Enablement
- Up to 2km reach over Single-Mode Fiber
- WDM Enables Lowest Fiber Cost
- Flexible Use for Back-End and Front-End Networks

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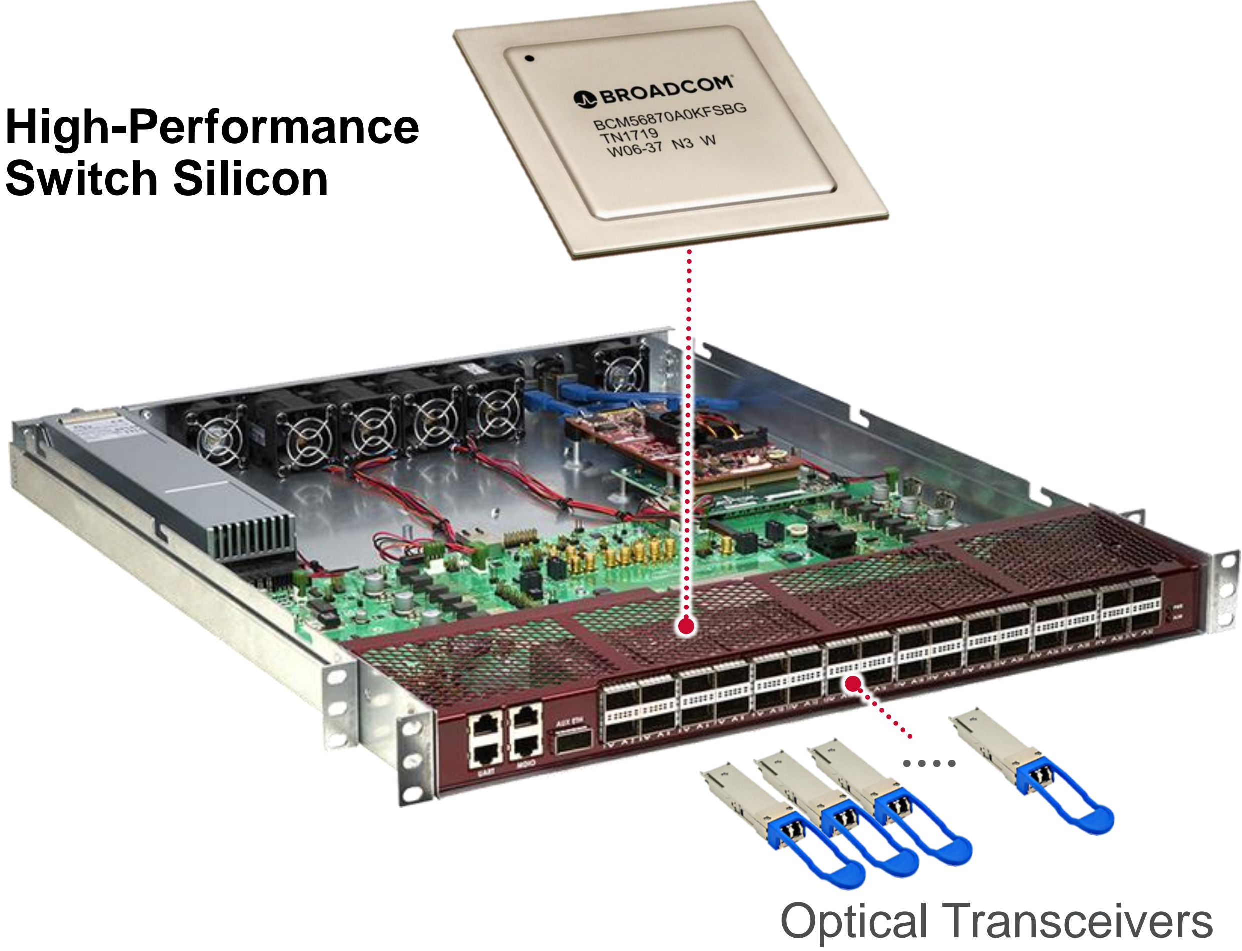
Optical Interconnect Dominates Fabric Silicon Spend



Optical Transceivers

Current Customer Spend*

10x $

Switch	Optics

Opportunity for Step Function Improvement in Optical Connectivity

* Source: LightCounting, Dell'Oro, 650 Group and Broadcom internal estimates

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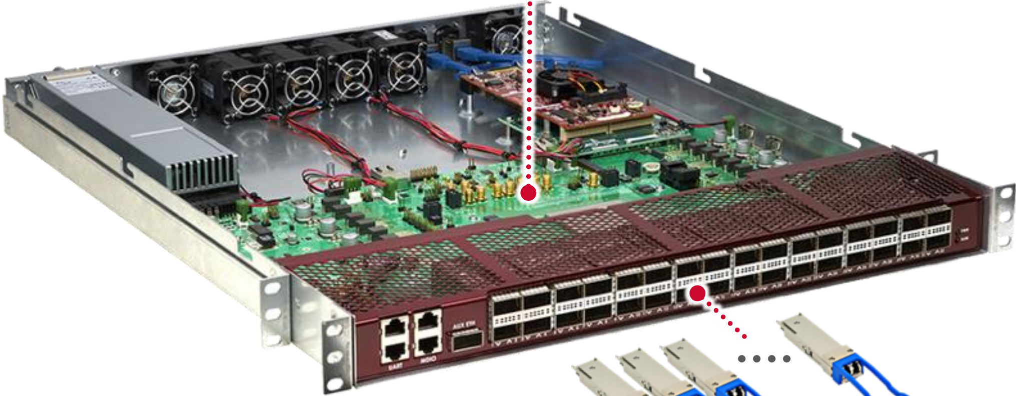
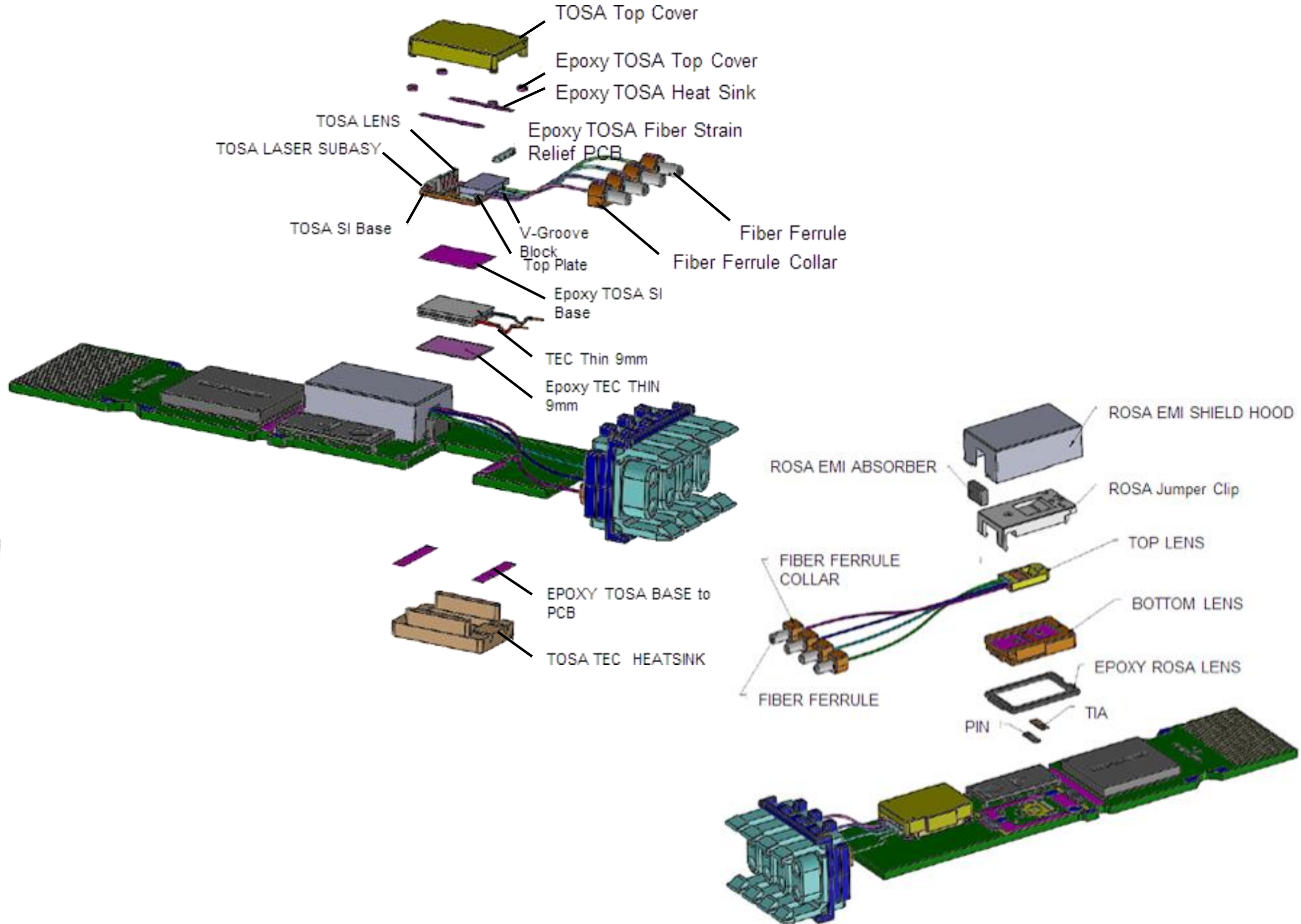
Complexity of Each Box in the Datacenter

High-Performance Switch Silicon



Optical Transceivers



Standard Rack Appliance

Standard Optical Transceiver

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Evolution of Optics: Discrete III-V to Co-Packaged SiPh

Conventional Module Design

TOSA Top Cover
Epoxy TOSA Top Cover
Epoxy TOSA Heat Sink
TOSA LENS
TOSA LASER SUBASY
Epoxy TOSA Fiber Strain
TOSA SI Base
V-Groove
Fiber Ferrule
Fiber Ferrule Collar
Epoxy TOSA SI Base
TEC Thin 9mm
Epoxy TEC THIN 9mm
ROSA EMI SHIELD HOOD
ROSA EMI ABSORBER
ROSA Jumper Clip
EPOXY TOSA BASE to PCB
TOP LENS
TOSA TEC HEATSINK
FIBER FERRULE COLLAR
BOTTOM LENS
EPOXY ROSA LENS
FIBER FERRULE
TIA
PIN

Engineering and manufacturing limits to scale

Integrated Module Design Based w/ Silicon Photonics

SiPh Chiplets in Package (SCIP)

Phy IC

Fiber Jumper

30% fewer Piece Parts!

Module Integration = First step to improved scale

Co-Packaged Optics

Highly Integrated Optical Engines (3.2T to 6.4T)

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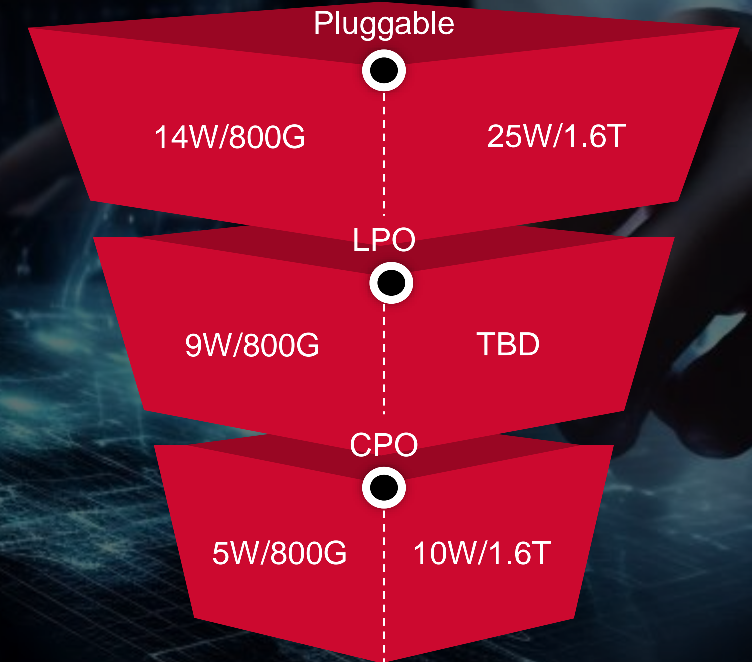
Why Co-Packaged Optics (CPO)?

Lowest Cost/Bit with massive reduction in components and interconnects

Power/Performance/Latency by eliminating the electrical interconnect power dissipation and variability

Leverage Silicon **Reliability** and eliminate practice of accepting high failure rate optics due to simple replacement

POWER COMPARISON



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CPO Insertion Loss Savings vs. Pluggables

DSP Pluggable

ASIC
Substrate
PCB
Cage
DSP
OSA
TX/RX
1 2 3 4 5 6

LPO Pluggable

ASIC
Substrate
PCB
Cage
DRV/TIA
OSA
TX/RX
1 2 3 4 5 6

CPO

ASIC
Optics
Substrate
PCB
TX/RX
1

>30%
Cost Savings

>80%
Insertion Loss savings

1. ASIC through substrate
2. Via Losses
3. PCB Trace Loss
4. Connector Losses
5. Module PCB Losses
6. OSA Interconnect loss

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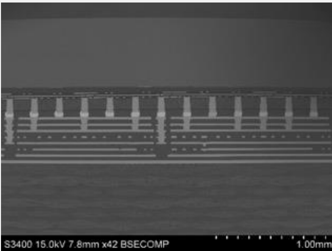
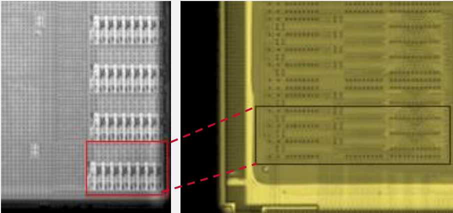
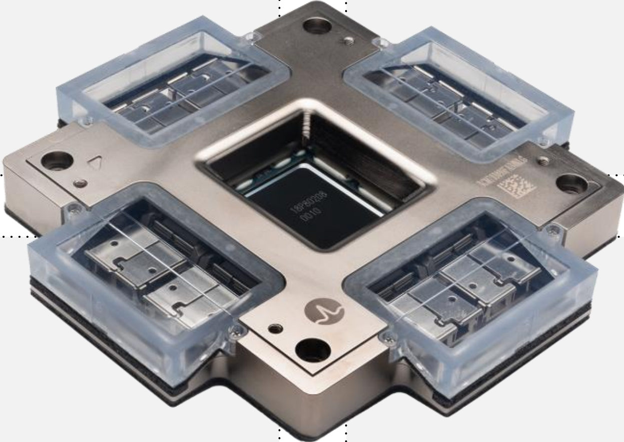
Sampling TH5-Bailly CPO today



Advanced Packaging

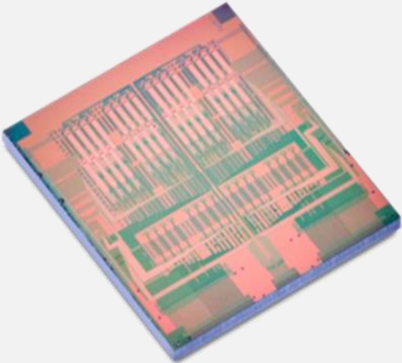
64 channel EIC with CMOS driver and TIA





ODM System Integration

64 channel FR4 PIC with integrated mux/demux



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Systems Shipping with Bailly CPO with Pluggable Lasers

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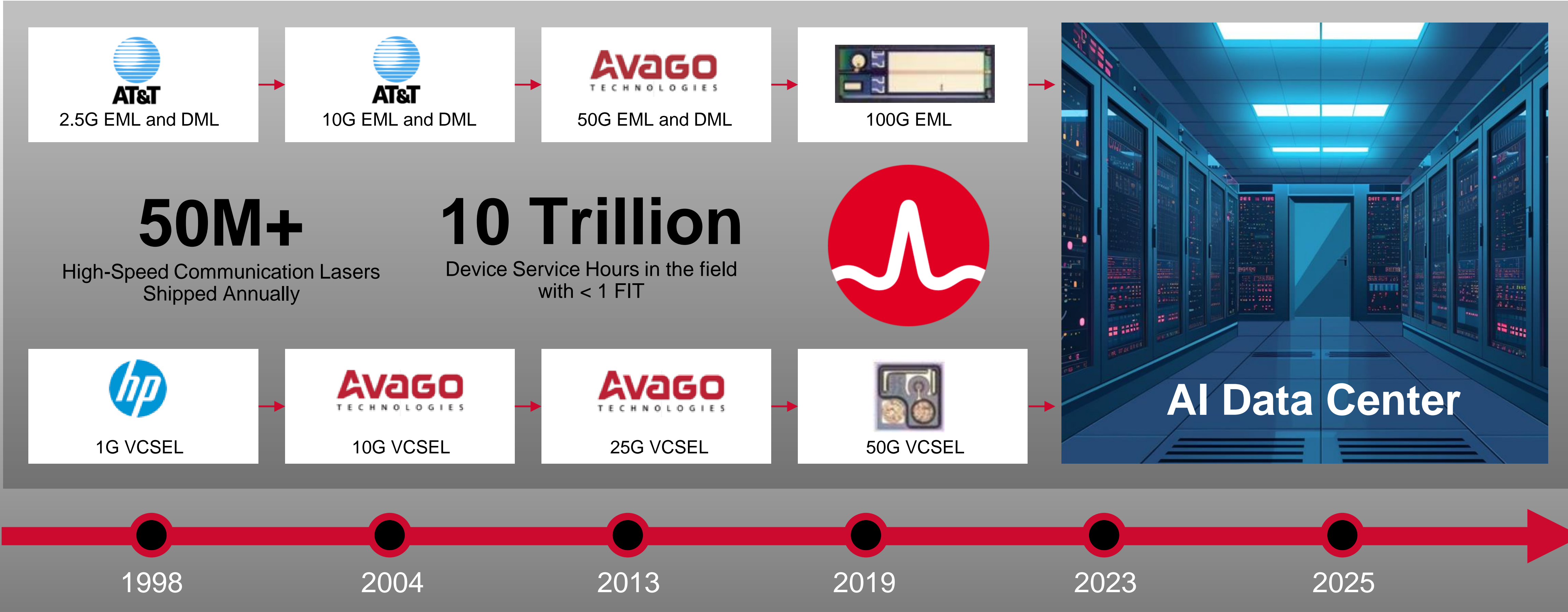
The Broadcom Optics Advantage



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