BROADCOM®

Data Sheet

AFBR-59E5APZ-HT

Multimode SFF Transceiver with LC Connector for Fast Ethernet

Description

The Broadcom® AFBR-59E5APZ-HT is a small form factor transceiver (SFF) with ultra-low power consumption that gives the system designer a product to implement a range of solutions for multimode fiber communication links.

This transceiver is supplied in the industry-standard 2 × 5 DIP style with a LC fiber connector interface.

Transmitter

The transmitter contains a 1310-nm high-reliable LED. This LED is packaged in the optical subassembly of the transmitter. It is driven by an integrated circuit that converts differential LVPECL logic signals into an analog LED drive current.

The LED is switched off if a static signal is present at the LVPECL inputs.

Receiver

The receiver uses a PIN photodiode that is integrated with a transimpedance pre- and post-amplifier in a single IC. This IC is packaged in the optical subassembly of the receiver. The data output is differential LVPECL. Rx squelch is activated at the deassert level of signal detect.

Features

- SFF package
- LC duplex connector optical interface
- Operates with 50/125-µm and 62.5/125-µm multimode fiber
- Compatible with the 100BASE-FX version of IEEE 802.3u
- Single +3.3V power supply
- Data input and output are AC-coupled
- Signal Detect Output and TX-Disable feature
- Squelched receiver outputs
- Compatible with wave solder and aqueous wash processes
- Operating temperature range: –40°C to 95°C
- Manufactured in an ISO 9001 certified facility
- RoHS compliant
- Lead free

Applications

- Factory automation
- Merging unit
- Substation automation
- HVDC systems

Module Package

The pinout and package outline, shown in Figure 1 and Figure 3, are compliant with the multisource definition of the 2 × 5 DIP. The low profile of the Broadcom transceiver design complies with the maximum height allowed for the LC connector over the entire length of the package.

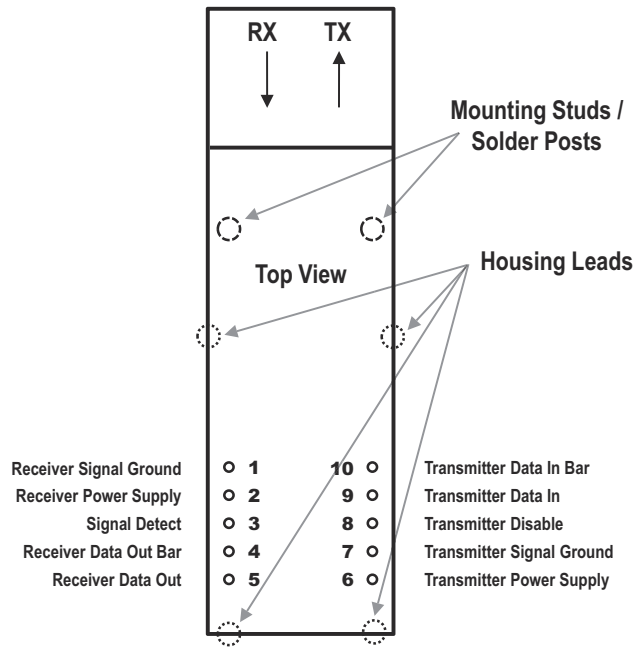
The optical subassemblies use a high-volume assembly process together with low-cost lens elements, which results in a cost-effective building block with high immunity to external EMI fields.

The electrical subassembly consists of a high-volume multilayer printed circuit board on which the TX-IC, the optical subassemblies, and various surface-mounted passive circuit elements are attached.

The outer metal cover is soldered to the PCB's TX and RX signal ground. The LC port section with solder posts is attached to the PCB by non-conductive epoxy and is isolated to the metal cover. This provides mechanical strength and full isolation from the internal circuit of the transceiver.

The transceiver has ten signal pins, two solder posts, and four housing leads. The solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver by mating with the LC connector fiber cables.

Figure 1: Pinout Diagram



Pin Descriptions

Pin 1 Receiver Signal Ground VEE RX:

Directly connect this pin to the receiver ground plane.

Pin 2 Receiver Power Supply VCC RX:

Provide +3.3V DC via the recommended receiver power supply (Figure 2). Locate the power supply filter circuit as close as possible to the V_{CC} RX pin.

Pin 3 Signal Detect SD:

The TX-IC analyses the light input power level information of the RX-IC via the "Imon" signal and provides the corresponding SD output levels. To ensure SD functionality, a supply voltage within the recommended range must be applied to the RX-IC and to the TX-IC.

Typical optical input levels (average) to the receiver result in a logic "1" output.

Low optical input levels (average) to the receiver result in a logic "0" output.

Pin 4 Receiver Data Out Bar RD-:

Rx signal AC-coupled LVPECL. See Figure 2.

Pin 5 Receiver Data Out RD+:

Rx signal AC-coupled LVPECL. See Figure 2.

Pin 6 Transmitter Power Supply VCC TX:

Provide +3.3V DC via the recommended transmitter power supply (Figure 2). Locate the power supply filter circuit as close as possible to the V_{CC} TX pin.

Pin 7 Transmitter Signal Ground VEE TX:

Directly connect this pin to the transmitter ground plane.

Pin 8 Transmitter Disable:

The transmitter is disabled when connected to HIGH.

The transmitter is enabled when connected to GND or left OPEN.

Pin 9 Transmitter Data In TD+:

Tx signal AC-coupled LVPECL. See Figure 2.

Pin 10 Transmitter Data In Bar TD-:

Tx signal AC-coupled LVPECL. See Figure 2.

Mounting Studs/Solder Posts:

The mounting studs are provided for transceiver mechanical attachment to the circuit board. It is recommended to connect them to chassis ground.

Housing Leads:

The housing leads are provided for additional signal grounding. The holes in the circuit board must be tied to signal ground.

The following information provides answers to the most common questions about using the part.

Transceiver Optical Power Budget versus Link Length

The Optical Power Budget (OPB) is the available optical power for a fiber optic link to accommodate fiber cable losses plus losses due to inline connectors, splices, and optical switches and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

The 1310-nm Broadcom LEDs show very stable performance in long-time tests, typically less than 1 dB of aging effect over normal commercial equipment life periods. Contact your Broadcom sales representative for additional details.

Handling and Precautions

It is recommended that typical industrial precautions be taken in handling and assembling these transceivers to prevent damage that might be induced by electrostatic discharge (ESD).

The AFBR-59E5APZ-HT passed the Electrostatic Discharge to all Electrical Pins by the human-body model (HBM) according to JS-001-2017 with U = ± 2000V.

Care should be taken to avoid shorting the receiver output pins to ground without proper current-limiting impedance.

Solder and Wash Process Compatibility

These transceivers are compatible with industry-standard wave or hand solder processes.

Protective process plugs are inserted in the LC receptacles of the transceivers during shipping. These process plugs act as a dust cover during shipping, but also protect the optical subassemblies during the wave solder and aqueous wash processing.

NOTE: Hand soldering is a process that is difficult to control and reproduce. Hand soldering may cause overstresses to the product that can affect product performance and reliability.

Board Layout – Decoupling Circuit, Ground Planes, and Termination Circuits

To achieve optimum performance, take care in the layout of your circuit board. Figure 2 provides a schematic for the recommended termination circuit that works well with these parts.

It is further recommended that a continuous ground plane be provided in the circuit board directly under the transceiver to provide a low-inductance ground for the signal return current. This recommendation is in keeping with good high-frequency board layout practices.

Board Layout – Hole Pattern

The Broadcom transceiver complies with the circuit board Common Transceiver Footprint hole pattern defined in the original multisource announcement that defined the 2 × 5 package style. Figure 4 reproduces this drawing with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board. It illustrates the recommended panel opening and the position of the circuit board with respect to this panel.

Label

The label is attached to the outer metal cover (illustrated in Figure 3) and provides information about the product number, the country of origin, a barcode, and the serial number (XXXXXYYWW; X = numeric counter, YY = production year, WW = production week).

Electrostatic Discharge (ESD)

The transceivers are packed in trays and shipped inside moisture barrier bags (MBBs) to keep the devices protected against humidity and to provide protection from mechanical and ESD damage during shipment and storage.

There are two main cases in which immunity to ESD damage is important.

The first case is when the transceiver is handled before it is mounted on the circuit board.

NOTE: Use typical industrial precautions for ESD-sensitive devices. These precautions include using grounded wrist straps, work benches, floor mats in ESD-controlled areas, and so on.

An ESD event may damage or degrade the device performance. Typical standards, such as DIN 61340-5-1, must be considered.

The second case to consider is static discharges to the exterior of the equipment chassis that contains the transceiver parts.

To the extent that the LC connector is exposed to the outside of the equipment chassis, it might be subject to whatever ESD system-level test criteria that the equipment is intended to meet.

Electromagnetic Immunity and Emission

Equipment that uses these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields.

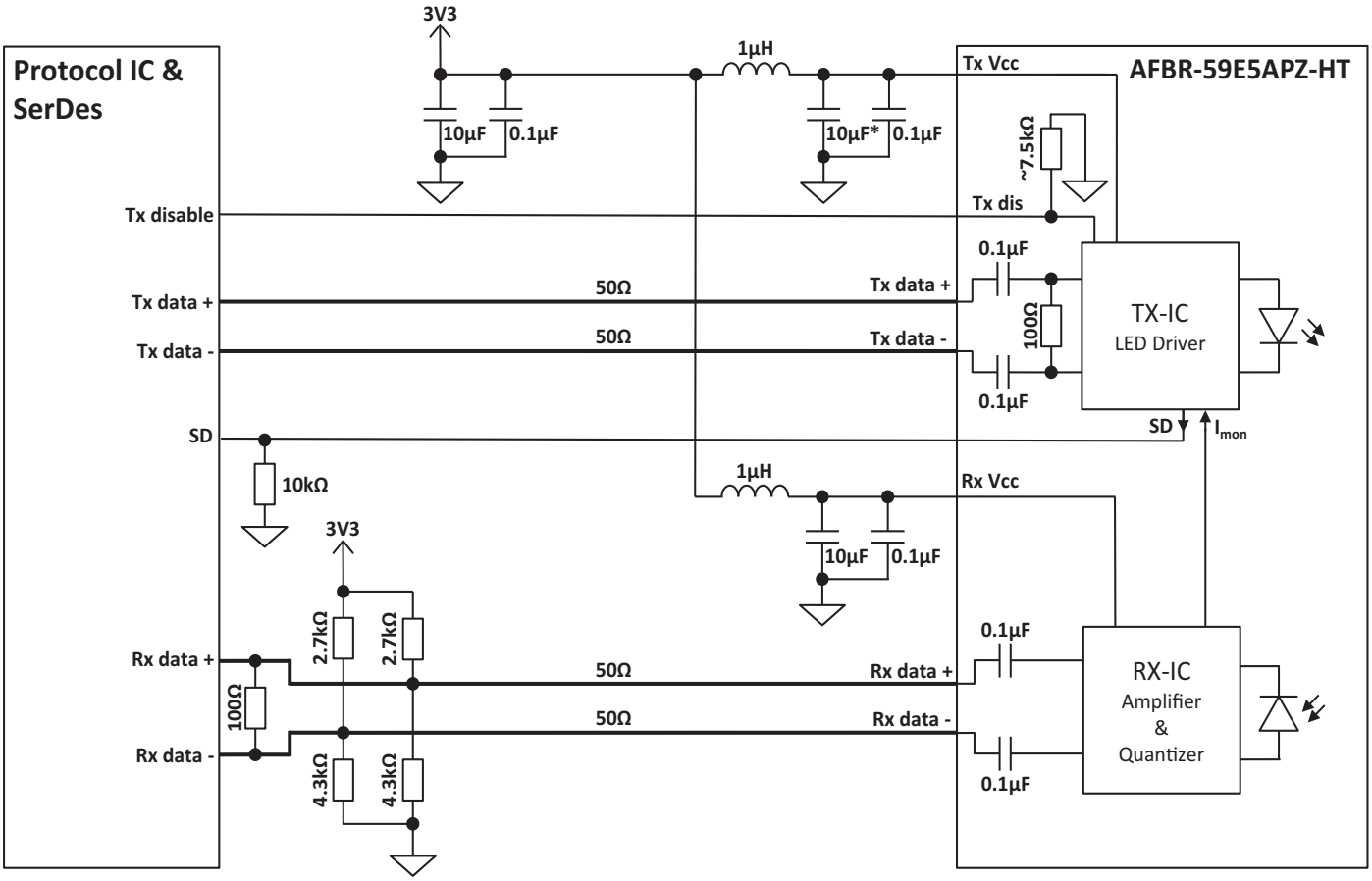
For additional information regarding EMI, ESD, and conducted noise testing procedures and results, refer to *Application Note 1166, Minimizing Radiated Emissions of High-Speed Data Communications Systems*.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	HBM: ANSI/ESDA/JEDEC - JS-001-2017	Withstand ± 2000V pulses, applied according the human-body model (HBM).
Electrostatic Discharge (ESD) to the LC Receptacle	EN/IEC 61000-6-2 (Base standard: EN 61000-4-2)	Typically withstand a 9-kV shot without damage when the LC connector receptacle is contacted by an ESD simulator with a discharge network (150 pF / 330Ω). Typically withstand a 15-kV air discharge shot on the LC connector receptacle.
Electromagnetic Interference Immunity	EN/IEC 61000-6-2:2019 (Base standard: EN 61000-4-2)	Typically show no bit errors while a 10V/m field swept from 80 MHz to 1 GHz is applied, while the transceiver is mounted to a test PCB without a chassis enclosure.
Electromagnetic Emission	EN55032:2015, CISPR32:2015 (Base standard: EN 55016-2-3)	Typically show a high margin to the emission limits at a test range from 30 MHz to 1 GHz, while the transceiver is mounted to a test PCB without a chassis enclosure.
Eye Safety	EN IEC 62368-1, EN 60825-1, EN 60825-2	Compliant with Laser Class 1. TÜV Certification: R 50486881
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	Compliant. UL File #: E173874
RoHS	RoHS Directive	Compliant to RoHS Directive 2011/65EU Annex II.

For further information, contact your Broadcom sales representative.

Figure 2: Recommended Application Circuit



* Optional capacitance (tantalum capacitor) is recommended.

NOTES:

1. Refer to the SerDes supplier's recommendation regarding the interface between the AFBR-59E5APZ-HT and the SerDes. The proposed termination is a general recommendation for AC-coupled LVPECL signals. Other terminations may apply depending on the SerDes interface.
2. Inductors should have less than a 1Ω series resistor per MSA.
3. Tx disable has an internal pull-down resistor.
4. For the Signal Detect SD, termination by a single 10-kΩ pull-down resistor is recommended. The use of another termination (such as a Thevenin equivalent LVPECL) increases power consumption and must be verified for each application.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	–40	+100	°C	—
Lead Soldering Temperature	T_{sold}	—	260	°C	a
Lead Soldering Time	t_{sold}	—	10	s	—
Supply Voltage	V_{CC}	–0.5	3.63	V	—
Data Input Voltage	V_I	–0.5	V_{CC}	V	—
Differential Input Voltage (pk-pk)	V_D	—	1.9	V	—

a. The Moisture Sensitivity Level is MSL-1.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Case Operating Temperature	T_C	–40	—	+95	°C	a, b
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	—
Data Output Load	R_L	—	100	—	Ω	Differential
Signaling Rate	B	—	125	—	Mbaud	c

a. The case temperature is measured at the transceiver topside surface using a thermocouple connected to the housing.

b. Electrical and optical specifications of the product are guaranteed across the recommended case operating temperature.

c. Fast Ethernet 4B/5B. Ethernet auto-negotiation pulses are not supported.

The following characteristics refer to AFBR-59E5APZ-HT parts that have been tested in the recommended application circuit (Figure 2). The typical data in the following tables represents the average values taken during the product characterization, measured at a case temperature of 25°C and a supply voltage of 3.3V.

Transmitter Electrical Characteristics

–40°C to +95°C, 3.0V < V_{CC} < 3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Current	I_{CC}	—	45	80	mA	—
Power Dissipation	P_{DISS}	—	149	288	mW	—
Differential Input voltage	V_{DIFF}	0.8	1.0	1.6	V	a
Input Differential Impedance	R_{IN}	—	100	—	Ω	b
Transmitter Disable High Level	V_{IH}	2.0	—	V_{CC}	V	c

a. Peak to peak.

b. Tx data inputs are AC-coupled.

c. The transmitter is enabled when Pin 8 is connected to GND or left OPEN. The transmitter is disabled when Pin 8 is connected to the HIGH level.

Receiver Electrical Characteristics

–40°C to +95°C, 3.0V < V_{CC} < 3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Current	I_{CC}	—	35	50	mA	—
Power Dissipation	P_{DISS}	—	116	180	mW	—
Data Output: Diff. Output Voltage (RD±)	$\|V_{OH} - V_{OL}\|$	0.4	—	2.0	V	a, b
Data Output Rise Time (10%–90%)	t_r	—	—	2.2	ns	—
Data Output Fall Time (90%–10%)	t_f	—	—	2.2	ns	—
Signal Detect Output Voltage – Low	SDV_{OL}	—	—	V_{CC} – 1.62	V	—
Signal Detect Output Voltage – High	SDV_{OH}	V_{CC} – 1.02	—	—	V	—

a. Differential output voltage is internally AC-coupled. The low and high voltages are measured using 100Ω differential termination.

b. RD+ and RD- outputs are squelched at SD deassert levels.

Transmitter Optical Characteristics

–40°C to +95°C, 3.0V < V_{CC} < 3.6V

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	P_O	–20	–16.5	–14	dBm	a, b
Output Optical Power 50/125 µm, NA = 0.20 Fiber	P_O	–23.5	–19.5	–14	dBm	a, b
Extinction Ratio	ER	10	—	—	dB	—
Center Wavelength	λ_C	1270	1308	1380	nm	—
Spectral Width – FWHM	$\Delta\lambda$	—	147	—	nm	—
Optical Rise Time (10%–90%)	t_r	0.6	1.0	3.0	ns	—
Optical Fall Time (90%–10%)	t_f	0.6	1.0	3.0	ns	—
Duty Cycle Distortion Contributed by the Transmitter	DCD	—	—	0.6	ns	c, d
Data Dependent Jitter Contributed by the Transmitter	DDJ	—	—	0.6	ns	c
Random Jitter Contributed by the Transmitter	RJ	—	—	0.69	ns	c, e

a. Optical values are measured over the specified operating voltage and temperature ranges. The average power can be converted to a peak value by adding 3 dB.

b. Average.

c. Characterized with a 125-Mbaud, $PRBS2^7$-1 pattern.

d. Duty cycle distortion contributed by the transmitter is measured at 50% of the threshold of the optical signal.

e. Peak to peak.

Receiver Optical and Electrical Characteristics

–40°C to +95°C, 3.0V < V_{CC} < 3.6V

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Input Optical Power	P_{IN}	–31	—	–14	dBm	a, b
Operating Wavelength	λ_R	1270	—	1380	nm	—
Duty Cycle Distortion Contributed by the Receiver	DCD	—	—	0.4	ns	c, d
Data Dependent Jitter Contributed by the Receiver	DDJ	—	—	1.0	ns	d
Random Jitter Contributed by the Receiver	RJ	—	—	2.14	ns	d, e
Signal Detect – Assert	SD_A	—	—	–31	dBm	b
Signal Detect – Deassert	SD_D	–45	—	—	dBm	b
Signal Detect – Hysteresis	$SD_D – SD_A$	0.5	2	—	dB	—
Signal Detect Assert Time (Off to On)	SD_{on}	0	—	100	µs	f
Signal Detect Deassert Time (On to Off)	SD_{off}	0	—	350	µs	g

a. This specification is intended to indicate the performance of the receiver section when optical input power signal characteristics are present per the following definitions:
   1. Over the specified operating temperature and voltage ranges.
   2. Bit error rate (BER) is better than or equal to 1×10^{-10}.
   3. The transmitter operates to simulate any crosstalk present between the transmitter and receiver sections of the transceiver.
   4. Fiber: 62.5/125 µm, NA = 0.275; or 50/125 µm, NA = 0.20.

b. Average.

c. Duty cycle distortion contributed by the receiver is measured at 50% of the threshold of the electrical signal.

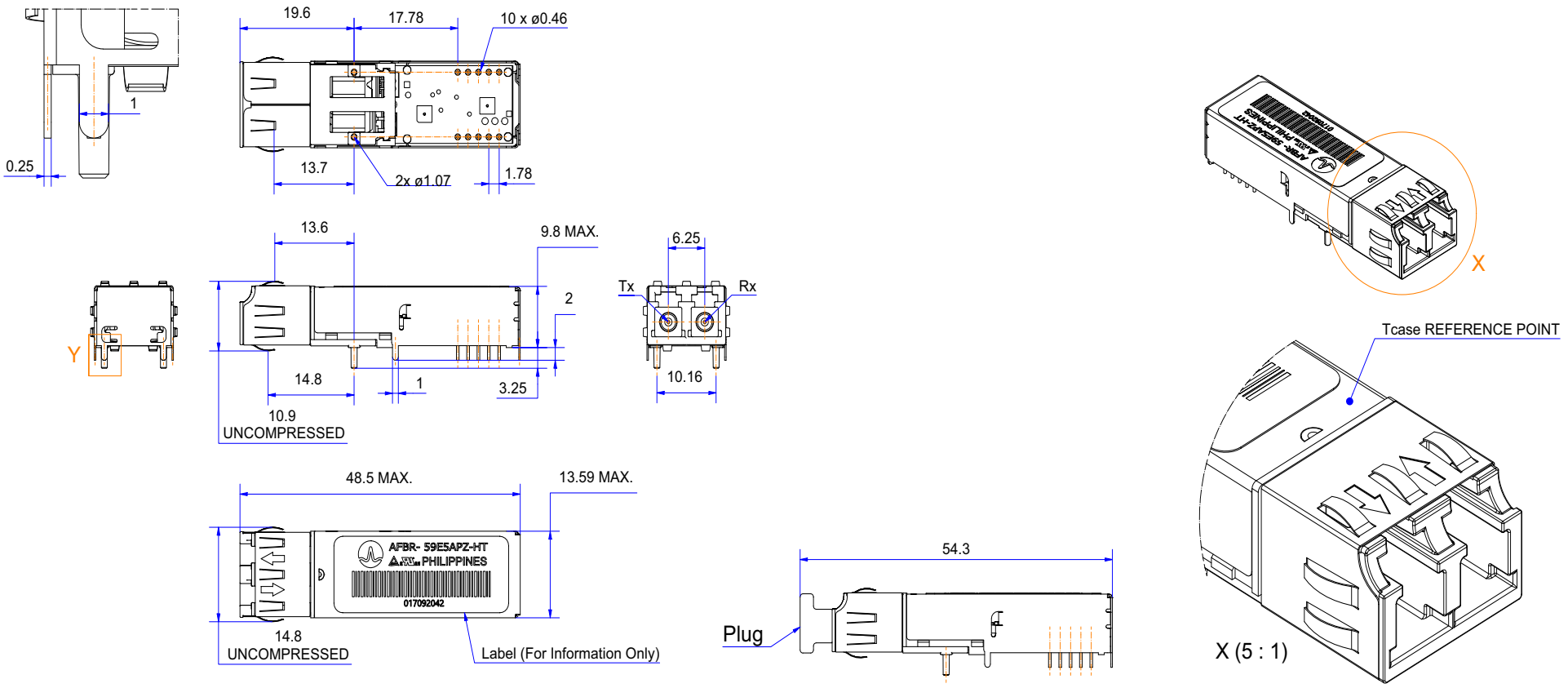
d. Characterized with a 125-Mbaud, $PRBS2^7$-1 pattern.

e. Peak to peak.

f. Signal detect output shall be asserted within the specified time after a step increase of the optical input power.

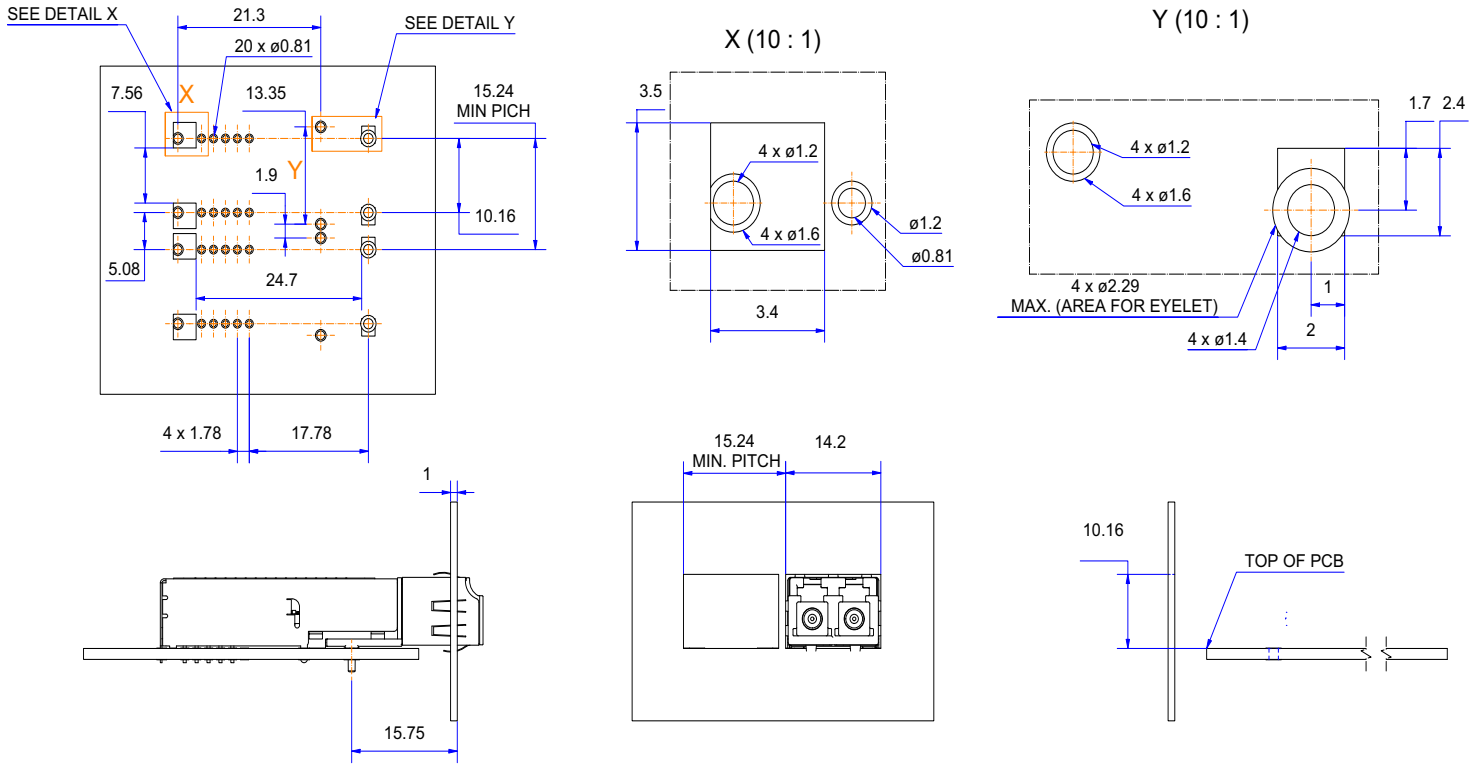
g. Signal detect output shall be deasserted within the specified time after a step decrease of the optical input power.

Figure 3: Package Outline Drawing



NOTE: All dimensions are in millimeters.

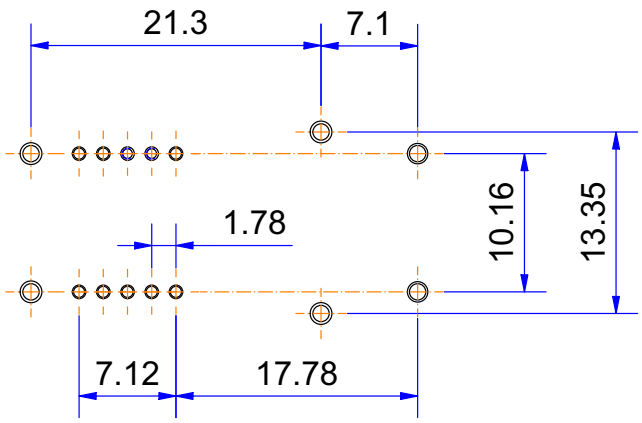
Figure 4: Recommended Board Layout Hole Pattern



NOTES:

1. This page describes the recommended circuit board footprint and front panel openings for SFF transceivers.
2. The rectangular details (as described; X and Y) are keep-out areas that are reserved for housing standoffs. No metal traces are allowed in keep-out areas.
3. Holes for mounting studs must not be tied to signal ground; they should be tied to chassis ground.
4. Holes for housing leads are required for the AFBR-59E5APZ-HT. Their positions deviate from the Common Transceiver Footprint hole pattern defined in the multisource announcement.
5. All dimensions are in millimeters.

Figure 5: Recommended Footprint (Top View)



NOTE: All dimensions are in millimeters.

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