1 Introduction

This document is intended for systems design engineers incorporating the USB 3380 PCI Express-to-SuperSpeed USB bridge into a system hardware design. It provides a handy list of basic design checks covering schematic and printed-circuit board (PCB) layout designs. Including these checks as part of your design review can help insure that important details are not overlooked when your design is committed to hardware, thereby improving your chances for a successful bring-up. In preparation for your design review, we also recommend that you check our website, www.plxtech.com, and download the most current technical specifications, errata, and related documentation. This document supersedes and replaces previously dated versions.

2 Schematic Design Checks

This section includes checks on basic elements of the circuit design, including schematic symbol, power supply, configuration straps, clocks, reset, configuration serial EEPROM, I2C, JTAG, GPIO, and other signals. All power and signal pins on the device are covered.

2.1 Schematic Symbol

For designers using ORCAD schematic capture tools, an ORCAD symbol library is available on the PLX website at www.plxtech.com. This library symbol is pre-checked by PLX engineers.

For designers not using the PLX-supplied schematic symbol, we highly recommend double-checking your symbol's signal pin names and numbers for accuracy before using the symbol in your schematic design.

2.2 Power Supply

2.2.1 Regulated DC Supply Voltages

The USB 3380 requires the following regulated DC voltages:

- 1.0 Volts (0.95V – 1.10V) - Powers digital and analog core logic. As of this writing, the estimated current requirement for all 1.0V supplies is 686 mA max.
- 3.3 Volts, +/- 0.3V - Powers external I/O signals and SerDes analog circuits. As of this writing, the estimated current requirement for all 3.3V supplies is 81mA max.

2.2.2 Power Supply Sequencing Requirements

The 1.0V and 3.3V supplies can be sequenced in any order. No special hardware is required to control the order in which the power supply rails power up and down. It is recommended that both supplies be powered up or down together.

2.3 Power, Ground Pin Connections

Signal Name	Pin #	Signal Type	Checked	Recommendations
IO Power Pins (3.3V)				In the simplest applications, all 3.3V supply pins can be powered from a common 3.3V DC voltage source. See the USB 3380 EVB schematic for a reference circuit including recommended supply bypass cap networks.
PEX_VDDA_P0 PEX_VDDA_P2 USB_VDDA	17 69 73	APWR	YES ☐ NO ☐ UNKNOWN ☐	**3.3V Power for SerDes Analog Circuits (3 Pins)** Filtered from main 3.3 Volt supply (VDD_IO). See USB 3380 example schematic for filter circuit. *Note: In PCI Express adapter mode applications, if standby power is implemented ($D3_{cold}$), power for these pins should be derived from the VAUX_IO supply.*
VDD_IO	40, 50, 59, 63	IOPWR	YES ☐ NO ☐ UNKNOWN ☐	**3.3V Power for Digital IO Circuits (4 Pins)** Main 3.3 Volt supply for digital I/O circuits. ***Important Note*:** Data Sheet version 1.2 corrects pin 34 as VAUX_IO. Designs powering VDD_IO and VAUX_IO supplies separately may be impacted by this change.
VAUX_IO	25, 34, 85	IOPWR	YES ☐ NO ☐ UNKNOWN ☐	**3.3V Auxiliary Power Supply (3 Pins)** For PCI Express Adapter mode applications, if stand-by power is implemented ($D3_{cold}$), this power supply should be derived from Vaux (3.3V). Otherwise, connect these pins to the main 3.3V (VDD_IO) supply.
USB_VDD33	6	PWR	YES ☐ NO ☐ UNKNOWN ☐	**3.3V Power for USB Digital Circuits** Connect to main 3.3V I/O supply (VDD_IO). *Note: In PCI Express adapter mode applications, if standby power is implemented ($D3_{cold}$), connect this pin to the VAUX_IO supply.*
USB_AVDD33	1	APWR	YES ☐ NO ☐ UNKNOWN ☐	**3.3V Power for USB Analog Circuits** This power supply should be derived from the main 3.3V (VDD_IO) supply through a filter circuit. See the USB 3380 RDK schematic for an example filter circuit. *Note: In PCI Express adapter mode applications, if standby power is implemented ($D3_{cold}$), power for these pins should be derived from the VAUX_IO supply.*
Core Logic, SerDes, and PLL Power Pins (1.0 V)				In the simplest applications, all 1.0V supply pins can be powered from a common 1.0 V DC voltage source. See the USB 3380 RDK schematic for a reference circuit including recommended supply bypass cap networks.

Signal Name	Pin #	Signal Type	Checked	Recommendations
PEX_VDDD0_P0 PEX_VDDD0_P2 USB_VDDD0 PEX_VDDD1_P0 USB_VDDD1	15 71 75 12 78	DPWR	YES ☐ NO ☐ UNKNOWN ☐	**Power for SerDes Digital Circuits (5 Pins)** Filtered from the main 1.0V supply (VDD_CORE). See example schematic for filter circuit. *Note: In PCI Express adapter mode applications, if standby power is implemented ($D3_{cold}$), power for these pins should be derived from the VAUX_CORE (1.0V) supply.*
PLL_AVDD	42	PLLPWR	YES ☐ NO ☐ UNKNOWN ☐	**Power for Internal PLL Circuit** This pin supplies power to the internal PLL. As such it is sensitive to noise, and should be filtered from the main 1.0V supply (VDD_CORE) to reduce noise. See the USB 3380 example schematic for an example filter circuit.
VDD_CORE	39, 41, 52, 62, 67	CPWR	YES ☐ NO ☐ UNKNOWN ☐	**Power for Core Logic (5 pins)** Main 1.0V supply for digital core logic.
VAUX_CORE	18, 72	CPWR	YES ☐ NO ☐ UNKNOWN ☐	**Auxiliary Core Logic Supply (2 pins)** For PCI Express adapter mode applications, if stand-by power is implemented ($D3_{cold}$), power for these pins should be derived from the slot Vaux (3.3V) supply. Otherwise, connect these pins to the VDD_CORE supply.
Ground Pins				Connect all Ground pins below directly to Ground (CENTER_PAD).
PLL_AGND	43	GND	YES ☐ NO ☐ UNKNOWN ☐	**Connect to Ground**
PEX_VSSA_P0 PEX_VSSA_P2 USB_VSSA	16 70 74	GND	YES ☐ NO ☐ UNKNOWN ☐	**Connect to Ground (3 pins)**
PEX_VSSD0_P0 USB_VSSD0 PEX_VSSD1_P0 USB_VSSD1	11 79 8 82	GND	YES ☐ NO ☐ UNKNOWN ☐	**Connect to Ground (4 pins)**
USB_AVSS	3	GND	YES ☐ NO ☐ UNKNOWN ☐	**Connect to Ground**
USB_PVSS	4	GND	YES ☐ NO ☐ UNKNOWN ☐	**Connect to Ground** Connects also to USB_RREF via external resistor.

Signal Name	Pin #	Signal Type	Checked	Recommendations
VSS	29, 32	GND	YES ☐ NO ☐ UNKNOWN ☐	**Ground (2 Pins)** Connect to Ground
THERMAL_GND	CENTER PAD	GND	YES ☐ NO ☐ UNKNOWN ☐	**Connect to Ground** See package drawing for pad dimensions.

2.4 Clocks

2.4.1 Clock Source and Line Termination

REFCLK Source	Signal Type	Checked	Requirements
External REFCLK Clock Transmitter	External-CML	YES ☐ NO ☐ UNKNOWN ☐	Frequency Tolerance: ± 300 ppm, max. 33 Ω series (in-line) and 49 Ω shunt (to GND) required on each differential signal, near the clock source.

2.4.2 Clock Input Pins – 2 Pins

Signal Name	Pin #	Signal Type	Checked	Recommendations
PEX_REFCLKn , PEX_REFCLKp	37 36	CML Input	YES ☐ NO ☐ UNKNOWN ☐	**100 MHz PCI Express Reference Clock input pair. (2 pins)**

2.5 Reset

Signal Name	Pin #	Signal Type	Checked	Recommendations
PEX_PERST#	24	I	YES ☐ NO ☐ UNKNOWN ☐	**PCI Express Reset** Used to initiate a fundamental reset. This reset is propagated to all downstream ports. Adapter card designs connect this pin directly to the PCI Express slot PERST# pin. For Root Complex mode applications, this pin should be driven from a power-on reset circuit. PEX_PERST# should remain asserted for 100 ms after power supplies and clocks are stable.

2.6 Configuration Straps

These pins should be pulled High (H) to VDD_IO, Low (L) to Ground, or left unconnected, as indicated. Recommended value for pull-up/pull-down resistor is 4.7K Ohms unless otherwise noted.

Signal Name	Pin #	Signal Type	Checked	Recommendations
STRAP_DEBUG_SEL#	22	I PU	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** This signal can be left unconnected in normal applications. If this ball is connected to a board circuit trace, it must be externally pulled up to VDD_IO.
STRAP_LEGACY	66	I PU	YES ☐ NO ☐ UNKNOWN ☐	**USB Legacy Mode Select** When pulled high or left unconnected, the device operates in Legacy Adapter mode. Pull or tie to Ground (VSS) to enable Enhanced Adapter mode. See the data book for details.
STRAP_PLL_BYPASS#	65	I PU	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** This signal can be left unconnected in normal applications. If this ball is connected to a board circuit trace, it must be externally pulled up to VDD_IO.
STRAP_PORTCFG	58	I PD	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Do not connect this pin to board circuit traces.
STRAP_PROBE_MODE#	19	I PU	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** This signal can be left unconnected in normal applications. If this ball is connected to a board circuit trace, it must be externally pulled up to VDD_IO.
STRAP_RC_MODE	57	I PD	YES ☐ NO ☐ UNKNOWN ☐	**Root Complex Mode Enable** Must be externally pulled High to VDD_IO or Low to Ground. High: USB 3380 functions as PCI Express Root Complex, with all PCI Express lanes presenting downstream port(s). Low (or N/C): PCI Express Port 0 is upstream-facing, and USB 3380 is enumerated by an external PCI Express Root Complex.
STRAP_SERDES_MODE_EN#	56	I PU	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** This signal can be left unconnected in normal applications. If this ball is connected to a board circuit trace, it must be externally pulled up to VDD_IO.
STRAP_SSC_CENTER#	64	I PU	YES ☐ NO ☐ UNKNOWN ☐	**SuperSpeed USB Center-Spread Clock** For most applications, this pin can be left unconnected (pull high if trace attached). Can optionally be pulled low if needed to support SuperSpeed USB Hosts or Hubs that implement a non-standard center-spread reference clock.

Signal Name	Pin #	Signal Type	Checked	Recommendations
STRAP_TESTMODE[3:0]	47, 46, 45, 44	[3,1]: I, PU [2:0], I, PD	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only (4 Pins)*** STRAP_TESTMODE[3:0] select the USB 3380 clocking configuration. Supported strap settings are as follows: **HLLL: Dual clocks configuration** - PCI Express interface is clocked from PEX_REFCLKn/p input (100MHz) - PEX_REFCLK_OUT*nx/px* (100 MHz) are buffered from PEX_REFCLKn/p input - USB interface is clocked from XTAL_IN input (30 MHz) **HLLH: 30 MHz only configuration** - PCI Express and USB interfaces are clocked from XTAL_IN input (30 MHz) - PEX_REFCLK_OUT*nx/px* (100 MHz) are generated from XTAL_IN input - PEX_REFCLKn/p signals are not used (N/C). All other strap settings are ***Factory Test Only***.
STRAP_UPCFG_TIMER_EN#	38	I PU	YES ☐ NO ☐ UNKNOWN ☐	**Link Upconfigure Timer Enable** This input maps to the Debug Control register *UPCFG Timer Enable* bit. This signal and its corresponding register bit must NOT be toggled at runtime. When STRAP_UPCFG_TIMER_EN# is pulled high, the Data Rate Identifier symbol in the TS Ordered-Sets always advertises support for both the 5 GT/s (Gen 2) data rate and Autonomous Change. When STRAP_UPCFG_TIMER_EN# is pulled low, if this Link training sequence fails during the Configuration state, the next time the LTSSM exits the Detect state, TS Ordered-Sets advertise only the 2.5 GT/s (Gen1) data rate and no Autonomous Change. The LTSSM then continues to toggle between Gen1 and Gen2 advertisement every time it exits Detect state. ***NOTE: This feature should only be enabled if a non-compliant device will not link up when these Data Rate Indentifier bits are set.*** ***(if adding an option resistor to pull this ball low, a default pull-up resistor should also be used)***

2.7 PCI Express Interface

Signal Name	Pin #	Signal Type	Checked	Recommendations
PEX_PERn PEX_PERp	10 9	CMLRn	YES ☐ NO ☐ UNKNOWN ☐	**PCI Express Receive Differential Pair** See section 2 below for PCB routing tips.
PEX_PETn PEX_PETp	14 13	CMLRp	YES ☐ NO ☐ UNKNOWN ☐	**PCI Express Transmit Differential Pair** 100 nF AC coupling caps required on all PCI Express transmit pins. See section 2 below for PCB routing tips.

2.8 USB Interface

Signal Name	Pin #	Signal Type	Checked	Recommendations
USB_DM USB_DP	5 7	I/O	YES ☐ NO ☐ UNKNOWN ☐	**High-Speed USB Interface Differential Pair** Route these signals directly to the USB cable receptacle as a differential pair. See Section 2 below for routing tips.
USB_RREF	2	A	YES ☐ NO ☐ UNKNOWN ☐	**External Reference Resistor** Connect this pin to USB_AVSS through a 1.6K Ohm +/- 1% resistor. Place resistor close to the signal pin. Keep traces as short as possible.
USB_RXM USB_RXP	80 81	CMLRn CMLRp	YES ☐ NO ☐ UNKNOWN ☐	**SuperSpeed USB Receive Differential Pair** Route these signals directly to the USB cable receptacle as a differential pair. See Section 2 below for routing tips.
USB_TXM USB_TXP	76 77	CMLTn CMLTp	YES ☐ NO ☐ UNKNOWN ☐	**SuperSpeed USB Transmit Differential Pair** 100 nF AC coupling caps required on USB_TXM and USB_TXP. Route these signals to the USB cable receptacle as a differential pair. See Section 2 below for routing tips.
USB_VBUS	88	I	YES ☐ NO ☐ UNKNOWN ☐	**VBUS Presence Detect** Connect USB_VBUS through 27K Ohms to the VBUS pin of the USB cable receptacle. Also connect USB_VBUS through 47K Ohms to Ground. *Note: When the device is not powered (VDD_IO = 0 V), the USB_VBUS pin presents a leakage path to Ground when an external USB Host is connected and driving the connector VBUS pin at 5V. This leakage current is limited by the external 27K resistor to approximately 150 uA. For designs that require zero leakage current when the device is not powered, an external FET is recommended.*

2.8.1 ESD Considerations for USB Signals

1. The ground shield of the USB receptacle should not be directly connected to the GND plane, rather a separate GND island. The GND island should be connected to the GND plane through a single zero ohm resistor.
2. Place transient suppressor components close to the USB receptacle, and return to the GND shield.

2.9 Serial EEPROM

As of this writing, a serial configuration EEPROM is ***not required*** for the USB 3380. Use of a serial configuration EEPROM in systems designs is optional. However, we highly recommend including the serial EEPROM circuit as a stuffing option, to allow inclusion of EEPROM-based performance enhancements and/or errata workarounds that may become available in the future.

2.9.1 Serial EEPROM Type

If implementing serial EEPROM, use Microchip Technology, Inc. p/n 25AA128 or equivalent for programming the USB 3380. Serial EEPROM should support 3.3V operating voltage. Power the device from the VDD_IO supply, bypassed with 0.1 uF.

2.9.2 Serial EEPROM Interface – 4 Pins

Signal Name	Pin #	Signal Type	Checked	Recommendations
EE_CS#	53	O	YES ☐ NO ☐ UNKNOWN ☐	**Serial EEPROM Chip Select Output.** Connect to EEPROM CS# input. Can be left unconnected if not used.
EE_WRDATA/EE_DI	51	O	YES ☐ NO ☐ UNKNOWN ☐	**Serial EEPROM Data Input (Write Data)** Connect to EEPROM serial data input, SI. Can be left unconnected if not used. ***Note:*** *This signal requires an external pull-up when connecting to serial EEPROM. Recommend 4.7K – 10K Ohms. Rise time of this signal is dependent on the strength of the external pull-up.*
EE_RDDATA/EE_DO	55	I/PU	YES ☐ NO ☐ UNKNOWN ☐	**Serial EEPROM Data Output (Read Data)** Connect to EEPROM serial data output, SO. Weakly pulled up. Should be externally pulled high to VDD_IO through 4.7K Ohms.
EE_SK	54	O	YES ☐ NO ☐ UNKNOWN ☐	**Serial EEPROM Clock Output** Connect to EEPROM clock input, SCK. Can be left unconnected if not used.

2.9.3 Additional EEPROM Signals

WP#: Tie to EEPROM VCC if not used, else jumper to GND to enable write-protect.

HOLD#: Tie to EEPROM VCC

2.10 Device-Specific Signals (14 Pins)

Signal Name	Pin #	Signal Type	Checked	Recommendations
CPU_RXD	60	I	YES ☐ NO ☐ UNKNOWN ☐	**8051 Serial Port Receive Data Input** Used only for applications that use the on-chip 8051 Microcontroller. Used by 8051 firmware to receive serial data from a debug console/terminal. Requires external RS-232 transceiver for connection to PC serial port. See the RDK schematic for an example. Ok to leave unconnected if not used.

Signal Name	Pin #	Signal Type	Checked	Recommendations
CPU_TXD	61	O	YES ☐ NO ☐ UNKNOWN ☐	**8051 Serial Port Receive Data Input** Used only for applications which use the on-chip 8051 Microcontroller. Used by 8051 firmware to transmit serial data to a debug console/terminal. Requires external RS-232 transceiver for connection to PC serial port. See the RDK schematic for an example.
GPIO[3:1]	27, 83, 20	I/O PU	YES ☐ NO ☐ UNKNOWN ☐	**General Purpose Input/Output (3 pins)** General Purpose I/O signal providing input, output or pulse-width-modulated (PWM) output functions for specific applications. See the data book for details on use.
MFG_AMC	23	I PD	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Do not connect this pin to board electrical paths.
MFG_TAPEN	26	I PD	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Do not connect this pin to board electrical paths.
MFG_TMC1	84	I PD	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Do not connect this pin to board electrical paths.
MFG_TMC2	87	I PD	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Do not connect this pin to board electrical paths.
LANE_GOOD#	28	I/O PU	YES ☐ NO ☐ UNKNOWN ☐	**Active-Low PCI Express Lane Linkup Status Indicator Outputs** These signals can directly drive status LEDs to indicate link Up/Down status on PCI Express lanes 1:0 (external current-limiting resistors are required). Default function is GPIO0. See the data book for details on use.
PROCMON	68	O	YES ☐ NO ☐ UNKNOWN ☐	***Factory Test Only*** Do not connect this pin to board electrical paths.
PWRON_RST#	21	I/O PU	YES ☐ NO ☐ UNKNOWN ☐	**Power-On Reset** Adapter Mode: When stand-by (Vaux) power is implemented, and where remote wake up using WAKE# or beacon signaling from D3cold power state has to be forwarded, PWRON_RST# must be held high when device is in D3cold power state. If stand-by power is not implemented, connect this signal to PEX_PERST#. Root Complex Mode: For designs not implementing stand-by power, connect PWRON_RST# together with PEX_PERST# and drive them from a power-on reset controller circuit. This circuit should insure that PWRON_RST# is held low for at least 100 ms after power and clocks are stable.
WAKE#	86	OD	YES ☐ NO ☐ UNKNOWN ☐	**PCI Express WAKE#** If standby power and remote wake are implemented, WAKE# should be pulled high (4.7K ohms) to VAUX_IO. Otherwise pull high to VDD_IO.

Signal Name	Pin #	Signal Type	Checked	Recommendations
XTAL_IN	48	I/O PU	YES ☐ NO ☐ UNKNOWN ☐	**External Crystal/Oscillator Input** Connect to a 30-MHz external crystal resonator circuit or a CMOS oscillator. See the USB 3380 RDK reference schematic for an example. When selecting a crystal, specify as follows: Nominal Frequency: 30.000 MHz Cut: AT Fundamental Frequency Tolerance: +/- 50 ppm Stability Over Temp.: +/- 100 ppm Load Capacitance: 8-18 pF ***Note:*** *Although this is an I/O signal, its logical operation is input.*
XTAL_OUT	49	O	YES ☐ NO ☐ UNKNOWN ☐	**External Crystal/Oscillator Input** Connect to a 30-MHz external crystal resonator circuit. If an external oscillator module is driving XTAL_IN, this pin can be left unconnected.

2.11 PCI Express Reference Clock Outputs

Signal Name	Pin #	Signal Type	Checked	Recommendations
PEX_REFCLK_OUTp1	30	HCSLOUT	YES ☐ NO ☐ UNKNOWN ☐	**Positive Half of Reference Clock Output Pair 1** When USB 3380 is configured as a Root Complex, PEX_REFCLK_OUTp1/n1 can be used to provide a 100 MHz reference clock for a downstream PCI Express device. In Adapter mode (STRAP_RC_MODE = Low), USB 3380 inputs reference clock by way of PEX_REFCLKp/n input pair. Note: No termination resistor networks are required for REFCLK output pairs.
PEX_REFCLK_OUTn1	31	HCSLOUT	YES ☐ NO ☐ UNKNOWN ☐	**Negative Half of Reference Clock Output Pair 1**
PEX_REFCLK_OUT_BIAS	33	A	YES ☐ NO ☐ UNKNOWN ☐	**Optional Bias Voltage Input** This pin can be left un-connected for typical applications. Suggest routing this pin to a test point.
PEX_REFCLK_OUT_RREF	35	A	YES ☐ NO ☐ UNKNOWN ☐	**External Reference Resistor** Connect this pin to Ground through a 2.00K Ohms, 1% resistor. Place resistor close to the pin.

2.12 Additional Schematic Design Considerations

2.12.1 Mid-Bus Probe Points

If your design contains embedded PCI Express links, it can sometimes be useful to add probe pads to your PCB design to allow instrumentation access to PCI Express links on the board. If you are planning to include mid-bus probe footprints in your PCB

design, be aware that they may induce jitter and/or reduce signal integrity on the PCI Express lanes it is connected to. Refer to your instrumentation vendor's specifications for specific layout design considerations.

2.12.2 Spread Spectrum Clocking (SSC)

The USB 3380 supports a Spread Spectrum REFCLK source. The SSC clock *must* originate from the PCI Express connector on a slot in the motherboard or through a common clock source that is being distributed to all add-in cards and/or PCI Express devices in the system.

If your REFCLK source is non-SSC, then you may have separate REFCLK sources on different cards or devices as long as their frequency difference is within ± 300ppm. (~30ps for a 100MHz Clock source) Refer to the USB 3380 data book for more information.

3 PCB Layout Design Checks

3.1 Routing Guidelines for PCI Express Signals

Note: The following guidelines were provided for PCI Express 2.5 GT/s (Gen 1) transmission lines. On the Gen 2 PCI Express 5.0 GT/s signaling by increasing the pre-emphasis and increasing receiver sensitivity are supposed to counteract the bandwidth related losses associated with the frequency increase. However, as frequency goes up, other discontinuities become more of a factor not just the simple channel loss. We strongly recommend you simulate and verify your design at the operating frequency. HSPICE models are available on the PLX website.

Since PCI Express links operate at very high speeds, proper PCB routing of each RX and TX pair in each lane is critical for maintaining signal integrity on each PCI Express link. The PCI-SIG provides numerous suggestions about how to correctly design PCB's containing PCI Express links. Several important guidelines for proper layout of PCI Express SerDes signals are listed below. Additional information is available from the PCI-SIG website, www.pci-sig.com.

1. Recommended Microstrip Trace Impedance:
   - Differential Impedance: 85 Ω ± 20%
   - Single ended Impedance: 55 Ω ± 15%
2. Recommended Stripline Trace Impedance:
   - Differential Impedance: 85 Ω ± 15%
   - Single ended Impedance: 55 Ω ± 15%
3. Maintain ≥ 20 mil trace edge to plane edge gap
4. Match signal trace lengths to within 5 mils. Equalize using a snaked trace near the receive end if needed, but avoid "tight bends"
5. Route signals over continuous, un-broken planes.
6. Use GND-GND stitching vias near signal vias when routing between PCB layers
7. Do not route over plane splits or voids. Allow no more than 1/2 trace width routed over via antipad
8. Match left/right turn bends where possible. No 90-degree bends or "tight" bend structures.
9. The reference clock signal pair should maintain the same reference plane for the entire routed length and should not cross any plane splits (breaks in the reference plane)
10. Reference clock terminating components should be placed as close as possible to their respective driving sources, ideally within 100 mils of the clock/receiver component pin/pin.

11. Match all segment lengths between differential pairs along the entire length of the pair.
12. Maintain constant line impedance along the routing path by keeping the same line width and line separation.
13. Avoid routing differential pairs adjacent to noisy signal lines or high speed switching devices such as clock chips.
14. Recommended reference clock differential pair spacing (clock to clock#) ≤ 11.25 mils.
15. Recommended reference clock trace spacing to other traces is ≥ 20 mils.
16. Recommended reference clock line width ≥ 5 mils.
17. When routing the 100MHz differential clock, do not divide the two halves of the clock pair between layers.
18. Recommended reference clock differential impedance: 85 Ω ± 15%
19. Recommended PCI Express reference clock to PCI express reference clock length matching to within 25 mils
20. AC Coupling Capacitors: The same package size and value of capacitor should be used for each signal in a differential pair. Refer to the *PCI Express Base Specification* for permitted values.
21. AC Coupling Capacitors: Locate capacitors for coupled traces in a differential pair at the same location along the differential traces. Place them as close to each other as possible.
22. AC Coupling Capacitors: The "breakout" into and out of the capacitor mounting pads should be symmetrical for both signal lines in a differential pair. In addition, the area under the cap footprint should be voided of metal.
23. Test points and probing structures should not introduce stubs on the differential pairs.
24. Use Low ESR, ceramic caps for lane AC-coupling.

3.2 Routing Guidelines for Super-Speed and High-Speed USB Signals

1. Super-Speed and High-Speed differential pairs should be routed directly from USB 3380 to the USB 3.0 connector receptacle using the shortest, straightest route possible. Locate the USB 3380 component close to the USB 3.0 connector. Maximum recommended trace length should not exceed 10 cm (4 in.).
2. Match differential trace lengths within 5 mils.
3. To avoid cross-talk between SS/HS pairs, maintain 20 mils minimum spacing between signal pairs and any other circuit traces. Route HS signal pairs clear of SS signal pins (and vice-versa) at the device and connector.
4. Avoid routing SS/HS signal pairs near high-speed digital circuits, switching regulators, crystal oscillators or other noise sources on the board.
5. Route differential pairs over continuous ground plane. Avoid crossing plane splits, voids, etc.
6. No 90^{o} bends in differential signal traces (emits noise). Use a round bend or two 45^{o} bends instead.
7. Recommended differential impedance is 90 Ohms +/- 10%.
8. Avoid creating trace stubs on differential signal traces by placing test points, ESD components, etc.
9. AC coupling caps on USB_TXM/USB_TXP transmit pair should be placed near the USB connector, in symmetric, not staggered fashion. Use 0.1uF, ceramic, 0402 size components.

For additional PCB layout design recommendations, refer to the Intel *High Speed USB Platform Design Guidelines, Rev 1.0*, available at the USB-IF website, http://www.usb.org/developers/docs/.

4 Assembly Guidelines for QFN Packages

USB 3380 assembly guidelines are provided in an application note entitled "QFN Surface Mount Requirements". This document is available for download in the PEX 8603 web toolbox, http://www.plxtech.com/products/usbcontrollers/usb3380. This document covers important points for proper assembly of aQFN packages, including center pad layout, stencil design, and assembly process steps. Designers should review these procedures with their assembly house to insure reliable PCB assembly.