PEX 8XXX

PLX Switches/Bridges RDK Interoperability

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Design Note

1 Purpose

This Design Note illustrates examples of different compatibility issues and variables that arise when using PCI Express Add-in Cards.

Issues are seen when PCI Express Add-in Cards like the PLX RDK's (Rapid Development Kits) for various PLX devices (Switches/Bridges) are plugged into a range of different motherboards with PCI Express Slots capable of X1, X4, X8 or X16 Lanes.

This document's emphasis is mainly on the compatibility issues related to the customization of several flags within the System BIOS CMOS variables which changes the behavior of the Serial Link on the PCI Express Slots.

2 Overview

The scope of this document is to discuss the several CMOS variables that were seen on a list of different Desktop/Server type Root Complex-based motherboards during the interoperability tests at PLX. The Root Complexes were from vendors such as Intel, Via, Nvidia, ULi, and ATI.

This will serve as an example to illustrate the different compatibility issues in a wide variety of Motherboards that are available in the Market.

3 Core System BIOS

In the PC industry, there are three core System BIOS vendors: American Megatrends (AMI), Phoenix Technologies, and Award Software International. Due to a Merger and Acquisition, Phoenix Technologies and Award Software International are a single company now. AMI and Phoenix Technologies provide licenses with core BIOS versions which support different chipsets available from Intel, AMD, Via, SIS, Nvidia, ATI and PC Motherboard Manufacturers.

Apart from the aforementioned companies, the following are the leading OEM's that develop there own System BIOS versions in-house, such as Dell Computers, IBM and HP.

4 Major Motherboard Vendors

The following is a table that lists the cross reference of the major Motherboard vendors with different core system BIOS versions used:

For Example, if you get a motherboard from ASUS, the System BIOS core used on this motherboard will be from AMI.

S. No.	Motherboard Vendor	Core System – BIOS Version Used	Comments
1	ASUS	AMI	All ASUS Motherboards use AMI Core BIOS
2	TYAN	AMI	All TYAN Motherboards use AMI Core BIOS
3	INTEL	AMI	All INTEL Motherboards use AMI Core BIOS
4	ABIT	Award-Phoenix	All ABIT Motherboards use Award-Phoenix Core BIOS
5	GIGABYTE	Award-Phoenix	All GIGABYTE Motherboards use Award-Phoenix Core BIOS
6	MSI	Award-Phoenix	All MSI Motherboards use Award-Phoenix Core BIOS
7	SuperMicro	Award-Phoenix	All SuperMicro Motherboards use Award-Phoenix Core BIOS.

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S. No.	Motherboard Vendor	Core System – BIOS Version Used	Comments
8	**DELL Systems** ▪ Optiplex Desktop ▪ Dimension Desktop ▪ Precision-Workstation ▪ Poweredge-Server	Dell proprietary developed system BIOS version	All Dell Systems use proprietary system BIOS versions.

5 Different System BIOS'- CMOS Variables

5.1 PHOENIX-AWARD DESKTOP BIOS

5.1.1 SSC - Spread Spectrum Clocking [Enable/Disable]

The data rate can be modulated from +0% to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30 kHz - 33 kHz. The +/- 300 ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600 ppm difference.

For most implementations, both ports require the same bit rate clock source when the data is modulated with an SSC. The PLX Bridge and Switch RDK's may not work in motherboards with SSC; the symptom will be that the RDK will not link up within a given Motherboard/PC System. Please disable SSC from the BIOS CMOS.

5.1.2 PCI Express Root Port Function

1. PCI Express Slot 1 – Auto; Enabled; Disabled
2. PCI Express Slot 2 – Auto; Enabled; Disabled
3. PCI Express Slot 3 – Auto; Enabled; Disabled

Some of the slots from the Root Port on the Motherboard/PC are disabled from the System BIOS as a CMOS option as described with the above options. If the PLX Bridge or Switch PCIe RDK's are plugged into these slots, they may not link up.

5.1.3 Initial Display First Function [PCI Slot/PCIe Slot]

This is an option for the Graphics Card. The X16 slot on a Motherboard/PC is dedicated to the Graphics Card if the above option is selected as a PCIe Slot. If the PLX Bridge or Switch PCIe RDK is plugged into the X16 slot, it may not link up. Some of the BIOS's will be checking for the Class Code of a graphics device.

The optional PCI Slot selects the Primary Graphics Display on a PCI slot and not on a PCIe graphics slot, this way the X16 is released to other devices.

5.1.4 PCI Express Compliancy Mode – R 1.0a/R1.0

This option will enable the PCIe Compliance Mode based on R1.0a Spec or R1.0 Base Specification.

5.1.5 Power Management Setup Functions

The following are some of the PCI Express Power Management Functions defined by the System BIOS.

PCI Express Power Management Function	**[S1 Power on-Suspend]** **[S3 (Suspend to RAM)]**
1. Wake up by PME# of PCI	**[Enable/Disable]**
2. ACPI Suspend Type	**[S3 (Suspend to RAM)]**
3. Soft-off by PWRBTN	**[Instant/off]**
4. Run VGA BIOS if S3 Resume	**[Auto/Manual]**

5.1.6 PnP/PCI Configurations:

1. PCI Express Relative Items like Maximum Payload Sizes

   [128 Bytes, 256 Bytes, … , 4096 Bytes]

These are the options for the Root Complex Maximum Payload Sizes selection. For all 9xx Intel Desktop Chipsets, 128 Bytes is the default and for the Intel Server Chipsets, 256 Bytes is the default.

2. PCI BAR above 4GB [Enable/Disable]

This selection is to enable/disable the Base Address Registers' Memory Range.

5.2 AMI DESKTOP BIOS

5.2.1 Advanced Chipset Features

Graphics Adapter Priority **- [PCI/PCI Express**]

Options:

[Internal VGA]
[PCI Express/Int. VGA]
[PCI Express/PCI]
[PCI/PCI Express]
[PCI/Int. VGA]

These are the different combinations of options selected for the Primary Graphics Display to be in the PCI Slot or in the X16 PCIe Slot or the On Board integrated Graphics Controller in the chipset.

Again, the X16 slot will be dedicated by the System BIOS for the Graphics Adapters Class Code. If we disable the PLX Bridges or Switches, the RDK will link up and work properly.

PEG Buffer Length	**[Auto: Long/Short]**
Link Latency	**[Auto; Slow; Normal]**
PEG Root Control:	**[Auto: Enabled; Disabled]**
Slot Power:	**[Auto: Light/ Normal/Heavy/Heavier]**

These are the options in the System BIOS CMOS for PCI Express Graphics Buffer Length, Link Latency, PCI Express Graphics Root Control, and Slot Power.

5.2.2 Power Management Setup:

Suspend Mode	**[Auto: S1(POS) only/S3 only]**
Report Video on S3 Resume	**[No/Yes]**
ACPI 2.0 Support	**[Yes/No]**

These are the different options for the Power Management Setup in the System BIOS CMOS settings.

5.3 AMI SERVER BIOS

5.3.1 Advanced Chipset Features

PCI CONFIG

On Board Video **[Enable/Disable]**

Primary integrated graphics controller within the chipset – Enable/Disable feature.

Boot Setting Config

Post Error Pause	**[Enable/Disable]**
Security Settings NMI	**[Enable/Disable]**

Boot Setting configurations.

5.3.2 Server

5.3.2.1 System Management

Assert NMI on SERR# **[Enable/Disable]**

Assert NMI on PERR# **[Enable/Disable]**

These are some of the System Management options for SERR# and PERR# Enable/Disable functions.

5.3.2.2 Server Console Features

BIOS Redirection Port **[Serial A/Serial B]**

ACPI Reduction Port **[Serial A/Serial B]**

The above are some of the Server Console Features for the Serial Port Direction.

5.4 OTHER BIOS ANOMALIES

1. *Some ASUS Motherboards with AMI BIOS using the PLX Bridges and Switches based RDK during BIOS enumeration will not allocate the BAR0 (Base Address Register) space. Thus when Windows OS re-enumerates with the plug and play driver, it will report Code 12, due to the System BIOS not allocating the BAR0 and thus the device does not work properly in windows.*

Workaround: AMI fixed this in the BIOS version 8.00.11. Please get an updated System BIOS from AMI or from the ASUS Motherboard vendor.

2. *RCB (Read Completion Boundary Setting) for BRIDGES*

The PEX 8111 Forward & PEX 8114 Forward, CSR bit 3 at offset 0x78h is set to default value of 1. This bit is supposed to be set by the BIOS to match the RCB of the root complex. All the BIOS versions do this. All Chipsets we have seen supporting with the RCB value of 0 (which is 64-byte Read Completion Boundary).

3. *References for Motherboard Manufacturers & System BIOS Core Vendors*

The following are the websites for the Motherboard Manufacturers and System BIOS Core Vendors:

Motherboard Manufacturers	Website
MSI	http://www.msicomputer.com/product/p_list.asp?class=mb&cpu=1
ASUS	http://usa.asus.com/prog/spec.asp?m=P5GDC-V Deluxe&langs=09
GIGABYTE	http://www.giga-byte.com/Motherboard/Default.htm
TYAN	http://www.tyan.com/
INTEL	http://www.intel.com/products/motherboard/index.htm
SuperMicro	http://www.supermicro.com/products/motherboard/
ABIT	http://www.abit-usa.com/products/mb/
DELL	http://www.dell.com/

System BIOS Vendors	Website
AMI – American Megatrends	http://www.ami.com/
Award – Award International	http://www.award-bios.com/index.cfm?refererid=35
Phoenix – Phoenix International	http://www.phoenix.com/en/Home/default.htm