BROADCOM

Product Brief

PEX88T32 Retimer

PCIe 4.0 Connectivity for Server, Storage, and Cloud Systems

PEX88T32

Key Features

- PCIe 1.0, 2.0, 3.0, and 4.0 support
- 32 bi-directional PCIe lanes: 16 lanes up and 16 lanes down
- The Industry's best SerDes technology with extended reach (up to 39 dB loss)
  - SerDes field-tested by Broadcom in various products
- Low-power SerDes (under 90 mW per lane)
- Configurable with SBR
- Cut-through packet latency of 105 ns
- DPC/eDPC support, Read tracking for surprise removal
- SSC isolation, SRIS, SRNS, and Common Clock support
- Each lane is independent of other lanes
- No reference resistors, NV RAM is programmed during test
- CTLE, 9-tap DFE equalizer to support up to 39 dB channel loss
- CDR, pre/post-cursor settings
- Lane margining and loop-back supported
- Exceeds 20 dB normal channel loss handling set by PCI-SIG

Overview

Broadcom PEX88000 switches allow customers to build systems from simple PCIe connectivity in and outside the box to high performance, low latency, scalable, cost-effective PCIe fabrics for composable hyper-scale compute systems.

For a complete eco-system with PCIe 4.0 connectivity, system designers and integrators require PCIe 4.0 switches and retimers to interconnect devices within a system and to connect PCIe sub-systems together via cables or mid/backplanes. Broadcom has taken an innovative path by re-purposing its PCIe 4.0 technology to create a retimer, the PEX88T32, to fill this market need. The PEX88T32 offers a total of 32 bi-directional PCIe 4.0 lanes where one x16 PCIe port can connect to a host and other x16 port to an I/O device, cable connector, or mid-plane. The PEX88T32 retimer uses the same field-tested device architecture and robust long-reach SerDes as the PEX88000 PCIe 4.0 Switch family.

Downstream Port Containment (DPC/ eDPC)

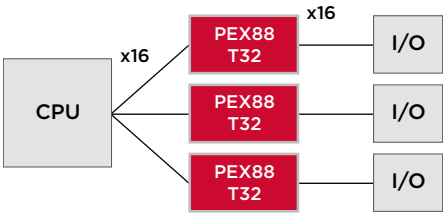
Most servers have difficulty handling serious errors in I/O devices, especially when a device disappears from the system. PEX88T32 DPC/ eDPC implementation allows a downstream link to be disabled after an uncorrectable error or time-out, making recovery possible in a controlled and robust manner. This feature can be enabled via Serial Boot ROM (SBR) code.

Improved SSC Isolation

Like PEX88000 switches, the PEX88T32 retimer allows separation of clock domains that include spread-spectrum clocking. The device also supports SRNS, SRIS, and common clock.

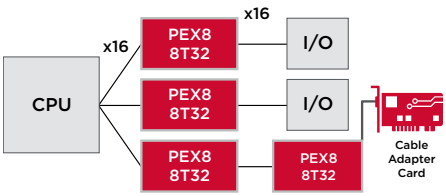
Inside-the-Box CPU to I/O Connectivity

The PEX88T32 retimer can be designed to support long channels in a server, storage system and NVMe appliance. The retimer device can be placed halfway between CPU and I/O devices to drive PCIe 4.0 signals to the other end of the boards, as shown below.



Outside-the-Box Cable Connectivity

The PEX88T32 can be used in cabled systems, where the retimer device can be mounted at the edge of the boards to connect to cable connectors or mounted on an adapter card with cable connectors.



Key Features (con't)

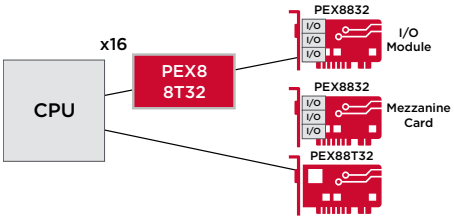
- Handles 39 dB (spec = 28 dB) loss with clean channel (5 to 11 dB margin)
- 800 mV PRBS-23 BERT + 28 dB CEM Channel + Package Loss
- Field proven debug and bring-up tools
- IBIS-AMI Models, Arctic SerDes Eyescope and other debug tools
- Reliability, availability, serviceability VisionPAK – SerDes Eye capture
- Very high jitter and interference tolerance (100% over PCIe spec)

Software Development Kit (SDK)

The PEX88T32 comes with a field-tested PCIe SDK that allows designers to read internal registers, SerDes settings, RxEye, and other data structures for debug and bring-up. Additionally, device supports classic PCIe performance monitoring and debug/testing features.

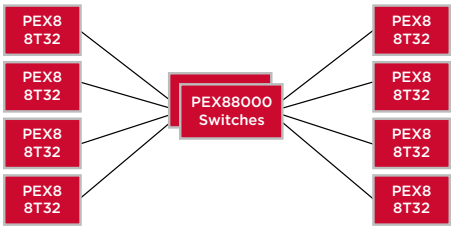
Add-in and Mezzinnine Cards

The PEX88T32 can be used to condition PCIe 4.0 signals for I/O Add-in cards and Mezzinine cards with multiple connectors in the path for system integration.



Back/Mid-Planes

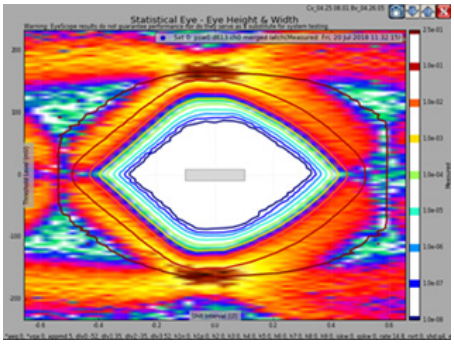
The PEX88T32 can also be used for mid-plane or backplane connectivity to create large systems.



Robust SI Clean Eye in noisy or stressed channels and high tolerance with jitter and interference, as shown below.

Prescribed PCIe 4.0 Interferers

Test Case	Compliance	Max. Before Failing	Margin
RJ	1 ps (rms)	2.1 ps (rms)	110%
Differential Interference (2.1 GHz)	31 mV	59 mV	90%



Ordering Information

Manufacturing Part Number	Description
SS08-0B00-00	PEX88T32: 32-lane PCIe 4.0 Retimer

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For more product information: broadcom.com

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