PEX 8311/SH7709 AN

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SH7709 to PEX 8311 Application Note

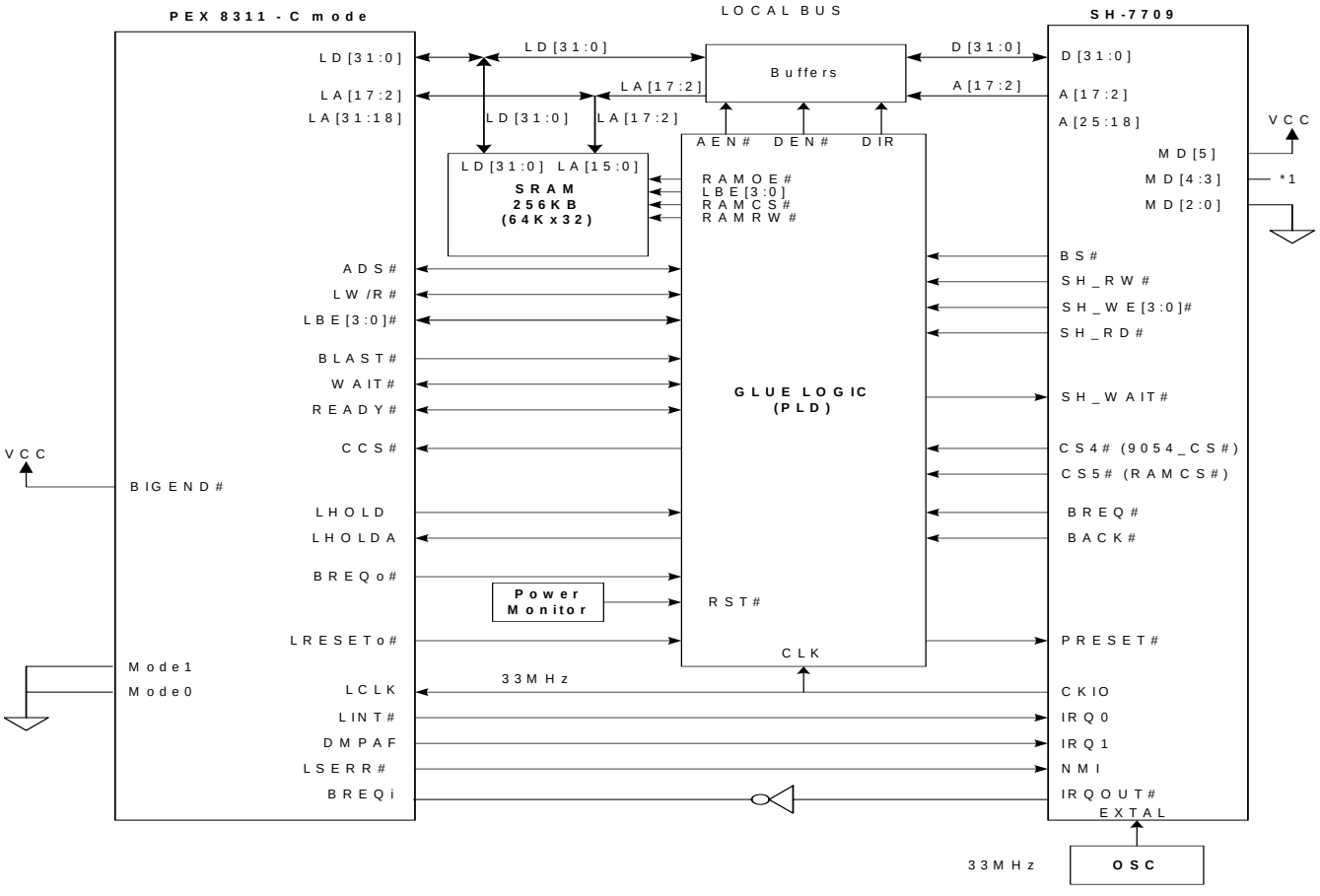
Features

- PLX Technology PEX 8311, with PCI Power Management features for adapters and embedded systems.
- Hitachi SH7709 32 bit RISC Processor
- 256KB of SRAM

General Description

PLX Technology PEX 8311, with PCI-Express Power Management features for adapters and embedded systems

The PEX 8311 has Direct Master, DMA and Direct Slave data transfer capabilities. The Direct Slave gives a master device on the PCI-Express bus the ability to access memory on the Local bus. The PEX 8311 allows the Local bus to run asynchronously to the PCI Express through the use of bi-directional FIFOs. In this design example, the PCI-Express interface runs at 2.5 GHz and the Local bus runs at 33 MHz.



Note: 1. State of these SH-7709 configuration pins are determined by the application.

Figure 1. SH7709 to PCI Subsystem

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1. INTRODUCTION

This application note describes how to interface the Hitachi SH7709 CPU to the PCI-Express interface using the PLX PEX 8311 "PCI-Express to Local bus Bridge" IC. The information can be used to build either a PCI-Express adapter or embedded system. The subsystem described in this note consists of a SH7709 connected to a PLX Technology PEX 8311 chip through “glue logic”. Figure 1, is a block diagram showing connections between the PEX 8311, PLD and SH7709.

The PEX 8311 has Direct Master (DM), DMA and Direct Slave (DS) transfer capabilities. The Direct Master mode is the mode by which the SH7709 transfers data to and from the PCI-Express interface. The Direct Master mode allows the SH7709 to access the PCI-Express interface.

The PEX 8311 also has a powerful two-channel Scatter/Gather DMA controller. They enable long and efficient burst transfers between a PCI-Express host and an adapter’s memory.

The Direct Slave mode gives a master device on the PCI-Express interface the ability to access the PEX 8311 configuration registers or memory on the Local bus. This design allows burst or single cycle direct slave transfers.

The PEX 8311 allows the Local bus to run asynchronously to the PCI-Express interface through the use of bi-directional FIFOs. In this application, the PCI-Express interface runs in 2.5 GHz and the Local bus runs at 33 MHz.

2. ARCHITECTURE

The Block Diagram of the PEX 8311/SH7709 application (Figure 1) will be discussed in the following subsections. The Local bus consists of all the signals in the application block diagram that is connected to the Buffers Block and the PLD. Only the PEX 8311 and the SH7709 can be the Local bus master. The SH7709 can access the PEX 8311 and SRAM. The PCI-Express interface, PEX 8311, and SH7709 are configured for little Endian operation. Each block is discussed in brief.

- PEX 8311 Block
  - The PEX 8311 bridges the PCI-Express interface with the Local bus.

- Buffers Block
  - The buffer provides the ability to isolate the SH7709 data and address from those of the PEX 8311 during dead lock recovery.
  - The data bus connects through the buffer D[31:0] to LD[31:0] respectively.
  - The address bus connects through the buffer A[17:2] to LA[17:2] respectively.

- OSC Block
  - The oscillator (OSC) provides a 33MHz clock to the SH7709.

- SH7709 Block
  - The SH7709 is the board CPU.
  - The SH7709 outputs on pin CKIO, a 33MHz clock to the PEX 8311 and the PLD.

- PLD Block
  - The PLD performs the glue logic functions.

- SRAM Block
  - The SRAM Block provides a common memory space for the PEX 8311 and the SH7709 for data transfers. The shared 256KB (64Kx32) SRAM needs 16 address bits and four byte enables for decoding.
  - If additional devices are to be made accessible by the PEX 8311, a PEX 8311 address decoder can be added to the PLD.

- Power Monitor Block
  - The power monitor resets the system upon initial power up and low power.

2.1 PEX 8311 Bus Mode Used

The PEX 8311 uses C mode. In C mode the PEX 8311 provides the READY# and BLAST# signals that help in interfacing with the SH7709.

2.1.1 Local Bus Arbitration

The PEX 8311 requests the Local bus by asserting HOLDA. The PEX 8311 is granted the bus when LHOLDA is asserted.

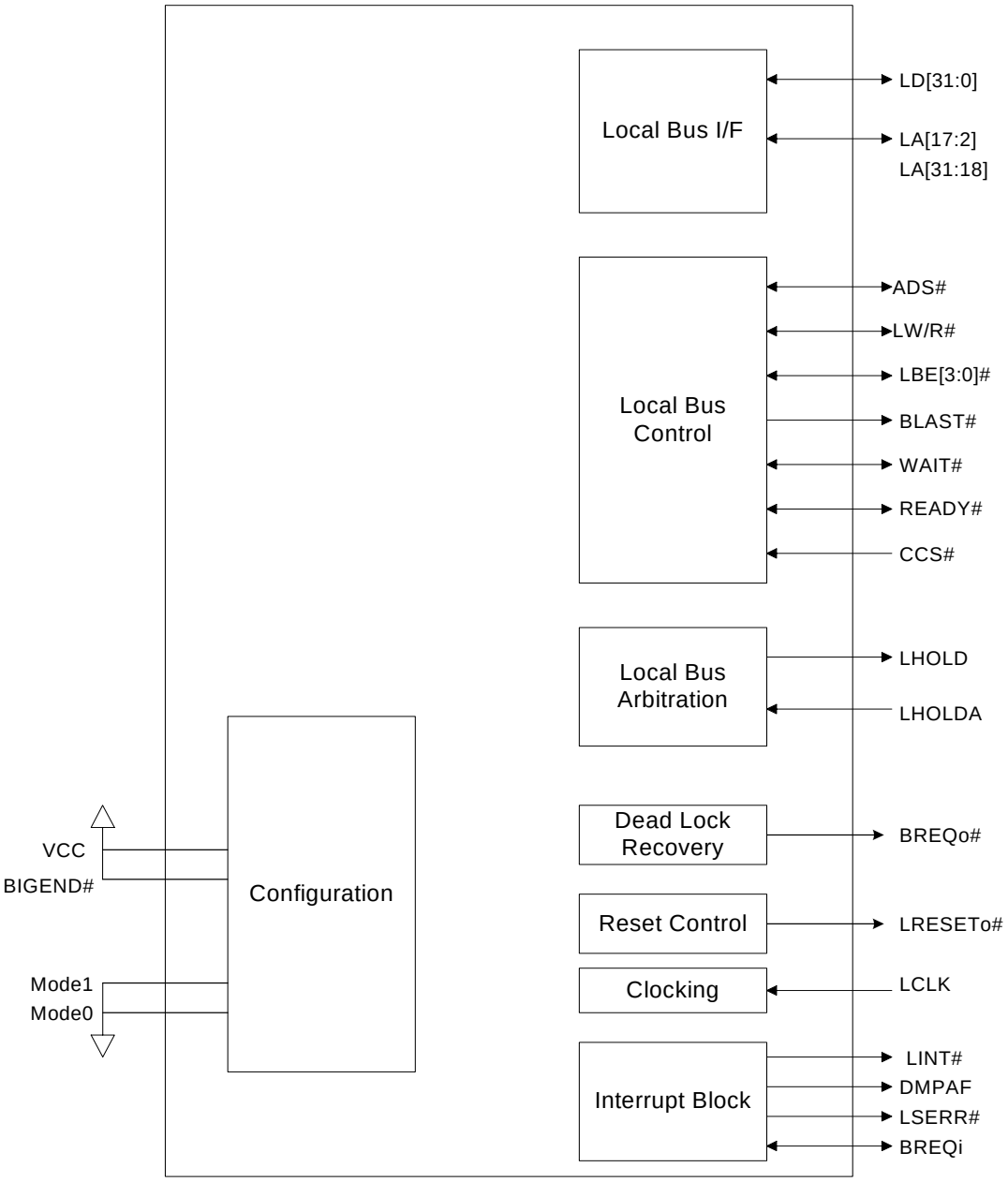

Figure 2. PEX 8311 Local Side Block Diagram

2.1.2 PEX 8311 Configuration Pins

Table 1 below shows the state of the configuration pins on the PEX 8311.

Table 1. Configuration Pins

Pin Name	Setting	Resulting Configuration
MODE [1:0]	00b	C Mode de-multiplexed address and data bus.
BIGEND#	1b	Little Endian

2.2 Control Signal Connections

The SH7709 is the board CPU. It is a powerful device with many features. Only those features relevant to this application note are described here. The SH7709 is a 32-bit RISC processor. The SH7709 block diagram (Figure 3) is described in the following sub-sections.

2.2.1 Central Processing Unit

The Central Processing Unit (CPU) is the 32-bit RISC core. It processes the address and data signals. The SH7709 has only 26 physical address lines, but the SH7709 has a virtual addressing space of 32 bits. This application requires only the 16 least significant address lines from the SH7709 to go to the SRAM Block.

2.2.2 Bus State Controller

The Bus State Controller block generates the SH7709 bus control signals.

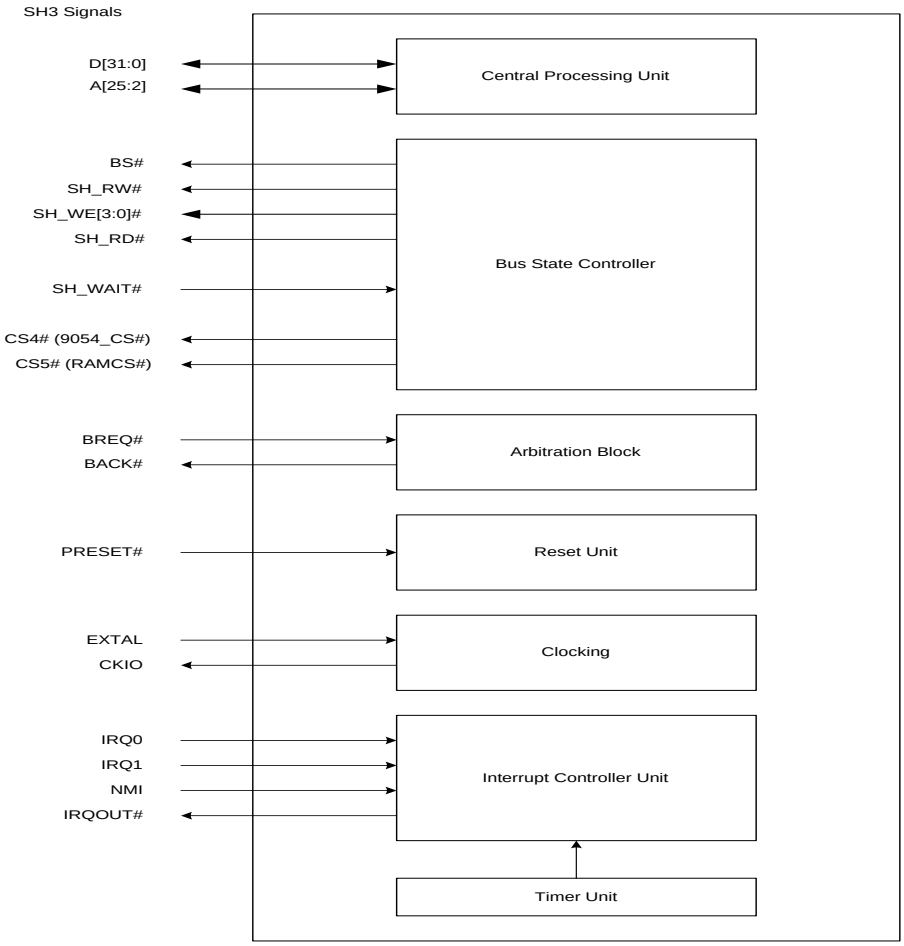

Figure 3. SH7709 Block Diagram Simplified

2.2.3 Bus Arbitration Block

In this application note the PEX 8311 and the SH7709 share the same bus.

2.2.3.1 BREQ

The SH7709 accepts bus requests from the PEX 8311 with the BREQ input. The SH7709 has no way of ending its own SH7709 bus cycle and granting the bus before its bus cycle is complete. The SH7709 may grant the bus to the PEX 8311 at the end of its current bus cycle. The SH7709 grants the bus by asserting BACK#.

2.2.3.2 BACK#

The SH7709 grants the bus to the PEX 8311 by asserting BACK# which asserts PEX 8311 LHOLDA.

2.2.4 Reset Unit

The reset unit controls device reset.

2.2.5 Clocking Unit

EXTAL is the clock input from the OSC block. The SH7709 provides a load compensated clock on the other components.

2.2.6 Interrupt Controller Unit

The SH7709 interrupt controller unit handles all interrupts from internal and external sources.

2.2.6.1 IRQOUT#

When the SH7709 gets an interrupt its SH7709 IRQOUT# signal is asserted. If the SH7709 does not have the bus at that time of the interrupt, the PLD asserts through an inverter the PEX 8311 BREQi pin. This will start bus arbitration to grant the bus to the SH7709 to perform its interrupt service routine and clear the SH7709 interrupt source. One of the SH7709 internal timers can be used to drive IRQOUT# to assure that the SH7709 gets the bus within a set amount of time.

2.2.6.2 IRQ0

The IRQ0 pin is to be programmed to trigger on the falling edge. The PCI-Express host can interrupt the application by writing to the PEX 8311 interrupt register and causing the PEX 8311 LINT# pin to be asserted. This causes the PLD to assert it's IRQ0# signal pin. This causes an interrupt in the SH7709. The SH7709 clears the interrupt source in its interrupt service route.

2.2.6.3 IRQ1

The IRQ1 pin is to be programmed to trigger on the rising edge. The PEX 8311 DMPAF pin output indicates to the SH7709 when the Direct Master FIFO level has exceeded a pre-programmed number of bytes.

2.2.6.4 NMI

The NMI pin is to be programmed to trigger on the falling edge. If the PEX 8311 detects a system error it asserts its PEX 8311 LSERR# pin which asserts the SH7709 NMI pin. Once the SH7709 gets the bus it will clear the interrupt source in its interrupt service route.

2.2.6.5 SH7709 Interrupting the PCI-Express Host

There are two options for the SH7709 to interrupt the PEX 8311. One option is for the SH7709 to write an interrupt to the PEX 8311 interrupt register. This causes 8311 to generate Assert_INTA message on the PCI-Express bus. The PCI-Express Host clears the PEX 8311 interrupt register in its interrupt service routine and Deassert_INAT message is generated.

A second possible option is for the SH7709 to interrupt the PCI-Express Host is to configure the PEX 8311 LINT# pin as an input and asserting the SH7709 output pin to assert the LINT# pin. Software is required to control the direction of the LINT# pin.

2.2.6.6 Timer Unit

The timer can be used to assure that the SH7709 requests the bus within a set amount of time by asserting the IRQOUT# pin.

2.2.6.7 SH7709 Configuration

The configuration of the SH7709 is shown in Table 2 below.

Table 2. SH7709 Configuration Table

Pin Name	Settings	Resulting Configuration
MD [5]	1b	Little Endian
MD[4:3]	Defined by the application	Area 0 data width depends on the boot memory data width. However, the boot memory is not defined in this application note
MD[2:0]	000b	Mode 0: EXTAL (input) =33MHz = CKIO (output), SH7709 CPU runs at 33MHz

2.3 Programmable Logic

The PLD block performs glue logic functions connecting the PEX 8311 and the SH7709. The following sub-sections describe the PLD Blocks.

2.3.1 Buffer Control Block

The Buffer Control Block controls the data and address buffers that give the SH7709 access to the shared memory. The address buffer is unidirectional from the SH7709 to the PEX 8311 and SRAM and is enabled by AEN#. The data buffer is bi-directional. DEN# enables the data buffer. DIR controls the direction of the data buffer.

2.3.2 SRAM Control Block

The SRAM Control Block decodes shared SRAM accessible to both the PEX 8311 and the SH7709. RAMOE# enables the SRAM for output. LBE[3:0] enables the bytes of SRAM for access. RAMCS# is provided to enable the SRAM bank (some SRAM implementation will not need this signal). RAMRW# controls whether it is a read or write access.

2.3.3 Local Bus Control Block

The Local bus Control Block decodes bus control signals from the SH7709 and the PEX 8311 and outputs hand shake signals. For example when the SH7709 accesses the PEX 8311. The Local bus Control Block drives signals to the Buffers Control to enable the buffers from the SH7709 to the PEX 8311. It asserts SH7709 WAIT# until the PEX 8311 asserts READY#.

2.3.4 Local Bus Arbitration Block

The PLD Local bus arbitration block accepts the PEX 8311 and SH7709 signals and performs Local bus arbitration between the PEX 8311 and the SH7709.

2.3.4.1 PEX 8311 Requests the Local Bus

The PEX 8311 requests the Local bus from the SH7709 by asserting LHOLD. The PLD then asserts the SH7709 pin BREQ. The SH7709 then grants the Local bus to the PEX 8311 by asserting its SH7709 BACK# pin. The PLD then asserts the PEX 8311 LHOLDA pin. The SH7709 can only grant the bus at the completion of its SH7709 bus cycle. The SH7709 cannot abort its own bus cycle before completion.

2.3.5 Dead Lock Recovery Block

When the PEX 8311 detects dead lock, it asserts its BREQo pin. This results in asserting the SH7709 WAIT# and the disabling of the Buffers Block. This isolates the SH7709 from the PEX 8311 and the SRAM. Controls of the local bus signals are transferred from the SH7709 to the PEX 8311.

This is done because the SH7709 has no way of ending its own bus cycle before it is complete. Therefore, when deadlock occurs, the PEX 8311 asserts BREQo, which results in asserting the SH7709 WAIT# pin. The PEX 8311 is granted the bus by the PLD asserting LHOLDA. The Local bus control signals, which the SH7709 was driving, are instead driven by the PEX 8311 so that the PEX 8311 can complete its bus access. Once the PEX 8311 is done, the PEX 8311 de-asserts its LHOLDA and BREQo outputs, which de-asserts the PEX 8311 LHOLDA, re-enables the Buffer Block, de-asserts SH7709 WAIT#, and restores the SH7709's driving of the Local bus.

2.3.6 Reset Control Block

The PLD Reset Control Block inputs reset from two sources, the PEX 8311 LRESETo# and the power monitor REST# signal. Either one of these conditions will reset the PLD and assert the SH7709 PRESET# pin resetting the SH7709.

2.4 Address Maps

The following sub-sections show the Local bus address maps of the PEX 8311 and the SH7709 respectively.

2.4.1 PEX 8311 Address Map

The PEX 8311 Local address map is shown in the table below for byte wide accesses. All other PEX 8311 Local bus addresses are duplicates. The PEX 8311 accesses with the SRAM can be 1, 2, or 4 bytes wide.

Table 3. PEX 8311 Address Map

Address range for byte wide access	Resource	Access
[0000,0000h – 0003,FFFCh]	SRAM	R/W

2.4.2 SH7709 Address Map

The SH7709 has programmable chip select signals among them, CS4# and CS5#, which are used for PEX 8311 and SRAM decode respectively. All other SH7709 Local bus addresses are duplicates. The SH7709 accesses with the PEX 8311 and SRAM can be 1, 2, or 4 bytes wide.

Table 4. SH7709 Address Map

Address range for byte wide access	Resource	Access
CS4# & [0000,0000h – 0000,0190h]	PEX 8311	R/W
CS5# & [0000,0000h – 0003FFFCh]	SRAM	R/W

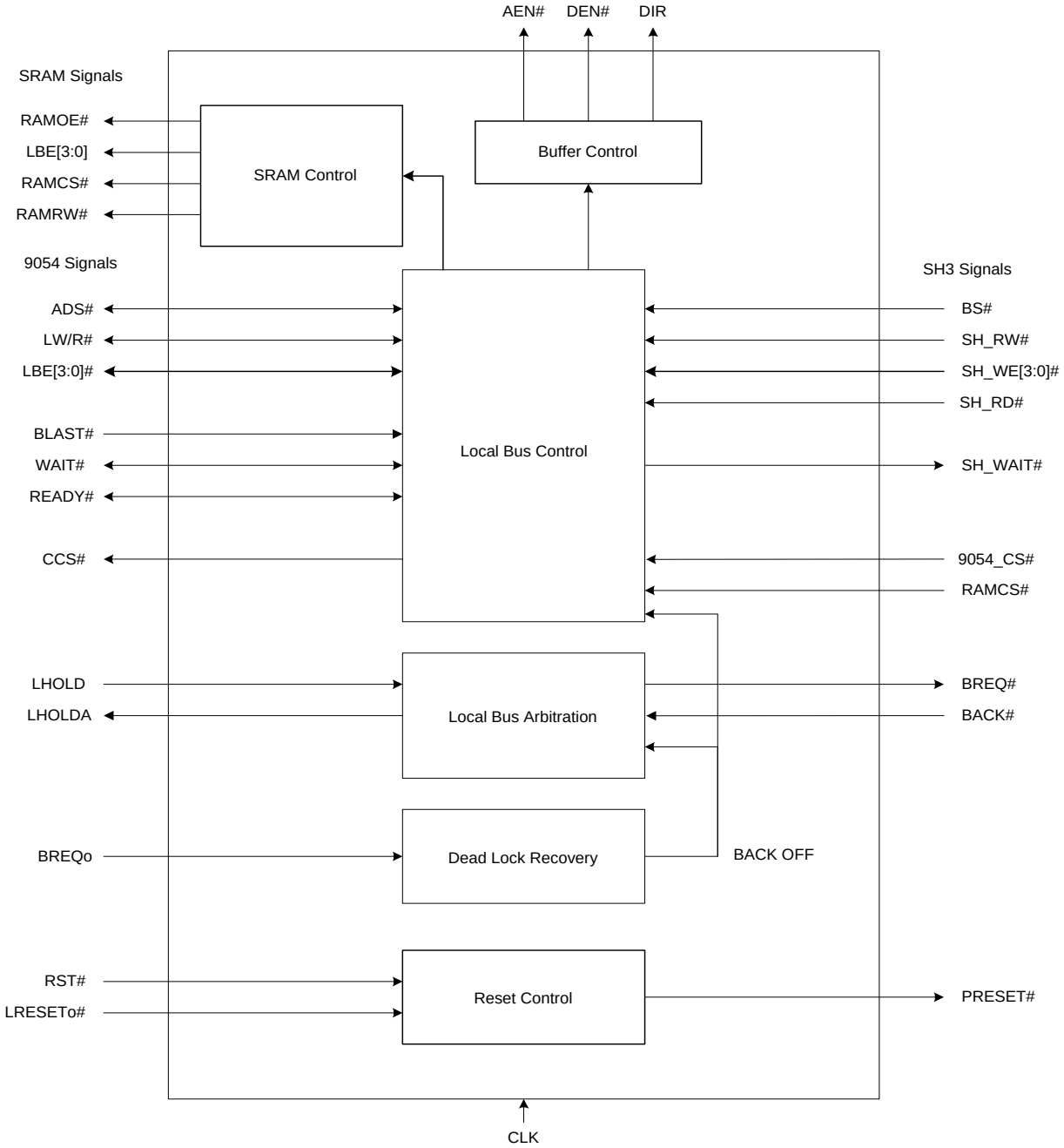

Figure 4. PLD Block Diagram

2.5 Board Reset

The board can be reset by the following methods.

1. The SH7709 writes a software reset to the PEX 8311.
2. The PCI-Express Host asserted the PERST# pin resetting the PEX 8311.
3. The PCI-Express hot reset
4. Power monitor can reset the PLD and the SH7709. The SH7709 PRESET# pin is driven by PEX 8311 LRESET# and Power Monitor RST#. Host software detects this reset condition deals with it.

3. ASSUMPTIONS

This application note is based on the following assumption:

- Some typically necessary design components (i.e. boot and code memory, EEPROM, and pull-up/down resistors) are not included in this applications note.

The designer is expected to add such components as needed.

4. REFERENCES

The following is a list of additional documentation to provide the reader with further information about the SH7709 processor.

- PEX 8311 Data Book
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