Wafer-Level Chip Scale Package (WLCSP)

OVERVIEW AND ASSEMBLY GUIDELINES

16215 Alton Parkway • P.O. Box 57013 • Irvine, CA 92619-7013 • Phone: 949-450-8700 • Fax: 949-450-8710

PACKAGING-AN300-R
12/31/03

REVISION HISTORY

Revision	*Date*	*Change Description*
PACKAGING-AN300-R	12/31/03	Initial release

Broadcom Corporation
P.O. Box 57013
16215 Alton Parkway
Irvine, CA 92619-7013

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

SCOPE

This application note provides an overview of Broadcom's WLCSP (Wafer-Level Chip Scale Package) technology and includes design and manufacturing guidelines for high yield and high reliability assembly.

WLCSP OVERVIEW

Broadcom's WLCSP technology offers a high-density, low form-factor package solution that is ideal for mobile applications which require small package footprints. The finished package is the same size as the silicon die. The technology enables a high yield implementation into high volume manufacturing environments. The WLCSP technology offers the following attributes:

- Tested bare die solution with flipchip bumps
- Provides small form factor for high degree of system miniaturization
- Ideal for mobile applications
- Compatible with conventional module design rules
- Compatible with conventional and Pb-free flipchip assembly processes

Figure 1 shows a representative picture of a WLCSP device.

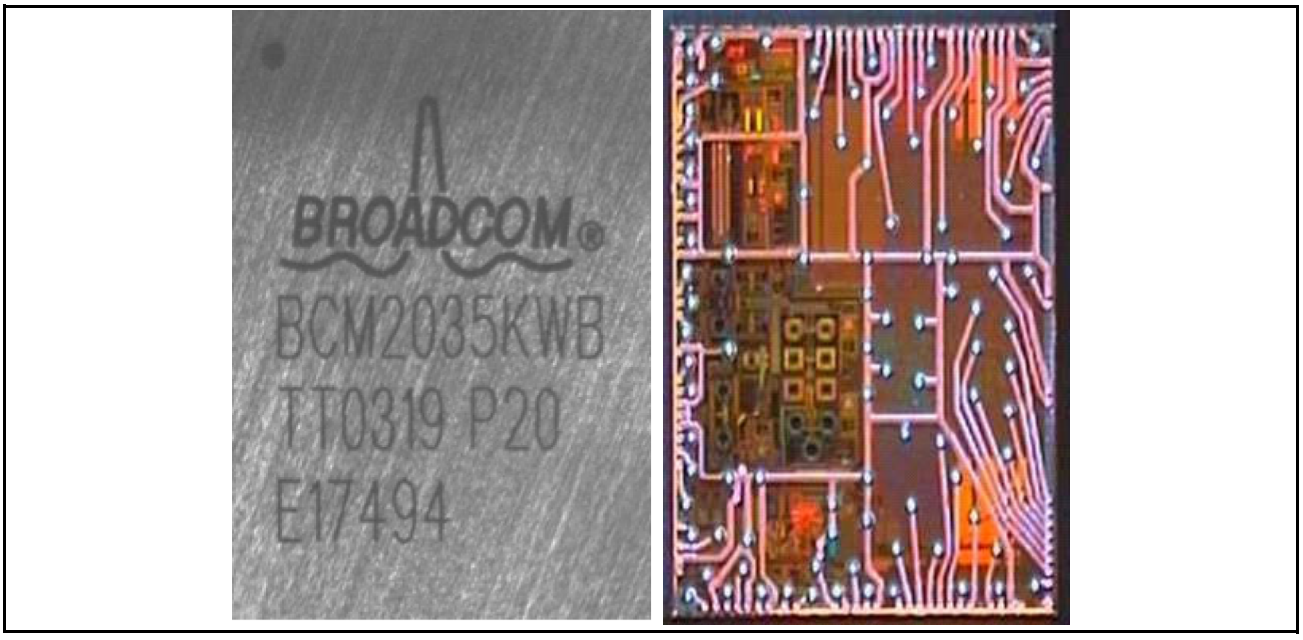

Figure 1: Top and Bottom View of WLCSP

WLCSP PROCESS OVERVIEW

As part of the WLCSP process, the native device is converted into a flipchip device. In a flipchip device, the pins are created with solder bumps that are used to solder the chip directly to the customer module or board. To create the new solder bump terminals, an additional metal layer is applied to the chip to provide connectivity from existing on-chip terminals to new solder bump terminals.

The majority of WLCSP processing is done with the device in wafer form. The general process flow for WLCSP devices is:

- Front-End Processing - The front-end process is where the additional dielectric and metal layers are applied to the chip while in wafer form to create WLCSP functionality. After the metal layers are added, solder bumps are applied to the device (still in wafer form).
- Testing - The testing process includes comprehensive functional and performance testing to ensure operational integrity.
- Back-End Processing -The back-end process is where the dies are background, laser marked, singulated, and packed into the appropriate carrier (tray or tape/reel). Most back-end processing is performed in wafer form.

Although not listed above, there are other inspection steps and procedures that ensure that only devices with acceptable quality are prepared for shipment.

FRONT-END PROCESS

The front-end process consists of the following steps:

- Application and patterning of dielectric material on wafer surface
- Deposition and patterning of redistribution metal trace layer above dielectric
- Application and patterning of additional dielectric material above redistribution
- Application and patterning of the under bump metallization (UBM)
- Application of solder

Figure 2 shows a representative cross section of a WLCSP device. The figure shows the additional dielectric layers, the redistribution layer (typically referred to as RDL), the UBM, and the solder bumps.

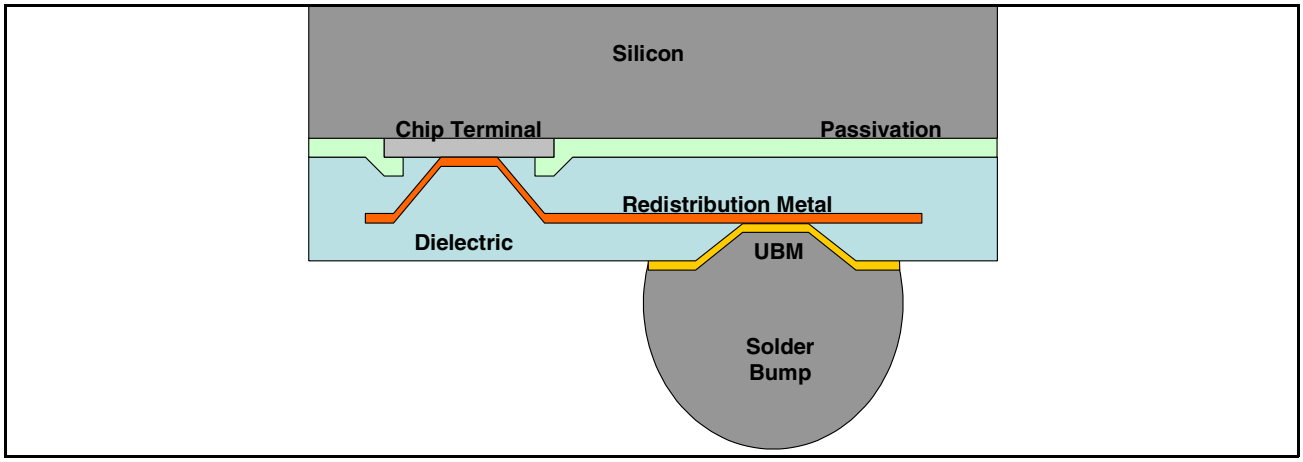

Figure 2: Schematic Cross Section of WLCSP Technology (not to scale)

TESTING

Following bumping, all devices on the wafer are fully tested with the appropriate function test parameters. The testing typically adds a small probe mark onto the bumps. The probe mark is cosmetic only, does not affect the overall bump shape, and does not affect the assembly of the WLCSP device.

BACK-END PROCESS

The back-end process involves the preparation of fully tested devices for customer shipment. The general flow for the back-end process is:

- Wafer backgrinding
- Backside laser marking of each device (still in wafer form)
- Singulation/Dicing
- Packing into appropriate shipping format (waffle pack or tape/reel)

INSPECTION PROCESSES

Throughout the manufacturing process, Broadcom employs numerous inspection steps designed to detect any defects on the device. These following steps are in addition to the standard process level inspection steps:

- 100% automated visual inspection after bumping
- 100% automated visual inspection during tape/reel (or waffle pack) process

These inspection steps are designed to detect any defects that could impact the quality of the WLCSP device including missing or damaged bumps, surface defects, chipped die, or incorrect or illegible marking, etc.

OUTGOING BUMP SPECIFICATIONS

WLCSP devices meet the bump specifications listed in Table 1.

Table 1: *Outgoing Bump Specifications*

Parameter	*Specification*
Bump height	100±15 µm
Bump coplanarity	Less than 30 µm
Bump shear	>24.7 g/bump

WLCSP Pb-Free Availability

All WLCSP devices are Pb-free.

WLCSP Form Factor

The WLCSP length and width dimensions are dependent on the specific device. Consult the product data sheet for these dimensions. Every WLCSP conforms to the height dimensions shown in Figure 3 and Table 2.

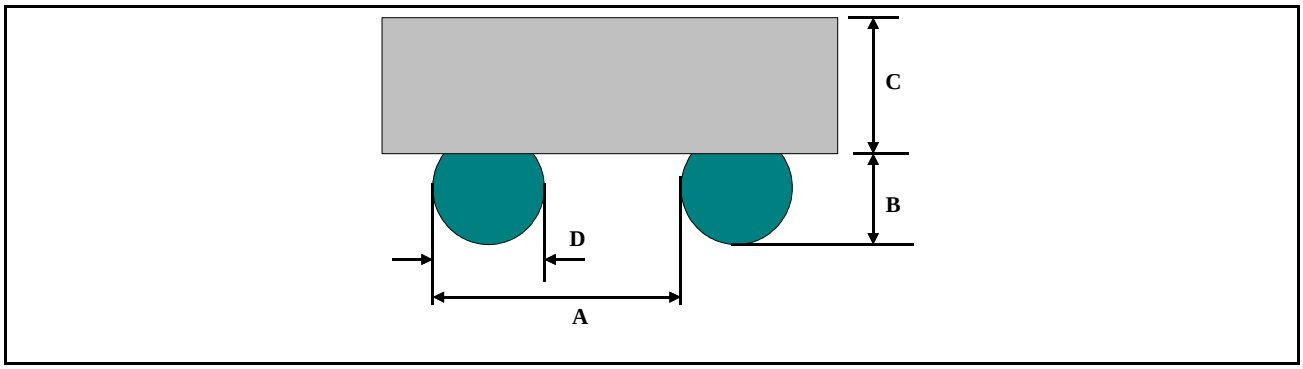

Figure 3: WLCSP Dimensions

Table 2: *WLCSP Dimensions*

Parameter	*Dimension Label*	*Specification*
Bump pitch	A	250 µm minimum *
Bump height	B	100±15 µm
Die thickness	C	300±25 µm
Bump diameter	D	140±15 µm
Total WLCSP height	B+C	400±40 µm
* The bump pitch on each device typically varies with a minimum pitch of 250 µm		

Please refer to the product data sheet for the specific product outline drawing.

WLCSP Layout Design Guidelines

WLCSP technology is compatible with conventional ceramic and laminate substrate design rules. The guidelines described in this section are recommended, but can be modified based on the user's expertise and experience.

Laminate Design Guidelines

Pad Geometry

The guidelines shown in Figure 4 and Table 3 are recommended for designs using laminate substrates (i.e., FR4, BT, etc.).

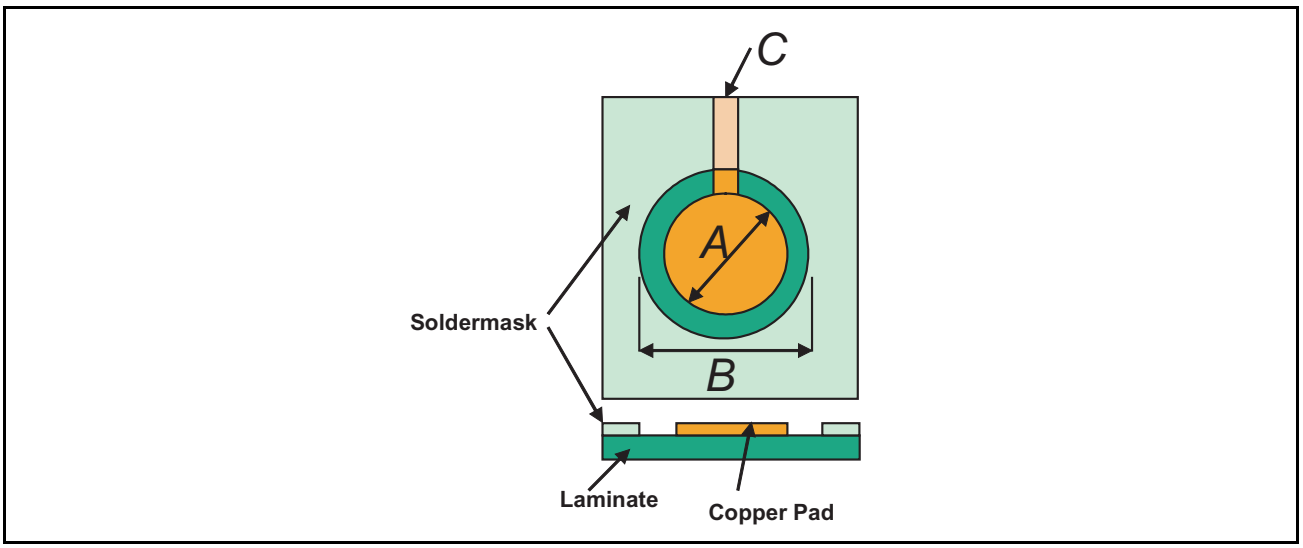

Figure 4: Recommended Laminate Pad Geometry (NSMD)

Table 3: *Recommended Laminate Pad Dimensions for NSMD Pad*

Parameter	*Dimension Label*	*Recommendation*
Pad diameter	A	90-100 µm
Soldermask opening	B	150-200 µm
Trace width	C	40-60 µm

Note: Non-soldermask defined pads (NSMD), as shown in Figure 4, are recommended.

- The soldermask opening dimension depends on the capability of the substrate manufacturer.
- The dimension should be specified so the soldermask will never overlap onto the pad.

Soldermask-defined (SMD) pads should be used only if the Solder-On-Pad (SOP) technology is applied to the substrate. In the SOP process, solder is pre-applied to the substrate by the substrate supplier. The solder is reflowed and then flattened or coined as shown in Figure 5.

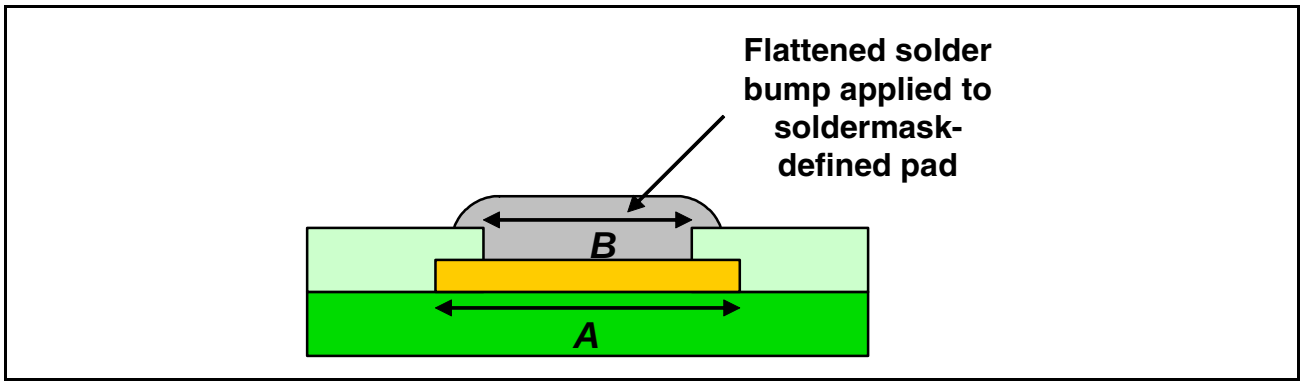

Figure 5: Laminate Pad Geometry for SMD Pad With SOP

The recommended dimensions for the SMD configuration are provided in Table 4.

Table 4: *Recommended Laminate Pad Dimensions for SMD Pad*

Parameter	*Dimension Label*	*Recommendation*
Pad diameter	A	150-200 µm
Soldermask opening	B	90-100 µm

Note: For SMD/SOP implementation:

- The pad diameter dimension depends on soldermask registration tolerance. The soldermask must completely cover the edge of the pad.
- SOP height should be at least as high as the soldermask.

Via Geometry

Via-in-pad technology is sometimes used to increase the routing density. Blind via-in-pad technology, typically created by either laser drilling or photolithography, is acceptable only if SMD/SOP is used (see “Pad Geometry” on page 5). A blind via-in-pad is shown in Figure 6. The typical via diameter is 50-100 mm. Note that the blind via-in-pad may increase the chance of voiding in the solder joint since the via hole can trap outgassing from the soldering flux.

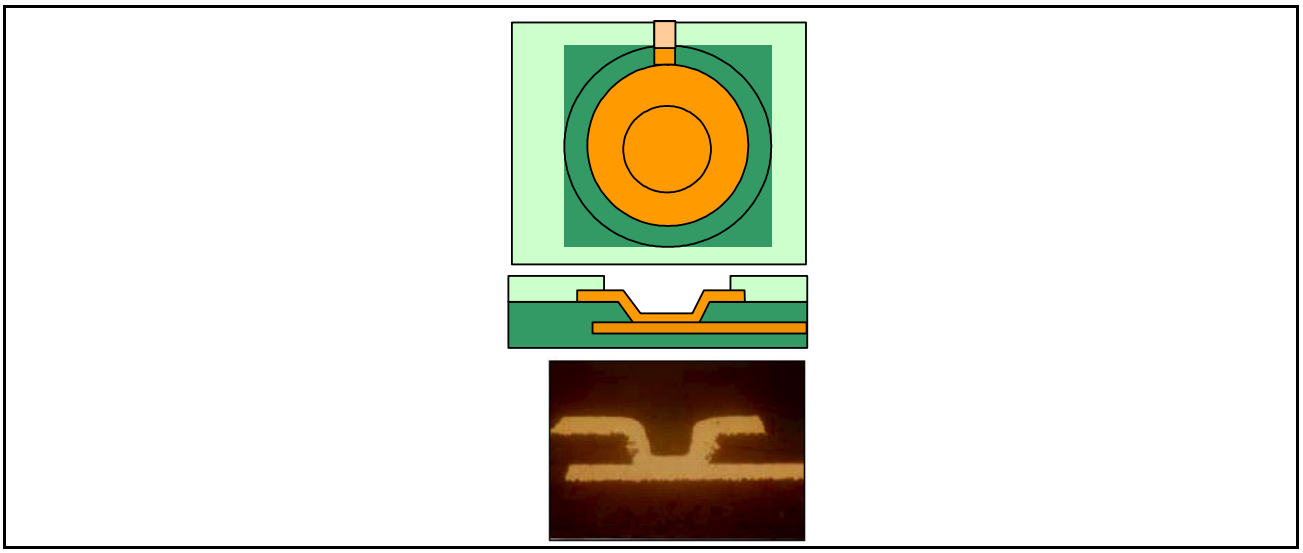

Figure 6: Blind Via-in-Pad (Acceptable)

Via-in-pad using a mechanically drilled via, shown in Figure 7, is not recommended.

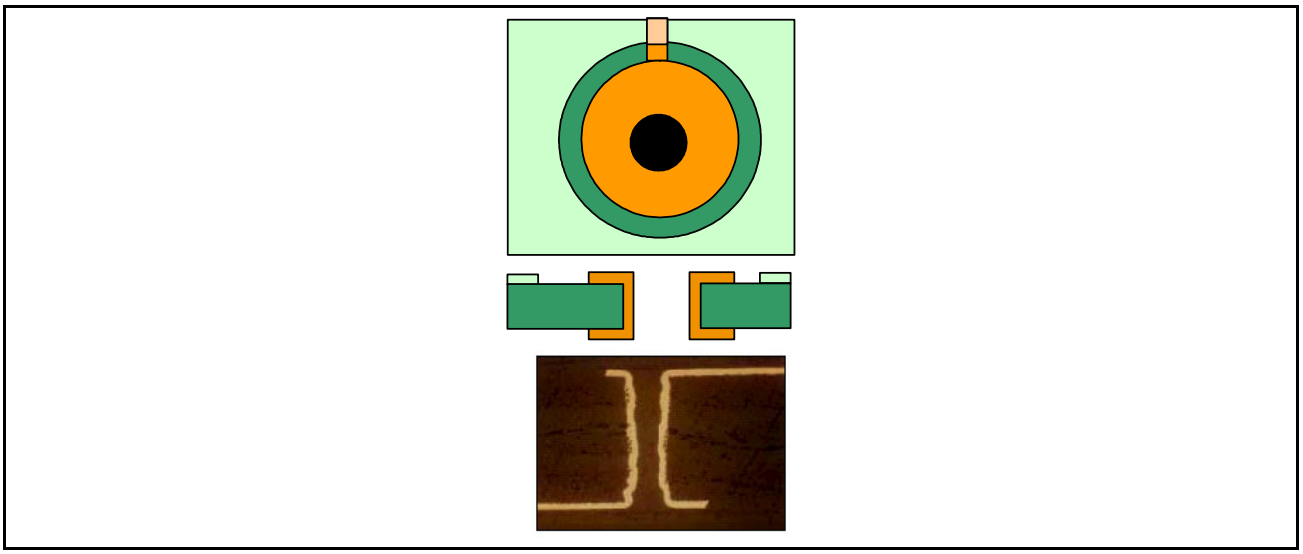

Figure 7: Mechanical Via-in-Pad (Not recommended)

Soldermask Design

Soldermask "webs" between pads are preferred (Figure 8) but are not required.

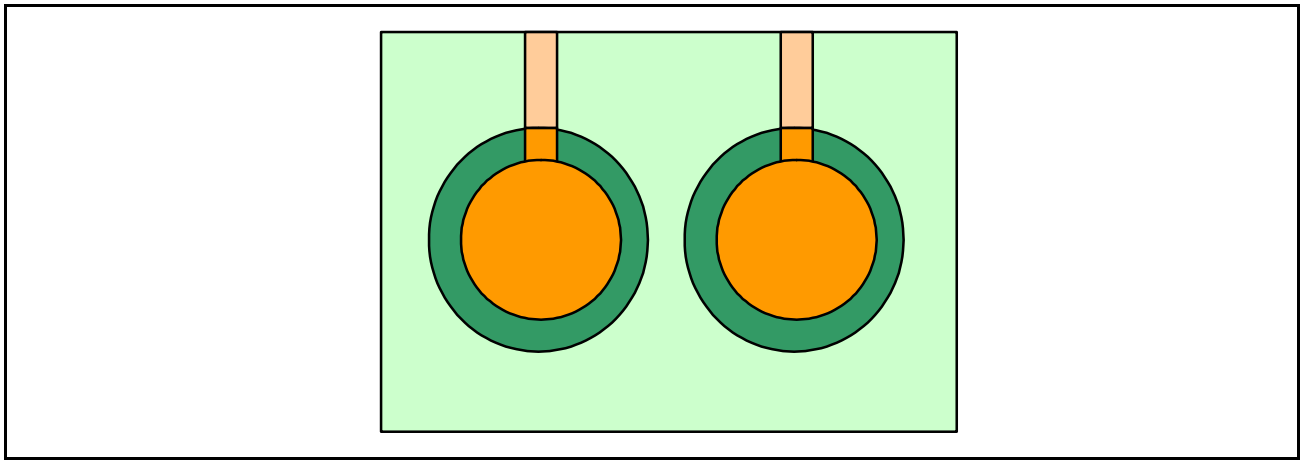

Figure 8: Soldermask Web Between Adjacent Pads

The use of a "scalloped" soldermask (Figure 9) is acceptable.

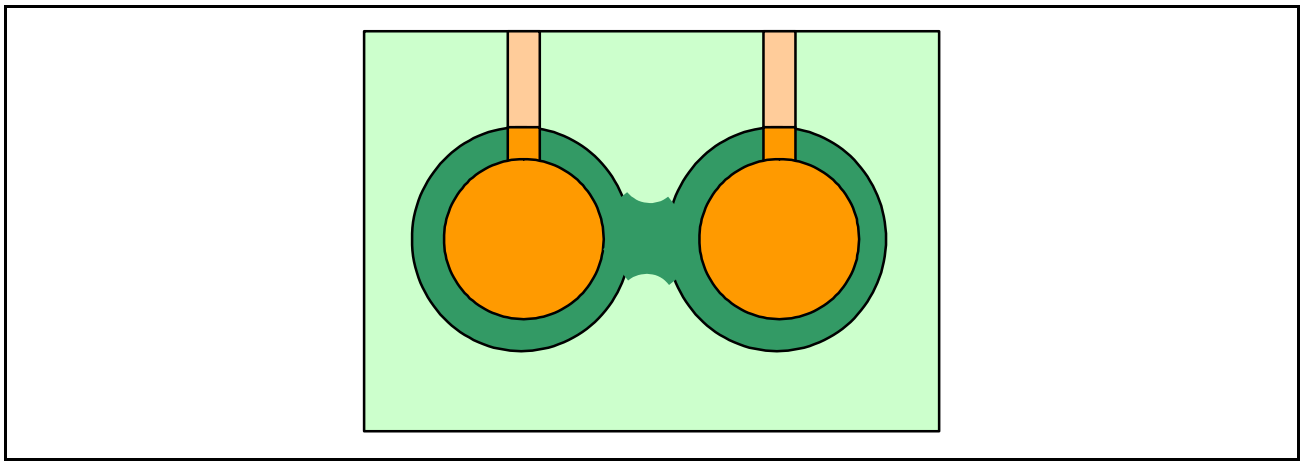

Figure 9: Scalloped Soldermask Between Adjacent Pads

Ground and Power Connections

There are typically multiple power and ground bumps on each device allowing the pads to connect to planes in the substrate. The pads must be carefully designed to avoid introducing manufacturing or reliability issues. The following guidelines are recommended:

1 It is recommended that the bump pads be connected to planes or vias using only a single trace (Figure 10). The pad size and trace width should follow the recommendations shown in Table 3 on page 5.

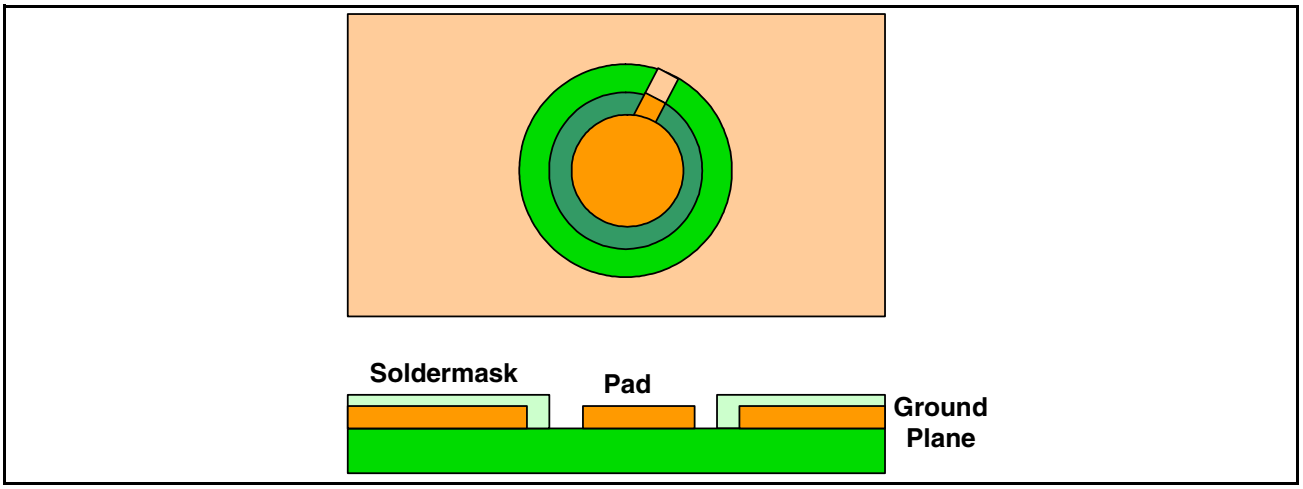

Figure 10: Recommended Pad/Trace Layout (NSMD pad shown)

2 Bump pads for ground pads should not be defined as a soldermask opening over a ground plane (Figure 11).

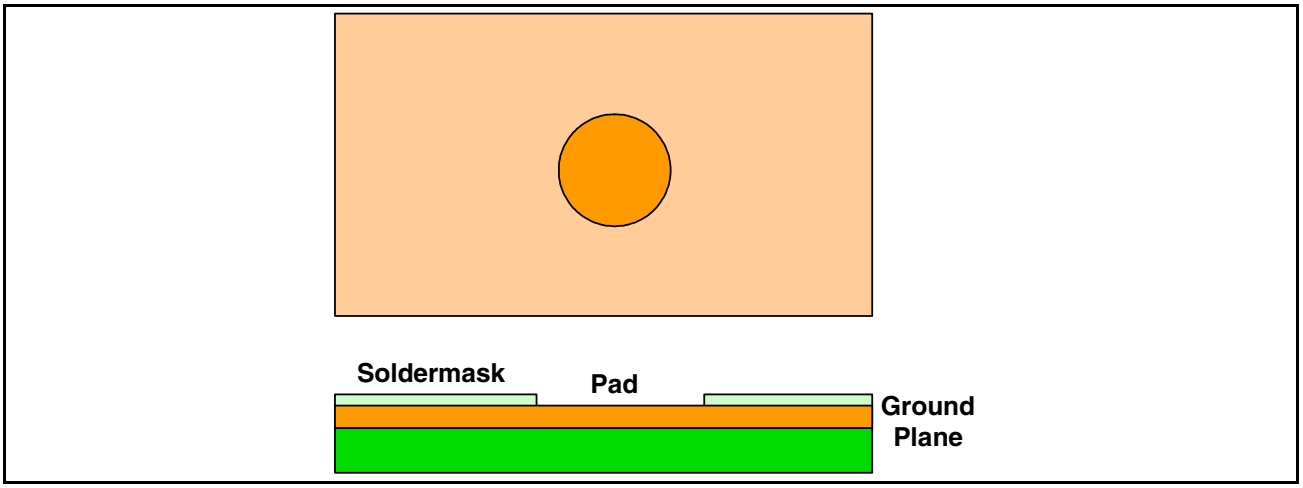

Figure 11: Soldermask Opening Over Ground Plane (Not recommended)

Note: For these recommendations, ground bumps are used to illustrate the guidelines. The same recommendations should also be applied to power nets.

3 Multiple trace connections between a ground bump pad and a plane are not recommended (Figure 12).

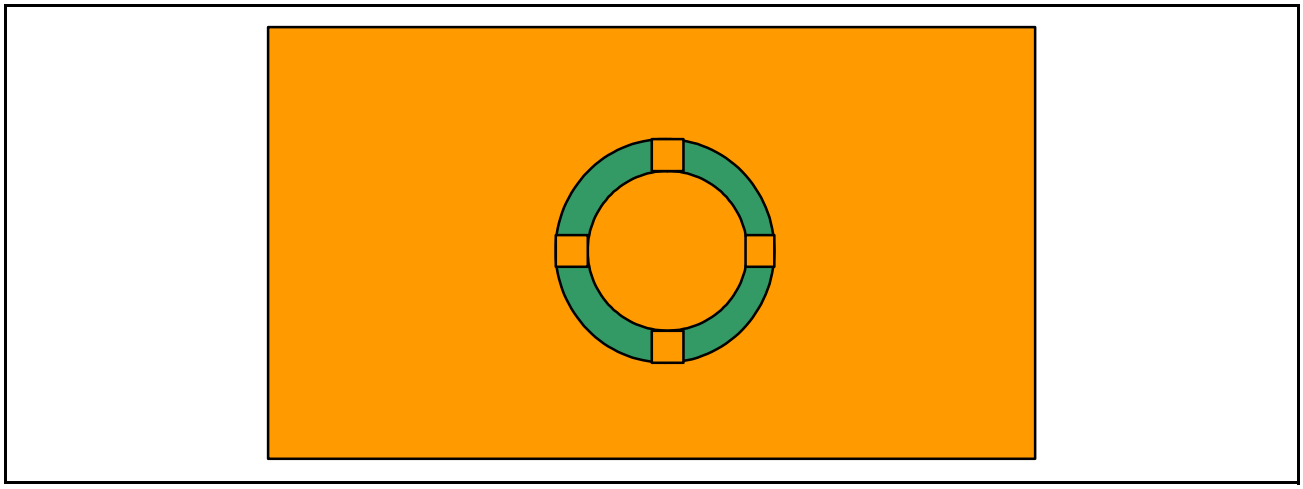

Figure 12: Multiple Traces Connecting Ground Pad to Plane (not recommended) [Soldermask not shown]

4 It is recommended that adjacent same net ground pads be connected to the ground plane separately and not connected together (Figure 13).

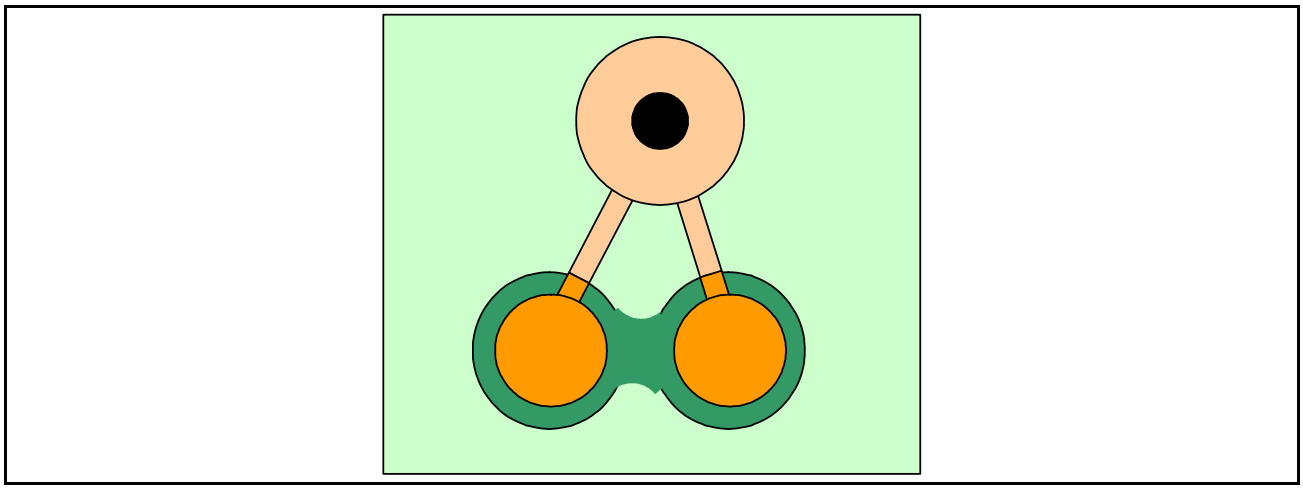

Figure 13: Recommended Connection of Ground Pads to Via (or plane)

CERAMIC DESIGN GUIDELINES

Pad Geometry

The guidelines shown in Figure 14 and Table 5 are recommended for designs using ceramic substrates (i.e., Alumina, LTCC, etc.).

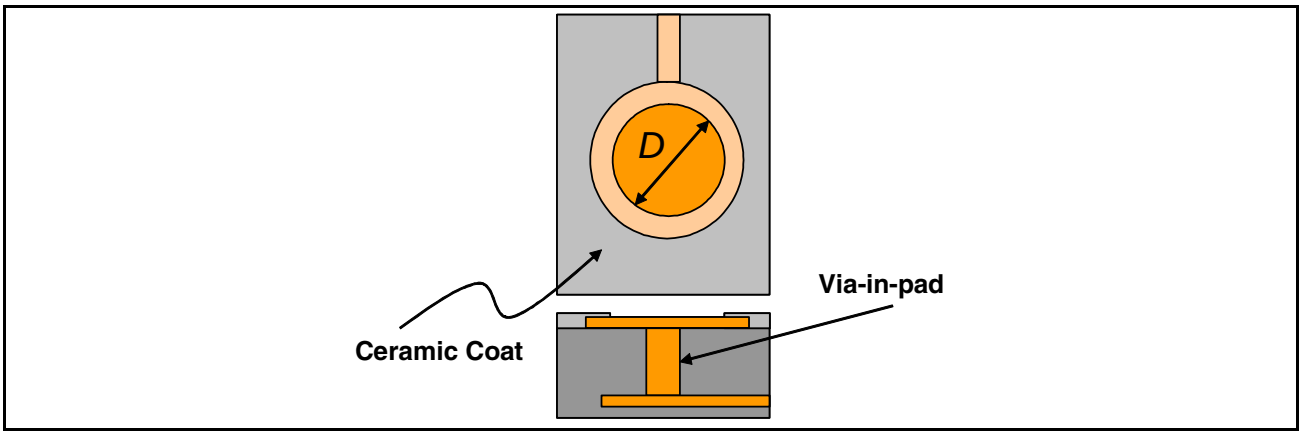

Figure 14: Recommended Ceramic Pad Geometry

Table 5: *Recommended Pad Dimensions for Ceramic Substrate*

Parameter	*Dimension Label*	*Recommendation*
Exposed pad diameter	D	90-100 µm

WLCSP SUBSTRATE PAD SURFACE FINISH RECOMMENDATIONS

The guidelines in this section pertain to the surface finish on the pads on the WLCSP side of the substrate.

LAMINATE SUBSTRATES WITH NSMD PADS

See “Pad Geometry” on page 11 for NSMD design guidelines.

Recommended

- Organic Solderability Preservative (OSP)

Alternatives to OSP

The following are potential alternatives to OSP based on the user's experience:

- Electroless Ni/Immersion Au (ENIG)
  - ENIG is susceptible to quality issues associated with brittle intermetallic formation (unrelated to WLCSP). Users are advised to confirm the quality of their supplier's ENIG finish.
  - Au thickness must be less than 0.1µm to avoid decreasing the solder joint strength.
- Immersion Ag
  - Requires anti-tarnish layer to prevent corrosion and silver migration

Not Recommended

- Hot Air Solder Leveling (HASL)
  - Surface flatness and consistency is not sufficient
- Electrolytic Ni/Au
  - Au thickness (0.4-0.7µm) is too high

LAMINATE SUBSTRATES WITH SMD PADS AND SOP

See “Pad Geometry” on page 11 for SMD/SOP design guidelines.

Recommended

- Organic Solderability Preservative (OSP) covered with SOP
- Bare copper on flipchip pads covered with SOP

Alternatives to OSP

The following are potential alternatives to OSP based on the user's experience:

- Electroless Ni/Immersion Au (ENIG) covered with SOP
  - ENIG is susceptible to quality issues associated with brittle intermetallic formation (unrelated to WLCSP). Users are advised to confirm the quality of their supplier's ENIG finish.
  - Au thickness must be less than 0.1µm to avoid decreasing the solder joint strength.
- Immersion Ag covered with SOP
  - Requires anti-tarnish layer to prevent corrosion and silver migration

Not Recommended

- Hot Air Solder Leveling (HASL)
  - Surface flatness and consistency is not sufficient
- Electrolytic Ni/Au
  - Au thickness (0.4-0.7µm) is too high

CERAMIC SUBSTRATES

Recommended

- Electroless Ni/Au
  - Electroless Ni/Au plating on ceramic substrates is not susceptible to the issues described above for ENIG on laminate substrates.

WLCSP SUBSTRATE QUALITY GUIDELINES

The substrate quality is critical to maintain high yield and reliability for WLCSP applications. The following critical items should be monitored by the user and/or the substrate supplier:

- Substrate planarity
  - WCCSP assembly will be sensitive to the planarity of the substrate in the WLCSP mounting area. The planarity should be specified as less than 30um in the WLCSP mounting area.
- Substrate pad size
  - To maintain high yield and reliability for the finished WLCSP solder joint, the pad size should be monitored by the user and/or the substrate supplier. The monitor should confirm that the pad size is within the specified limits agreed upon by the user and the substrate supplier. The acceptable variation in the pad size is +/- 15um.
- Soldermask opening
  - The soldermask opening size should be monitored. The acceptable variation in the soldermask opening is +/-25um. As stated above, the soldermask should not overlap the edge of the pad.
- Substrate surface finish quality
  - The thickness of the substrate surface finish should be monitored by the substrate supplier
  - For Ni/Au finishes, the Au thickness should be less than 0.1um.
  - The surface finished uniformity should be confirmed. The surface finish should be limited to the features and should not be overplated onto the substrate surface.

WLCSP ASSEMBLY PROCESS GUIDELINES

The WLCSP technology is designed to be compatible with existing flipchip/surface mount assembly processes.

HANDLING

As with any component, avoid exposure to electrostatic discharges, thermal/mechanical damage, and harsh environments.

MOISTURE SENSITIVITY

The WLCSP is rated at JEDEC level 1 moisture sensitivity (J-STD-20B). It is not moisture sensitive and is rated to fit into typical Pb-free reflow profiles with a maximum component temperature of 260°C.

WLCSP ASSEMBLY PROCESS

The recommended assembly process flow for WLCSP devices is:

- Apply flux
- Place component
- Reflow component
- Clean (optional)
- Underfill and cure

Fluxing

Flux Material Selection

The selection of the flux material depends on many factors including compatibility with the Pb-free bump material, compatibility with the user's assembly process, and compatibility with the underfill material. Different fluxes will leave different amounts of residues, which can affect underfill adhesion and reliability. Because it is difficult to remove the residues after the flipchip attach process, the so-called "No-clean" fluxes are recommended and aqueous-clean fluxes are not recommended.

The evaluation of a flux should include the consideration of the following factors:

- Bump Wetting
  - Cross sections are recommended to confirm that the solder bumps are fully wetting to the substrate pads and the solder joints are well-formed with a smooth surface and symmetric shape (Figure 15).

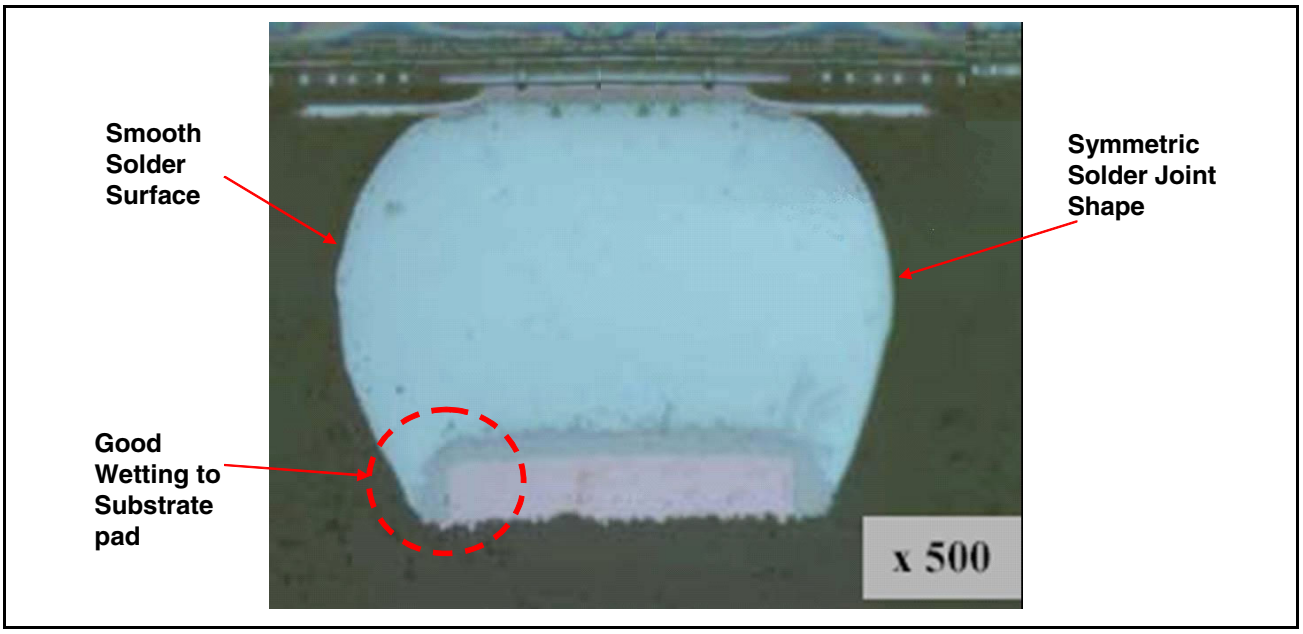

Figure 15: Cross Section of WLCSP Solder Joint Showing Good Joint Shape and Pad Wetting

- Underfill voiding
  - Flux residues can cause increased underfill voiding. This also greatly depends on the underfill material. C-mode Scanning Acoustic Microscopy (CSAM) inspection should be used to determine the voiding level.
- Underfill compatibility
  - Flux residues can cause decreased adhesion between the underfill and the chip surface which can lead to reliability issues. Reliability testing and CSAM inspection should be used to determine successful underfill adhesion.

See “Material Evaluation” on page 20 for a list of flux materials that Broadcom has successfully evaluated.

Flux Application Process

Fluxing guidelines for WLCSP are similar to the standard flipchip fluxing process. Typically, flux is applied to WLCSP bumps by using drum fluxer with a doctor blade (Figure 16) or by a flux plate (Figure 17). Both methods are acceptable.

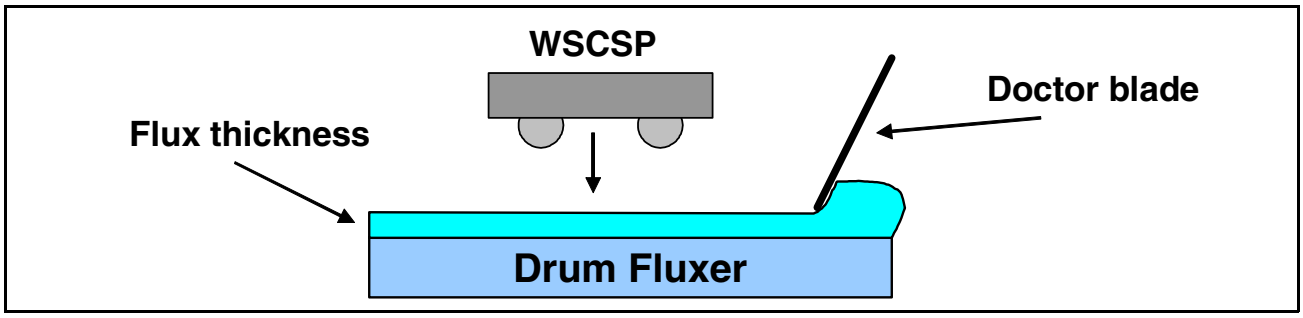

Figure 16: Drum Fluxer With Doctor Blade

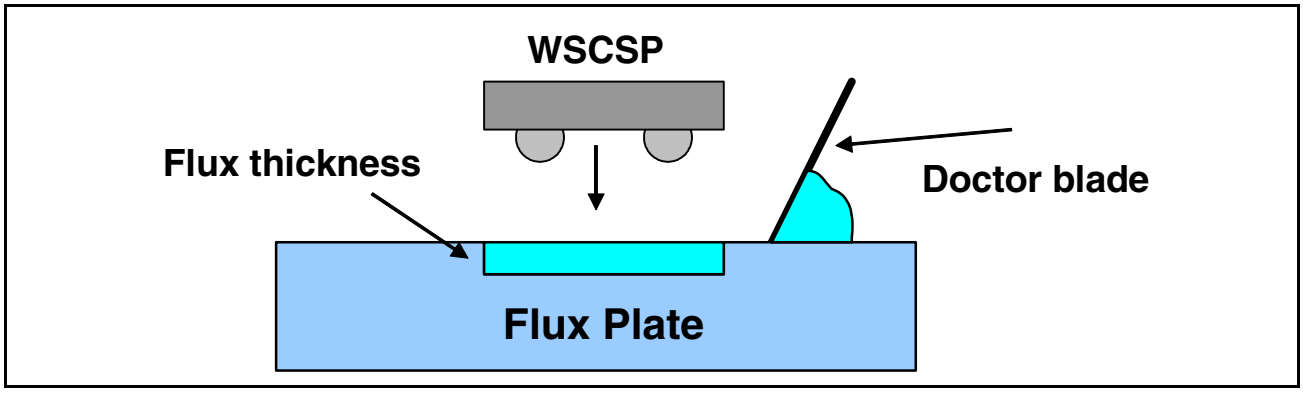

Figure 17: Flux Plate

For a drum fluxer, the flux thickness is set by the defined distance between the doctor blade and the rotating drum surface. For a flux plate, the flux thickness is set by the depth of a pocket in the plate, which is filled with flux by a doctor blade.

Typically, the fluxing process is part of the component placement equipment. The WLCSP component is picked up from the tray (or picked out of the tape/reel). The component is optically inspected to determine the orientation and then dipped into the flux. The component is then placed on the substrate (see “Component Placement” on page 17).

The recommended thickness of the applied flux is 1/3 to 1/2 of the bump height (30-50 mm for 100 µmWLCSP bump). With this process, only the tips of the bumps are coated with flux. It is critical that flux thickness be closely monitored on a lot basis to confirm consistent flux application. Allowing flux deposition on the die surface should be avoided. Excessive flux can promote shorting during reflow and cause problems for underfill adhesion.

Component Placement

The following guidelines are recommended:

- Automated high accuracy placement equipment should be used
- Maximum offset of component should be less than 50 mm (25 mm preferred)
- Placement force should be minimized to avoid component damage

Reflow

The reflow profile is dependent on many factors including flux selection, solder composition, assembly thermal mass, and the user's reflow equipment. Broadcom does not recommend a specific reflow profile but provides the following general guidelines:

- Guidelines for ramp rates and soak times provided by the flux supplier should be adhered to since it is critical that the flux behaves properly. The flux composition and requirements will set the shape of the reflow profile, including ramp rates and pre-soak requirements to achieve proper flux activation/evaporation and adequate wetting.
- The solder composition typically sets the peak temperatures of the profile. The melting point of the WLCSP Pb-free solder is between 217°C-224°C.
- It is recommended that the peak temperature at the solder joint be a minimum of 245°C.
- It is recommended that time above 220°C for the solder joints be between 60-90s with a minimum of 60s. The time above 220°C should not exceed 150s.
- The maximum component temperature should not exceed 260°C
- Excessive ramp rates (>3°C/s) should be avoided
- It is recommended that the substrates be baked prior to reflow to remove any moisture in the substrate

To develop the reflow profile, it is recommended that the user place thermocouples at various locations on the assembly to confirm that all locations meet the profile requirements. The critical locations are the solder joints on the outer edge and in the center of the WLCSP and the WLCSP case.

The oven profile parameters should account for the thermal mass of the component. Larger thermal mass components will need a hotter profile to meet the component temperature requirements. When developing the reflow profile, it is recommended that the actual fully loaded assembly be used to make sure that the total thermal mass is accounted for.

Following reflow, the following tests should be performed to confirm the results:

- The assembly should be X-rayed to confirm that there are no shorts or irregular solder joints. X-ray inspection will also indicate if the void level is acceptably low.
- It is recommended that several WLCSP components be mechanically removed from the substrate (prior to underfill). This evaluation can be used to determine if there is sufficient wetting between the bump and the substrate pad. There can be multiple breakage modes during this test including bulk solder breaking, UBM/die cracking, and pad pullout from the substrate. After reflow, physically pry the WLCSP off of the module/PCB to verify that 100% of the bumps have formed good solder joints with the module. The breakage mode is not critical, but should be used to confirm that there are no apparent non-wetting bumps. Non-wetting bumps will typically have an undisturbed appearance. Properly wetted bumps will fail either within the solder, or by pulling the pad out of the substrate module or out of the WLCSP.
- Cross sections are recommended to confirm the joint shape, wetting, and solder joint voiding.

The standoff height between the die surface and the top of the substrate soldermask should be between 50-65 mm as shown in Figure 18.

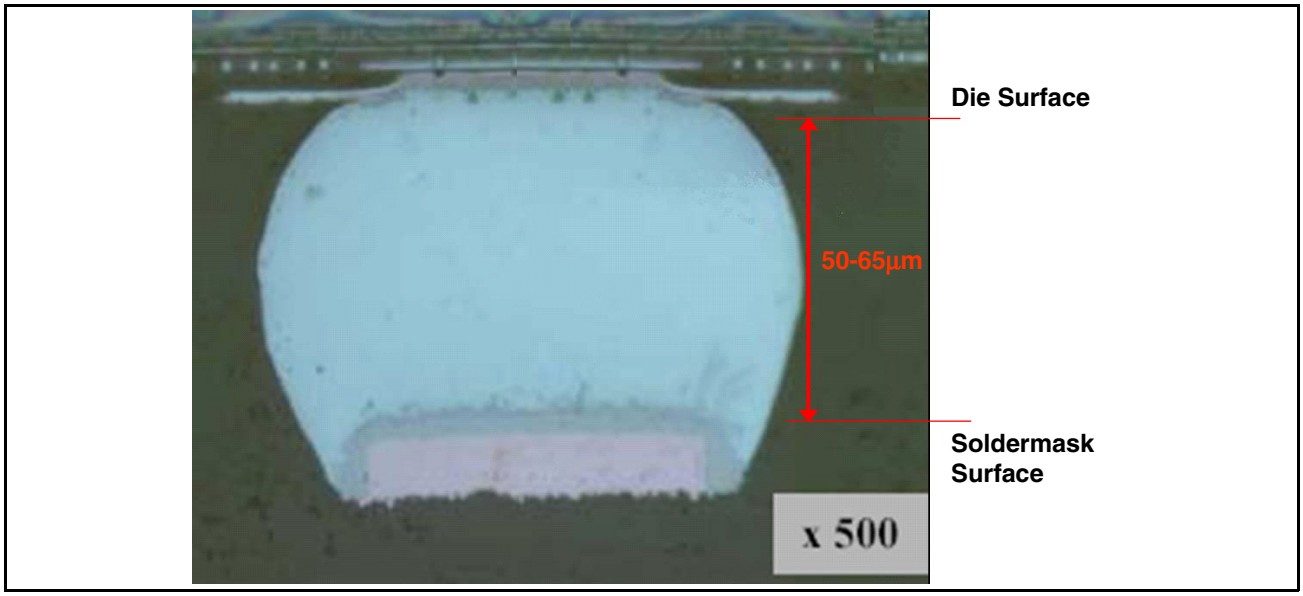

Figure 18: Typical WLCSP Solder Joint Cross Section Showing Standoff Height

Cleaning

Cleaning is typically challenging with flipchip and WLCSP components due to the small gap between the die and the substrate. For this reason, no-clean fluxes are recommended and cleaning is not required.

Underfill and Cure

Underfill Application Process

The underfill is intended to completely encapsulate the gap between the chip and the substrate. The primary purpose of the underfill is to reduce the stress on the flipchip solder joints. A poor underfill process can lead to poor assembly yield and poor reliability. The requirements of the underfill process are:

- Complete encapsulation of the chip-to-substrate gap with no voiding (or voiding within specified criteria)
- Proper fillet formation around the edge of the die
- Provide sufficient adhesion to protect against delamination during operation and environmental conditions.

The general underfill process is:

- Bake assembly to remove moisture
- Apply plasma cleaning to improve underfill wettability and remove any flux residues (optional)
- Place assembly on a heater block and set to appropriate temperature
- Dispense predetermined volume of underfill in a predetermined dispense pattern
- Wait a specific time for the underfill to fully flow under the WLCSP
- Apply a seal around all four sides of the WLCSP to create the appropriate fillet
- Cure underfill

The creation of a void-free underfill process depends on many factors including underfill material, underfill equipment, underfill dispense pattern, and underfill processing conditions. Broadcom does not provide specific recommendations for an underfill process, but provides the following general guidelines:

- Plasma cleaning prior to underfill is not required. Depending on the flux and underfill material selection, plasma cleaning can provide some enhancements to underfill adhesion.
- The temperature of the underfill processing is critical to achieve the correct viscosity for optimum underfill workability and void reduction. It is recommended to follow to underfill supplier's recommendation for processing temperature but this is a parameter that can be varied to minimize the voiding.
- Single-side dispense or L-shaped dispense patterns are both acceptable. In general, a single-side dispense pattern (where the underfill is dispensed only along a single edge of the WLCSP) is sufficient for WLCSP and will result in lower voiding.
- The amount of underfill to be dispensed should be experimentally determined. The underfill volume should be sufficient to completely encapsulate the WLCSP-to-substrate gap. Once the underfill volume is determined, it is recommended that the underfill volume be monitored as a process control parameter.
- Following the initial underfill dispense, the amount of time it takes to completely encapsulate the WLCSP-to-substrate should be experimentally determined. Once this time has elapsed, a single pass dispense may need to be made along the remaining three sides of the WLCSP to create the proper fillet.
- The fillet height should extend at least one-half the die thickness (Figure 19).

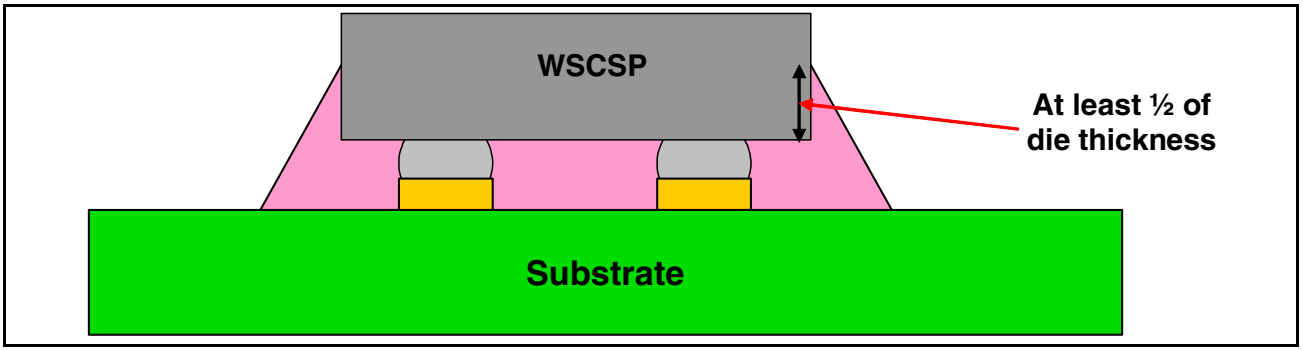

Figure 19: Recommended Underfill Fillet Height

- The underfill cure profile should follow the recommendation of the underfill supplier.
- During process development, it is recommended to use CSAM to inspect for any underfill voiding. The void criterion is dependent on the user's requirement, but it is recommended that the total voids be <1% by area with no void larger than 100 µm. It is also recommended to use CSAM inspection as a process monitor. This can typically be performed on setup units on a per lot basis.
- It is recommended that the temperatures associated with the underfill process (heater block, cure profile) be included as part of the in-line process monitor data collection.

Underfill Material Selection

The selection of the underfill material depends on the workability, as discussed in “Underfill Application Process” on page 18, as well as reliability requirements. The underfill should be compatible with both the WLCSP as well as the substrate material. It should be able to withstand subsequent processing steps (after underfill cure) and provide sufficient reliability. The following factors should be considered when selecting the underfill:

- Workability, as discussed in “Underfill Application Process” on page 18.
- Adhesion through the assembly process
  - CSAM should be used to assess underfill adhesion
- Adhesion through reliability process
  - Typically, the failure mode for flipchip components in reliability testing is underfill delamination. Once the underfill delaminates, it ceases to provide strain relief to the solder bumps, which can lead to bump cracking.
  - CSAM should be used to assess underfill adhesion during and after reliability testing.
- Material properties
  - In some cases, the material properties that result in excellent workability may result in lower than acceptable reliability. An excessively soft material (as determined by the glass transition temperature and the elastic modulus) can do an inadequate job of providing strain relief. Typically, a glass transition temperature <100°C is considered to be "soft" and may present some reliability issues.

See “Material Evaluation” on page 20 for a list of underfill materials that Broadcom has successfully evaluated.

WLCSP Rework

Rework of WLCSP components is not recommended for production material. Rework for prototype or engineering material is possible.

MATERIAL EVALUATION

As part of the WLCSP technology development, Broadcom has evaluated and qualified different flux and underfill combinations. These materials are listed in Table 6 for reference only. The listing of the materials in this document does not imply a recommendation or endorsement of these materials. Since every assembly system is different, successful results in one system may not produce successful results in a different system. The user must fully evaluate the materials used during WLCSP assembly to confirm that they meet the user's quality and reliability requirements.

Table 6: *Underfill/Flux Combinations*

Underfill	*Flux*
Ablestik UF8806H	Alphametals OL-107 Indium Tac-10 Kester TSF-6502 Heraeus TF-38
Sumitomo 4152R	Alphametals OL-107 Kester TSF-6502
Dexter FP4549	Kester TSF-6502

Module Assembly Considerations

A common implementation is to integrate WLCSP components into a module with other passive and active components. The WLCSP component is compatible with typical module assembly processes, but there are some factors that should be considered to ensure sufficient yield and reliability.

- Multiple reflow
  - The WLCSP component can be subjected to up to four reflow cycles.
  - It is recommended that the assembly process be optimized to reduce the number of reflows. For example, it is recommended that all solderable components (WLCSP, passive components, etc.) be reflowed simultaneously instead of sequentially.
- Material Compatibility
  - It should be verified that there are no issues with the underfill material compatibility with module assembly processes after the WLCSP mounting process. This includes additional reflows, overmolding, lid attach, etc. As with the original underfill process, it should be verified that the additional module assembly processes do not cause any delamination in the underfill, and that the underfill in the finished module can meet the module reliability requirements.
- Overmold process
  - The WLCSP component can be overmolded using processes that are consistent with typical overmold processes used in other plastic packages (i.e., Plastic Ball Grid Arrays, etc.). In evaluating the overmold process, it is recommended to consider the following factors:
    - Warpage should be minimized to reduce stresses on the module and module components. Warpage can be controlled by using proper fixturing and process conditions during the overmold process.
    - Process evaluation and reliability testing should confirm no overmold delamination.
    - Bubbles in the overmold should be avoided.
    - Mold bulging should be avoided.
    - The modules should be inspected to confirm that soldermask cracks are not induced at the mold cap edge during the molding process.
    - Standard package qualification testing should be applied to the finished module including shock and bend tests.

WLCSP RELIABILITY

The WLCSP technology has been fully qualified according to Broadcom's reliability standards. The testing shown in Table 7 has been performed as part of the WLCSP technology qualification.

Table 7: *WLCSP Qualification Testing*

Qualification	*Test Condition*
Wafer Level Qualification	Temperature cycling: -55 to 125°C, 500x Unbiased Pressure Cooker: 121°C, 2 atm, 100% RH, 168hrs High temperature storage: 150°C, 500hrs Bump shear after 5x, 10x reflow (260°C) Bump shear after 500, 1000h at 150°C Passivation integrity testing Construction analysis Physical dimensions
Package Level Qualification*	Preconditioning: JEDEC Level 3 with 3x 260°C reflow Temperature cycling: -55 to 125°C, 1000x Thermal shock: -55 to 125°C, 1000x Unbiased Pressure Cooker: 121°C, 2 atm, 100% RH, 168hrs High temperature storage: 150°C, 500hrs Die Shear Construction analysis Physical dimensions
*For the package level qualification, the WLCSP is assembled into a flipchip-land grid array package and subjected to the reliability testing	

WLCSP DELIVERY

The WLCSP parts are typically delivered in tape and reel packing. Consult the respective product data sheet for the tape and reel parameters.

Prototype quantities are available in waffle pack trays. Consult Broadcom Sales/Marketing for details.

Broadcom Corporation

16215 Alton Parkway
P.O. Box 57013
Irvine, CA 92619-7013
Phone: 949-450-8700
Fax: 949-450-8710