Soldering Guidelines for Exposed Pad Die-Up Leadframe Packages
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Change Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PACKAGING-AN200-R</td>
<td>7/28/03</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>

Broadcom Corporation  
P.O. Box 57013  
16215 Alton Parkway  
Irvine, CA 92619-7013  
© 2003 by Broadcom Corporation  
All rights reserved  
Printed in the U.S.A.

Broadcom® and the pulse logo are registered trademarks of Broadcom Corporation and/or its subsidiaries in the United States and certain other countries. All other trademarks mentioned are the property of their respective owners.
TABLE OF CONTENTS

Purpose ......................................................................................................................................................... 1
Scope ............................................................................................................................................................ 2
Reference Standards and Broadcom Documents............................................................................................. 3
Exposed Pad Leadframe Packages for Thermal Enhancement........................................................................ 4
   Heat Dissipation Paths and Package Thermal Resistances ...................................................................... 4
   Exposed Pad Leadframe Packages ....................................................................................................... 7
PCB Layout Recommendations .................................................................................................................. 8
   Terminal Solder Joint Analysis and Requirement for Leaded Exposed Pad Package: eTQFP ............... 9
   Terminal Solder Joint Analysis and Requirement for Leadless Exposed Pad Package: MLP ............. 10
   PCB Thermal Land Design Guidelines .................................................................................................. 12
      Design Guidelines of PCB Pads for Package Terminals ................................................................... 19
Stencil Design Recommendations ................................................................................................................. 22
Reflow Soldering Recommendations .......................................................................................................... 24
Rework Recommendations for Exposed Pad Leadframe Packages ............................................................. 25
LIST OF FIGURES

Figure 1: Junction-to-ambient Power Dissipation of a QFP Package .................................................................5
Figure 2: Package Heat Dissipation Primary Paths and Resistances............................................................... ..5
Figure 3: Package Equivalent Thermal Resistance Network of Primary Heat Dissipation Paths .......................6
Figure 4: Junction-to-ambient Power Dissipation of an eTQFP Package...........................................................7
Figure 5: Bottom View of Die-up Leadframe Package with Exposed Die Attachment Pad:
   (a) eTQFP, (b) MLP ........................................................................................................................................8
Figure 6: Solder Joint Fillet Requirement for Leaded Exposed Pad Packages [from Ref. 8, Section 11.2].......9
Figure 7: Solder Wetting on Terminal Side Surfaces (Including the Exposed Side Surface) is not Required for
   Leadless Exposed Pad Packages ................................................................................................................10
Figure 8: Solder Joint Length, Width, Thickness, and Overhangs for No-lead Exposed Pad Packages
   [Ref.6, Figure 9-4]........................................................................................................................................11
Figure 9: Junction-to-ambient Power Dissipation of an eTQFP Package ..........................................................12
Figure 10: Size of PCB Thermal Land Plane for eTQFP Package .....................................................................13
Figure 11: Size of PCB Thermal Land Plane for MLP Package .....................................................................13
Figure 12: Thermal Land Design Rule for Package with Exposed Pad Size Larger than 3mm x 3mm............15
Figure 13: Thermal Land Design Rule for Package with Exposed Pad Size 3mm x 3mm or Smaller..........16
Figure 14: SMD Design Rule on Thermal Land – Cross Section View ..............................................................16
Figure 15: Thermal via Design for Package with Exposed Pad Size Larger than 3mm x 3mm.......................17
Figure 16: Thermal via Design for Package with Exposed Pad Size 3mm x 3mm or Smaller....................18
Figure 17: Recommended via Design Rule for Via-to-plane and Via-to-thermal Land Connections ..........18
Figure 18: Thermal Relief Should Not be Used for Via-to-plane and Via-to-thermal Land Connections ....19
Figure 19: PCB Pad Dimension for Package Terminal .....................................................................................20
Figure 20: Solder Mask Opening Around PCB Pad for Package with Terminal Pitch 0.50mm or Larger ......21
Figure 21: Solder Mask Opening Around PCB Pad for Package with Terminal Pitch 0.40mm .................21
Figure 22: PCB Terminal Pad Stencil Design for: (a) Pad Pitch ≥ 0.50mm, (b) Pad Pitch = 0.40mm ............22
Figure 23: Thermal Land Stencil Design for Package with Exposed Pad Size Larger than 3mm x 3mm.........23
Figure 24: Stencil Design on Thermal Land for Package with Exposed Pad Size 3mm x 3mm or Smaller....23
Figure 25: Reference Reflow Profile [4] ............................................................................................................24
LIST OF TABLES

Table 1: Exposed Pad Leadframe Packages and Package Bottom Views ........................................................ 2
Table 2: Dimensional Criteria for No-Lead Exposed Pad Packages [Ref. 6, Table 9-4] ............................... 11
Table 3: Reference Reflow Profile Parameters ................................................................................................ 24
PURPOSE

This application note outlines the layout steps needed to ensure adequate soldering of the exposed pad lead frame packages on printed circuit board (PCB) for proper thermal and electrical connections.
**Scope**

This application note provides land pattern design general guidelines and surface mount recommendations for Broadcom devices using exposed pad leadframe packages listed in Table 1.

<table>
<thead>
<tr>
<th>Package</th>
<th>Package Description</th>
<th>Bottom View of Package</th>
<th>Cross Section Schematic View of Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>eTQFP [1]</td>
<td>Exposed Pad Thin Quad Flat Pack</td>
<td></td>
<td></td>
</tr>
<tr>
<td>eLQFP [1]</td>
<td>Exposed Pad Low Profile Quad Flat Pack</td>
<td></td>
<td></td>
</tr>
<tr>
<td>eSOIC</td>
<td>Exposed Pad Small Outline Package</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(Also known as QFN, MLF, LPCC)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Saw Singulation

Punch Singulation
REFERENCE STANDARDS AND BROADCOM DOCUMENTS

1. JEDEC Solid State Product Outline, MS-026, Low/Thin Profile Plastic Quad Flat Package, 2.00mm Footprint, Optional Heat Slug, January 2001.


7. JEDEC JC11 Item # 11.2-643(S), Proposed Design Guide for QFP-N/SO-N Package Families, JEDEC Publication 95, Design Guide 4.8, Plastic Quad and Dual Inline Square and Rectangular No-Lead Packages (with Optional Thermal Enhancements), November 2002


EXPOSED PAD LEADFRAME PACKAGES FOR THERMAL ENHANCEMENT

The following is a brief discussion on device thermal performance enhancement through the use of die-up packages with exposed die attach paddle. Pictorial illustrations in this section use only leaded packages since the thermal analysis applies to both leaded and no-lead (leadless) exposed pad packages.

HEAT DISSIPATION PATHS AND PACKAGE THERMAL RESISTANCES

Heat is generated due to Joule heating when there is electrical current flow through the integrated circuit (IC) on the active surface of semiconductor die. The amount of heat generation, $P$, is also known as IC power dissipation and has the unit of Watt (W). The heat generation causes an increase of temperature at the junctions of diodes and transistors as well as along the metal traces of the IC on the die active surface. The long-term reliability of IC devices is affected by the diffusion process of electromigration that causes drift of metal atoms in the direction of the electron flow. This diffusion process accelerates with the increase of device temperature.

Device power dissipation, package internal thermal resistances, board stack-up, board layout, package-to-board interconnection, and system thermal management design together control the device junction temperature rise. In application system environment, the device junction temperature, $T_J$, is correlated with power dissipation, $P$, and ambient temperature, $T_A$, through junction-to-ambient thermal resistance, $\theta_{JA}$.

$$T_J = T_A + P \cdot \theta_{JA}$$  \[1\]

Device junction temperature increases linearly with the increase of the device junction-to-ambient thermal resistance. The following provides a brief discussion on methods of reducing device junction-to-ambient thermal resistance through the application of exposed pad leadframe packages together with board layout optimization.

As shown in Figure 1, the primary paths of heat dissipation from the die of a leadframe package, such as a QFP package, to the ambient is

1. Package to board to ambient air, and
2. Package to case top to ambient air.
Figure 1: Junction-to-ambient Power Dissipation of a QFP Package

Figure 2: Package Heat Dissipation Primary Paths and Resistances
The total power dissipation from the die is approximately the summation of heat flow through these two paths,

\[ P = Q_{JB} + Q_{JC}, \]

where \( Q_{JB} \) and \( Q_{JC} \) are power dissipations from junction to board and from junction to package case top surface, respectively. Figure 2 illustrates these two primary heat dissipation paths and the corresponding thermal resistances. The equivalent thermal resistor network of the two primary heat dissipation paths are shown in Figure 3. Using the equivalent thermal resistor network, Figure 3, junction-to-ambient thermal resistance, \( \theta_{JA} \), can be approximated by

\[ \theta_{JA} = \left( \frac{1}{R_B} + \frac{1}{R_C} \right)^{-1}, \]

where

\[ R_B = \theta_{JB} + \theta_{BS} + \theta_{BA}, \]

and

\[ R_C = \theta_{JC} + \theta_{CA}. \]

Figure 3: Package Equivalent Thermal Resistance Network of Primary Heat Dissipation Paths

In the above equations, \( \theta_{JB} \) is package junction-to-lead (junction-to-board) thermal resistance, \( \theta_{JC} \) is package junction-to-case (junction to package top surface) thermal resistance, \( \theta_{BS} \) is board heat spreading thermal resistance, \( \theta_{BA} \) is board-to-ambient thermal resistance, and \( \theta_{CA} \) is package case-to-ambient thermal resistance. It is apparent from Eq. [3] and Eq. [4] that \( \theta_{JA} \) decreases with the reduction of junction-to-board thermal resistance, \( \theta_{JB} \), and board heat spreading thermal resistance, \( \theta_{BS} \), values.
EXPOSED PAD LEADFRAME PACKAGES

An effective method of reducing $\theta_{JA}$ value is to use packages with low value of junction-to-board thermal resistance. Die-up leadframe packages with the die attach pad exposed on the bottom side provides an effective heat conduction bridge from die to PCB. Figure 4 illustrates the primary heat dissipation paths of an eTQFP package mounted on a PCB with the exposed pad soldered to the board. Compared with the QFP package shown in Figure 1, the eTQFP package moves the die attachment pad from inside the plastic mold to the bottom of the mold and exposed. In addition, soldering the exposed pad of eTQFP package directly on PCB, Figure 4, eliminates the heat dissipation barrier in QFP package due to the air gap between the plastic mold and the PCB, Figure 1.

The following highlights the general features related to board layout design and surface mount for exposed pad leadframe packages.

- Exposed pad surface is plated with solder and has the same surface finish as package terminal critical surface(s).
- When soldered to metal plane(s) on board, the exposed pad provides a primary power dissipation path for the package. Exposed pad lowers package junction-to-board thermal resistance, $\theta_{JB}$, and reduces junction-to-ambient thermal resistance when soldered to board.
- If the exposed pad is not soldered to board, there is no thermal improvement by using the exposed pad packages.
- Package exposed pad is typically connected to IC die ground pads to provide electrical GROUND connection (additional current return path for signals).
- Loop inductance is reduced if the exposed pad is connected to the ground pads on IC die and soldered to the ground plane(s) on PCB.
- Placing a copper land under the package exposed pad land area on PCB improves both package thermal performance and soldering of the exposed pad during surface mount process. The copper land under the exposed pad of the package on PCB is called PCB thermal land, or thermal land, in this document.
- Connecting the thermal land to the internal and/or backside planes with a matrix of plated through holes (PTH) could significantly improve package thermal and electrical performances.
- A matrix of solder paste squares printed on the thermal land is recommended for soldering the exposed pad onto thermal land.
As mentioned above, junction-to-ambient thermal resistance decreases with the reduction of \( \theta_{JB} \) and \( \theta_{BS} \) values according to Eq. [3] and Eq. [4]. Exposed pad packaging technology reduces thermal resistance to the heat flow from die to the package bottom surface, \( \theta_{JB} \). To realize the benefit of low resistance to heat flow between die and board, the exposed pad must be soldered to the thermal land on board in order to further channel the heat flow to the rest area of the board. The performance benefit of exposed pad packages can be maximized when the board layout provides continuous heat conduction paths such that the board spreading thermal resistance, \( \theta_{BS} \), is minimized in the region around the thermal land. The following sections provide guidelines for board layout and stencil designs that could help maximize package thermal performance and reduce potential failure risks for board assembly.

## PCB Layout Recommendations

PCB layout design provides a land pattern within the footprint of exposed pad package envelope such that the interconnection can be accomplished between package pins and the corresponding copper pads on PCB. In addition to the pins on the perimeter of package footprint, the exposed pad at the center of package bottom must be soldered to PCB for eTQFP and MLP packages. The mechanical integrity of solder joint at both perimeter pins and the exposed center pad are critical for the component to pass surface mount qualification requirements. These requirements include visual inspection, differential thermal expansion test, vibration test, thermal shock test, and, mechanical shock test [3, 4], and temperature cycling test [5].

Figure 5 shows the bottom views of eTQFP and MLP packages. The major differences between the two packages are the terminal type (shape) and location of the perimeter terminals relative to package mold body. The perimeter terminals of the leaded package, eTQFP, are gull wing leads that are bent down and extend beyond the body of package mold with the lead foot at the end pointing away from the package [1, 6]. The perimeter terminals of the leadless package, MLP, are located on the bottom of package mold body along its periphery. By design, these terminals are essentially flush with the bottom surface of the plastic package body [7]. Only the bottom surface of the terminals is metallized for surface mount purpose (for example, plated with solder) [2, 6]. The differences are further illustrated in the cross section drawings in Table 1.

The solder joint quality and integrity of a surface mount device on a PCB is a function of both land pattern design and soldering process control. Analysis of solder joints for eTQFP and MLP packages are presented in the following before the recommendations on PCB thermal land design for the exposed pad and land pattern design for package perimeter terminals.

![Figure 5: Bottom View of Die-up Leadframe Package with Exposed Die Attachment Pad: (a) eTQFP, (b) MLP](image-url)
TERMINAL SOLDER JOINT ANALYSIS AND REQUIREMENT FOR LEADED EXPOSED PAD PACKAGE: eTQFP

Solder joint requirements for leaded exposed pad package perimeter pins are the same as QFP packages. The general solder joint requirement is the indicated evidence of wetting and adherence where the solder spreads one the soldered surface, forming a contact angle of 90° or preferably less, except when the quantity of solder results in a contour which extends over the edge of the land or solder resist [Ref. 6, Section 9.2.4]. The solder joints should have a generally smooth appearance with smooth transition from land to connection surface of component lead. The requirement for wetting on both soldered surface and component terminal metallized connection surface is quantified by the location and extent of fillet requirements of solder joint.

Figure 6 provides the solder joint minimums for toe, heel, and side fillets for leaded expose pad packages from IPC standard [Ref. 8, Section 11.2]. An observable solder fillet is necessary as the evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. The dimensions for minimum solder fillets at the toe, heel, or side ($J_T$, $J_H$, $J_S$) have been determined based on industry empirical knowledge and reliability testing.

![Figure 6: Solder Joint Fillet Requirement for Leaded Exposed Pad Packages](from Ref. 8, Section 11.2)
**TERMINAL SOLDER JOINT ANALYSIS AND REQUIREMENT FOR LEADLESS EXPOSED PAD PACKAGE: MLP**

Solder joint requirements for leadless exposed pad package perimeter pins are not yet defined in IPC/EIA J-STD-001C [6]. The general solder joint requirement is the indicated evidence of wetting and adherence where the solder spreads on the soldered surface, forming a contact angle of 90° or preferably less, except when the quantity of solder results in a contour which extends over the edge of the land or solder resist [Section 9.2.4 of Ref. 6]. The solder joints should have a generally smooth appearance with smooth transition from land to connection surface of component lead. The requirement for wetting on both soldered surface and component terminal metallized surface is quantified by the location and extent of solder fillet requirements. For leadless exposed pad packages such as MLP, however, only the bottom surface of terminal is metallized to promote wetting of solder. The other surfaces of the package terminals are not finished to promote solder wetting. By design, there is no control to wet the side surfaces of MLP terminal with molten solder during reflow surface mount. Consequently, it is not required (by package design) to exhibit solder joint fillet on the terminal side surfaces, including the exposed surface on the side of package mold body, Figure 7.

![Figure 7: Solder Wetting on Terminal Side Surfaces (Including the Exposed Side Surface) is not Required for Leadless Exposed Pad Packages](image)

An observable solder fillet on PCB terminal pads is necessary for evidence of proper wetting. Solder joint minimums for toe, heel, and side fillets for leadless expose pad packages are yet to be defined by industry standardization organizations. Figure 8 and Table 2 provide the minimum requirement on solder joint length, width, thickness, end and side overhangs for no-lead exposed pad packages [Ref. 6, Section 9.2.6.4].
Figure 8: Solder Joint Length, Width, Thickness, and Overhangs for No-lead Exposed Pad Packages [Ref. 6, Figure 9-4]

Table 2: Dimensional Criteria for No-Lead Exposed Pad Packages [Ref. 6, Table 9-4]

<table>
<thead>
<tr>
<th>Feature</th>
<th>Dim.</th>
<th>Class 1 Requirement</th>
<th>Class 2 Requirement</th>
<th>Class 3 Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum End Overhang</td>
<td>B</td>
<td>Not Allowed</td>
<td>Not Allowed</td>
<td>Not Allowed</td>
</tr>
<tr>
<td>Minimum End Joint Width</td>
<td>C</td>
<td>Min ((\frac{1}{2} W, \frac{1}{2} P))</td>
<td>Min ((\frac{1}{2} W, \frac{1}{2} P))</td>
<td>Min ((\frac{2}{3} W, \frac{2}{3} P))</td>
</tr>
<tr>
<td>Minimum End Overlap</td>
<td>J</td>
<td>Required</td>
<td>Required</td>
<td>Required</td>
</tr>
</tbody>
</table>
PCB THERMAL LAND DESIGN GUIDELINES

A copper land, called PCB thermal land or thermal land herein, is required on PCB at the land location under the package exposed pad in order to provide self-centering mechanism for confinement of molten solder during surface mount process. In addition to improving the soldering of the exposed pad, the copper land also provides a launch pad for heat spreading to the rest area of PCB, Figure 9.

Figure 9: Junction-to-ambient Power Dissipation of an eTQFP Package
Figure 10: Size of PCB Thermal Land Plane for eTQFP Package

Figure 11: Size of PCB Thermal Land Plane for MLP Package
The following are recommendations for PCB thermal land design:

- Size of PCB thermal land area should be larger than the exposed pad of the package and smaller than the square defined by the PCB pads for the perimeter terminals of the package, Figure 10 and Figure 11. Figure 10 shows the thermal land size for eTQFP package and Figure 11 shows the thermal land size for MLP package.
- Metal minimum separation between the thermal land and the PCB pads for package terminals is 0.3mm (12mil) for eTQFP packages, Figure 10, and 0.25mm (10mil) for MLP packages, Figure 11. The size of thermal land on PCB could be either larger or smaller than the size of the exposed pad of package.
- Solder mask defined (SMD) opening or openings should be designed on the thermal land to capture molten solder during reflow and to allow electrical and thermal interconnections between the PCB thermal land and the exposed pad of the package.
- For packages with exposed pad size larger than 3.0mm x 3.0mm, evenly distributed a matrix of square solder mask openings on the thermal land. The recommended solder mask opening size is 0.9mm x 0.9mm (36mil x 36mil). The recommended pitch between the solder mask openings is 1.125mm (45 mil), Figure 12.
- For packages with exposed pad size of 3.0mm x 3.0mm or smaller, use one solder mask opening on the thermal land. The solder mask opening size should be the same as the package exposed pad, Figure 13.
- To account for solder mask registration accuracy, solder mask should overlap the edge of the thermal land plane by at least 75 µm, Figure 12, Figure 13 and Figure 14.
- A matrix of plated through hole (PTH) vias should be evenly distributed on the thermal land. These vias should be covered by solder mask to prevent molten solder wicking into the vias, Figure 12, Figure 13 and Figure 14.
- The four corners of the square solder mask openings should be chamfered such that the PTH vias can be placed at the corners in between solder mask openings and be covered by solder mask, Figure 9, Figure 10 and Figure 11.
- If a PTH via is partially or entirely within solder mask opening, it should be covered with solder mask cap, Figure 13. The solder mask cap diameter should be at least 0.1mm (4mil) larger than via drill diameter.
- For packages with exposed pad size larger than 3.0mm x 3.0mm, the pitch for the matrix of PTH vias on the thermal land should be 1.125mm (45 mil), same as the pitch of the solder mask openings, Figure 12. Via drill diameter is 0.25mm (10 mil). Solder mask cap diameter is 0.35mm (14 mil). Recommended plating on via barrel is 1oz. Cu, Figure 15.
- For packages with exposed pad size of 3.0mm x 3.0mm or smaller, the recommended pitch for the matrix of PTH vias on the thermal land is 0.9 ~ 1.0 mm (36 ~ 40 mil), Figure 13. Via drill diameter is 0.30mm (12 mil). Via pad and solder mask cap diameter is 0.40mm (16 mil). Recommended plating on via barrel is 1oz. Cu, Figure 16.
- Solid connection is recommended for via-to-plane and via-to-thermal land connections, Figure 17.
- Thermal relief designs for via-to-plane and via-to-thermal land connection are not recommended. Dog-bone or teardrop designs for via-to-via pad connection on thermal land, Figure 15(a), are NOT recommended. Web construction design for via-to-plane connection, Figure 18(b), is NOT recommended.
- If not capped/tented with solder mask, PTH vias on thermal land must be plugged with epoxy to prevent molten solder wicking through via holes. Epoxy plugged vias could allow higher via density on thermal land for thermal improvement.
- If it is not feasible to either tent the PTH vias on the thermal land or plug the vias with epoxy, the PTH vias may be tented with solder mask from the bottom side of the board as the last resort to prevent molten solder wicking through the via holes. This could potentially introduce solder balling problem during reflow as the trapped gas in PTH vias escapes from the top and blows away the molten solder surrounding the PTH vias. Use solder ball capture land in between the PTH vias and the component terminal pads on PCB could reduce the potential of rolling solder balls traveling to the package terminals and shorting the pins. Because the higher tendency of solder bridging at perimeter pins during part reflow, it is recommended to avoid tenting PTH vias from the bottom side of board.
- Higher density of vias on thermal land may be required for specific Broadcom devices. If provided in application notes or datasheet, the thermal land design guidelines for a specific device supersede the corresponding recommendations in this document.
Figure 12: Thermal Land Design Rule for Package with Exposed Pad Size Larger than 3mm x 3mm
Figure 13: Thermal Land Design Rule for Package with Exposed Pad Size 3mm x 3mm or Smaller

Figure 14: SMD Design Rule on Thermal Land – Cross Section View
Figure 15: Thermal via Design for Package with Exposed Pad Size Larger than 3mm x 3mm
Figure 16: Thermal via Design for Package with Exposed Pad Size 3mm x 3mm or Smaller

Figure 17: Recommended via Design Rule for Via-to-plane and Via-to-thermal Land Connections
Figure 18: Thermal Relief Should Not be Used for Via-to-plane and Via-to-thermal Land Connections

**DESIGN GUIDELINES OF PCB PADS FOR PACKAGE TERMINALS**

JEDEC standard terminal pitch for exposed pad leadframe packages are 0.40mm, 0.50mm, 0.65mm, 0.80mm 1.00mm, and 1.27mm. Because fine pitches such as 0.50mm and 0.65mm are frequently used in the exposed pad leadframe packages, the PCB pads for package perimeter terminals should be designed to prevent solder bridging, voiding, de-wetting, and other surface mount problems due to misalignment.

- Width of PCB pads for package terminals should be the same as package terminal width.
- Length of PCB pads for package terminals should be 0.15mm (6mil) longer than package terminal foot length to accommodate placement accuracy. The additional 0.15mm (6mil) length for PCB pads should extend 0.05mm (2mil) inward (toward package center) beyond the package terminal footprint and extend the remaining 0.10mm (4mil) outward beyond the package terminal footprint, Figure 19.
- Non-solder mask defined (NSMD) pad should be used for package terminal pads on PCB.
- For packages with terminal pitch of 0.50mm or larger, solder mask openings should be designed around each PCB pads for package terminals. The clearance between solder mask and the edge of PCB terminal pads is 75 µm (3mil), Figure 20.
- For packages with terminal pitch of 0.40mm, one large solder mask opening should be designed around all pads for each side of the package terminals with 75µm clearance between the edge of the solder mask opening and the edge of the nearest pad, Figure 21.
- Minimum solder mask web width is 100µm (4mil) to prevent delamination on PCB.
- Inner edge of solder mask should be rounded, Figure 20 and Figure 21.
Figure 19: PCB Pad Dimension for Package Terminal
Figure 20: Solder Mask Opening Around PCB Pad for Package with Terminal Pitch 0.50mm or Larger

Figure 21: Solder Mask Opening Around PCB Pad for Package with Terminal Pitch 0.40mm
STENCIL DESIGN RECOMMENDATIONS

For die-up exposed pad leadframe packages, the exposed pad must be soldered to PCB thermal land to connect the path of heat flow from die to PCB. The amount of solder paste required for proper soldering exposed pad packages is determined by the standoff height from the solderable surface of thermal land to the bottom surface of the exposed pad, solder paste properties such as collapse ratio, and package terminal pitch. The difference in the exposed pad standoff height for leaded and no-lead exposed pad packages requires different stencil thickness to minimize potential SMT defects. These defects may include voids, insufficient solder coverage under the exposed pad, solder bridging, opening or no connect due to package floating on the molten solder over thermal land, and solder balling. It is likely that the exposed pad package is not the only package on board for surface mount. Special attentions are required in stencil design for solder paste printing to accommodate variations of surface mount processes used in different board assembly factories as well as on different application board for the same device. We recommend that stencil pattern design for exposed pad package should be carefully considered in the early stage of surface mount process development at board assembly factory. The following provides design guidelines for exposed pad package stencil patterns.

- Use stainless steel for solder paste print stencil.
- For exposed pad package with terminal pitch of 0.40mm, recommended stencil thickness is 5mil (0.125mm).
- For exposed pad package with terminal pitch of 0.50mm and larger, stencil thickness should be 6mil (0.15mm).
- Stencil aperture size for NSMD terminal pads should be the same as the pad size on PCB, Figure 22.
- For packages with exposed pad size larger than 3mm x 3mm, stencil aperture pattern and size on thermal land should be the same as the SMD pad opening pattern and size, Figure 23.
- For packages with exposed pad size at and smaller than 3mm x 3mm, stencil pattern is 4 apertures of the same size with outside edge of the 4 apertures match the SMD pad opening. Edge-to-edge thickness between stencil apertures is 0.225mm (9mil) on the thermal land, Figure 24.
- Minimum edge-to-edge thickness between stencil apertures is 0.2mm (8mil), Figure 21.

![Stencil Design Recommendations Diagram](image-url)
Figure 23: Thermal LandStencil Design for Package with Exposed Pad Size Larger than 3mm x 3mm

Figure 24: Stencil Design on Thermal Land for Package with Exposed Pad Size 3mm x 3mm or Smaller
REFLOW SOLDERING RECOMMENDATIONS

Broadcom does not provide device specific reflow profiles. The following summarizes reflow-soldering general guidelines. Customer should conduct reflow tests to optimize reflow profile for specific board. Further information is available in the Broadcom package application note [9] and JEDEC document [10].

Figure 25 shows a reference convection reflow profile. The parameter values for the reference reflow profile are provided in Table 3.

![Figure 25: Reference Reflow Profile](image)

<table>
<thead>
<tr>
<th>Profile Feature</th>
<th>Sn-Pb Eutectic Assembly</th>
<th>Pb-Free Assembly</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average ramp-up rate (T_L to T_p)</td>
<td>3°C/second max.</td>
<td>3°C/second max.</td>
</tr>
<tr>
<td>Preheat</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Temperature Min (T_{min})</td>
<td>100 °C</td>
<td>150 °C</td>
</tr>
<tr>
<td>• Temperature Max (T_{max})</td>
<td>150 °C</td>
<td>200 °C</td>
</tr>
<tr>
<td>• Time (min to max) (ts)</td>
<td>60-120 seconds</td>
<td>60-180 seconds</td>
</tr>
<tr>
<td>T_{max} to T_L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Ramp-up Rate</td>
<td>3°C/second max</td>
<td>3°C/second max</td>
</tr>
<tr>
<td>Time maintained above:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Temperature (T_L)</td>
<td>183 °C</td>
<td>217 °C</td>
</tr>
<tr>
<td>• Time (t_L)</td>
<td>60-150 seconds</td>
<td>60-150 seconds</td>
</tr>
</tbody>
</table>
Rework Recommendations for Exposed Pad Leadframe Packages

The exposed pad soldered on PCB provides excellent heat sinking capability to the exposed pad leadframe packages. The exposed pad also presents additional requirements to the package rework procedures. The body size of the exposed pad packages is typically small. The exposed pad is hidden underneath the package mold body. In order to heat up the exposed pad above solder melting point during part removal process, the package mold body is typically exposed to higher temperatures than the same size leaded leadframe packages without exposed pad. Broadcom follows the industry standard JESD22-A113C [11] for package preconditioning tests prior to reliability testing which include three cycles of reflow conditions. A package that has been attached to a board and then removed has already been exposed twice to the peak temperature conditions of reflow. If the board is double sided the package could have been exposed to three times reflow peak temperatures. Because of the potential for the exposed pad packages to be exposed to elevated temperatures during package removal from PCB and the closeness of the package to be at the end of the tested and qualified range of known survivability, we recommend that the component in exposed pad package should not be reused after removal from PCB.

The following are recommended procedures and requirements for the rework of exposed pad leadframe packages.

1. Pre-bake board for moisture removal – It is recommended to bake board assembly at 125 °C ±5/-0 °C for 4 to 24 hours before rework to release residual moisture that may cause failures in other components such as “popcorning”.

2. Part removal – After baking, the board is then placed in the rework holder and heated again to 125 °C. The board should be horizontally placed. Tilt of board could result in solder bridging during part removal. Hot air removal using specialized vacuum collets is recommended. These collets incorporate a high gas shroud that heats the part to the required reflow temperature. To prevent board warpage due to localized heating for part removal, it is recommended that the board underside also be heated to a temperature of 100 °C to 125 °C.

3. Site cleaning – After removal of component, the site must be cleaned of residual solder. This can be done on a de-soldering station and using solder wick. Special care must be taken to avoid applied temperature on the land area higher than 245 °C, which could damage the solder mask material and the copper pads. Use alcohol with a lint-free brush or swab to clear the reworked area.

4. Solder paste deposition – A mini-stencil is recommended for manually screen-printing of solder paste on the land area. The stencil should have the same thickness, aperture opening and pattern as the original stencil at the component site.

Note 1- All temperatures refer to topside of the package, measured on the package body surface.

Note 2- All exposed pad leadframe packages currently used at Broadcom are considered small body packages with thickness < 2.5mm or package volume < 350 mm³.

Note 3- Package volume excludes external terminals (leads, lands, ext.) and non-internal heat sinks.

Note 4- It is possible that very large (≥ 350 mm³), thick (≥ 2.5mm) boards that use components with a wide range of thermal mass, and/or boards undergoing rework, might have difficulty maintaining all component below the maximum temperatures in this specification. In such cases, the MSL level must be determined for the body temperature the component attains.

Table 3: Reference Reflow Profile Parameters (Cont.)

<table>
<thead>
<tr>
<th>Profile Feature</th>
<th>Sn-Pb Eutectic Assembly</th>
<th>Pb-Free Assembly</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak temperature (Tp)</td>
<td>240 ±0/-5 °C</td>
<td>255 ±0/-5 °C</td>
</tr>
<tr>
<td>Time within 5°C of actual peak</td>
<td>10-30 seconds</td>
<td>20-40 seconds</td>
</tr>
<tr>
<td>temperature (tp)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ramp-down rate</td>
<td>6 °C/second max.</td>
<td>6 °C/second max.</td>
</tr>
<tr>
<td>Time 25°C to peak temperature</td>
<td>6 minutes max.</td>
<td>8 minutes max.</td>
</tr>
</tbody>
</table>
The printed site should be inspected under a microscope for location accuracy, solder paste volume, and even distribution of solder paste before component placement. If unacceptable, the solder paste should be removed and the site should be re-cleaned for solder paste deposition.

5 Component placement – Use a component placement station equipped with vacuum nozzle, XY table and split field vision system that can display both the package leads and the copper pads on the PCB. Place a new package on the tip of the vacuum nozzle. Once the two images of the package leads and the copper pads on PCB are aligned, the package is placed down on the PCB land area. Visual inspection of misalignment under a microscope is required. Care must be taken during inspection and board transportation not to shake or overly tile the board that may cause the part out of alignment.

6 Reflow soldering – Localized heating of the reworked site is recommended to mount the new component on board. The gas shroud used for component removal (Step 2) is recommended for the localized reflow soldering. Temperature profile should be similar to the original board reflow surface mount temperature profile and the reflow soldering temperature requirements in this document (Table 3, Section 7) should be followed.

7 Board cleaning – Remove residues from the board. Board cleaning is not required if no-clean solder paste/flux is used for rework.

8 Final inspection – Visually inspect package perimeter terminals for solder joint defects per requirements in Section 5.1 for leaded exposed pad packages and Section 5.2 for no-lead exposed pad packages. Use X-Ray to exam the solder joint between the exposed pad and the PCB for solder coverage under the exposed pad. Recommended solder coverage area ratio is above 60%.