AFBR-89CDDZ

QSFP28 Pluggable, Parallel Fiber-Optics Module
100 Gigabit Ethernet Applications
850nm SR4, MMF, MPO Connector

Data Sheet

Description

The Avago Technologies AFBR-89CDDZ is a Four-Channel, Pluggable, Multi-mode, Fiber-Optic QSFP28 transceiver for 100 Gigabit Ethernet Applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnect applications. It integrates four data lanes in each direction with each lane operating at 25.78125 Gbps, giving an aggregated bandwidth of 103.125 Gbps. It allows optical interoperability up to 100m over an 8-fiber (or 12-fiber) MPO optical multi-mode OM4 cable. The pull tab facilitates the insertion and extraction of these transceivers in high density environment. Each electrical lane operates at 25.78125 Gbps and conforms to the 100GE CAUI4 interface with 802.3 Clause 91 RS-FEC.

Per channel transmitter and receiver retimers, configured for 4x25G operation, can be bypassed to enable alternative data rate transmission.

These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 38 contact QSFP28 edge type connector. The optical interface uses a conventional 8-fiber (or 12-fiber) MPO connector. This module incorporates Avago Technologies proven integrated circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Part Number Ordering Options

100 Gigabit Ethernet	AFBR-89CDDZ
Evaluation Board*	AFBR-89EVB
Evaluation Kit**	AFBR-89EVK

* Includes GUI and User Guide
**Includes GUI, User Guide, I2C controller, and power supply cable

Features

- Compliant to 100GbE electrical and optical specifications 802.3bm (Annex 83E CAUI-4 with Clause 91 RS-FEC, Clause 95 100GBASE-SR4)
- 100GbE Link Distances 100m OM4, 70m OM3
- QSFP28 MSA Specification Compliant, including new functions per SFF-8636 Rev 2.4
- Class 1 Eye Safety
- Pull tab: ease of transceiver insertion and extraction
- Operates at 25.78125 Gbps per channel with 64b/66b coded data
- 0 to +70 °C case temperature operating range
- Proven High Reliability 850 nm technology: Avago VCSEL transmitter and Avago PIN detector
- Hot pluggable QSFP28 transceiver for ease of installation and servicing
- Two Wire Serial (TWS) interface with Digital Monitoring and maskable interrupts for expanded functionality

Applications

- 100 Gigabit Ethernet interconnects
- Datacom/Telecom switch & router connections
- Data aggregation and backplane applications
- Proprietary protocol and density applications

QSFP28 Relevant Specifications per SFF-8024 (rev 3.3)

Steering Document	Low Speed, Connector and Electrical Requirements	Common Management Spec / Memory Map	Form factor / Module Mechanical	Cage / Connector Solution	
SFF-8665	SFF-8679	SFF-8636	SFF-8661	SFF-8662 and SFF-8663	Style A
				SFF-8672 and SFF-8683	Style B

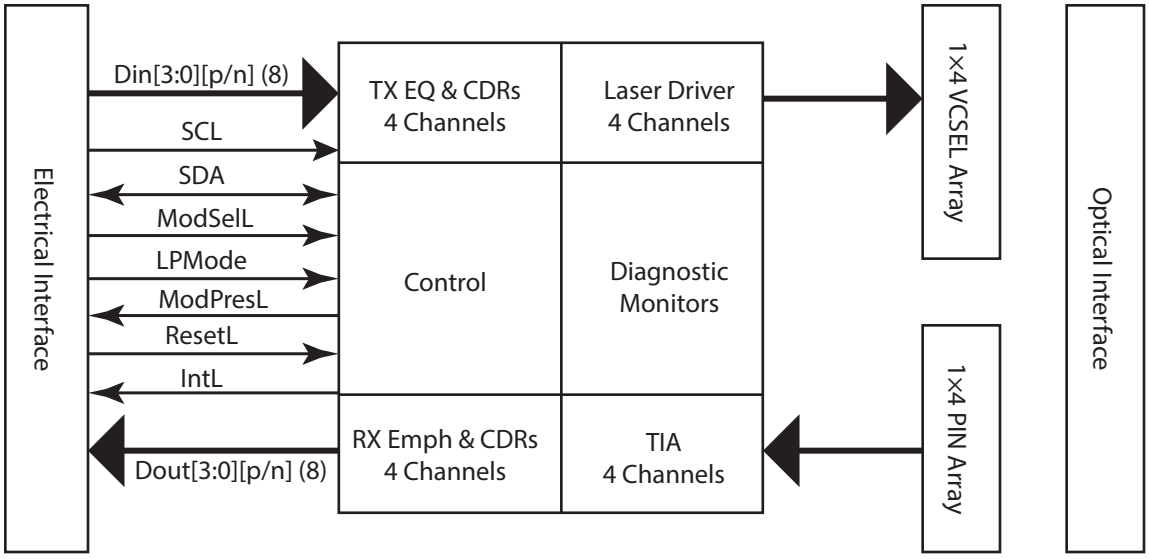

Figure 1: Transceiver Block Diagram

Transmitter

The optical transmitter portion of the transceiver (see Figure 1) incorporates a 4-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 4-channel Equalization (EQ) block with integrated CDR and laser driver, diagnostic monitors, control and bias blocks. The transmitter is designed for IEC-60825 and CDRH eye safety compliance; Class 1 out of the module. The Tx Input Buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 Ohms. AC coupling capacitors are located inside the QSFP28 module and are not required on the host board. For module control and interrogation, the control interface (LVTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals. Diagnostic monitors for VCSEL bias, temperature, and power supply voltage are implemented and results are available through the TWS interface.

Alarm and warning thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register. The optical output will squelch for loss of input signal unless squelch is disabled. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm/warning and fault information are available via the TWS interface. To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of alarm, warning, LOS and/or Tx fault.

Receiver

The optical receiver portion of the transceiver (see Figure 1) incorporates a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4 channel line driver with integral CDR, diagnostic monitors, control and bias blocks. The Rx Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 100 Ohms differentially that should be differentially terminated with 100 Ohms. AC coupling capacitors are located inside the QSFP28 module and are not required on the host board. Diagnostic monitors for optical input power are implemented and results are available through the TWS interface.

Alarm and warning thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of optical input signal (LOS). All flags are latched and will remain set even if the condition initiating the flag clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register. The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. Status and alarm/warning information are available via the TWS interface. To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of alarm, warning and/or LOS.

High Speed Electrical Signal Interface

Figure 2 shows the interface between an ASIC/SerDes and the QSFP28 module. For simplicity, only one channel is shown. The high speed signal lines are AC-coupled 100 Ohm differential lines. The AC coupling is inside the QSFP28 module and not required on the host board. The 100 Ohm differential terminations are inside the QSFP28 module for the transmitter lines and at the host ASIC/SerDes for the Receiver lines.

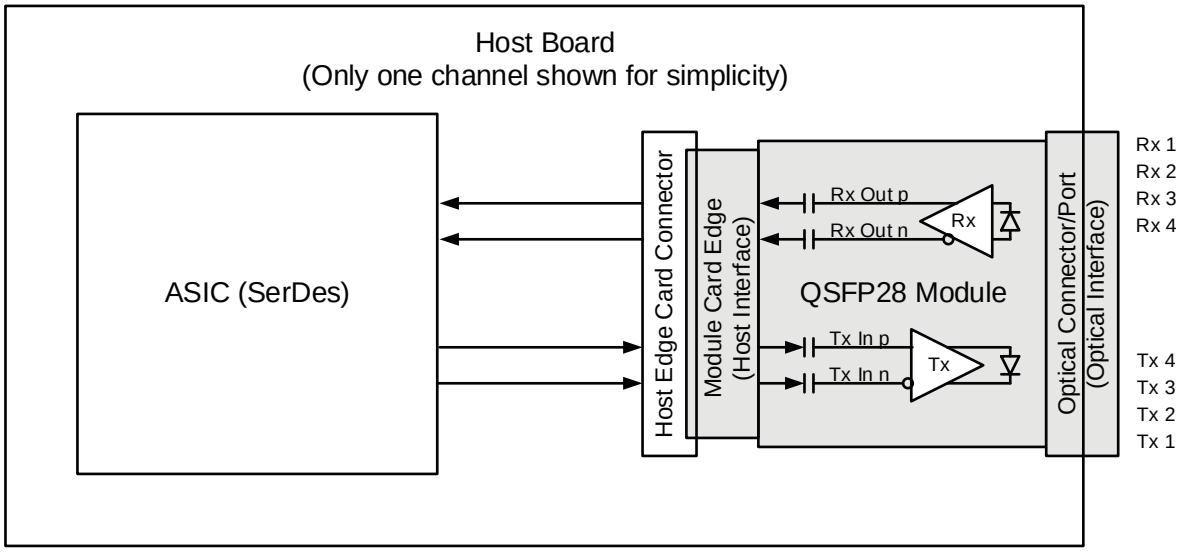

Figure 2: Application Reference Diagram

Control Signal Interface

The module has the following low speed signals for control and status: ModSelL, LPMode, ResetL, ModPrsL, IntL. In addition, there is an industry standard two wire serial interface scaled for 3.3 volt LVTTL. It is implemented as a slave device. Signal and timing characteristics are further defined in the Control Characteristics and Control Interface & Memory Map sections.

The registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Digital Diagnostic Monitoring

The information provides opportunity for predictive failure identification, compliance prediction, fault isolation and component monitoring.

Predictive Failure Identification – The diagnostic information allows the host system to identify potential link problems. Once identified, a "failover" technique can be used to isolate and replace suspect devices before system uptime is impacted.

Compliance Prediction – The real-time diagnostic parameters can be monitored to alert the system when operating limits are exceeded and compliance cannot be ensured. As an example, the real time average receiver optical power can be used to assess the compliance of the cable plant and remote transmitter.

Fault Isolation – The diagnostic information can allow the host to pinpoint the location of a link problem and accelerate system servicing and minimize downtime.

Component Monitoring – As part of host system qualification and verification, real time transceiver diagnostic information can be combined with system level monitoring to ensure performance and operating environment are meeting application requirements.

Digital diagnostic monitoring for the following attributes is implemented.

Transceiver module temperature

Represents the module case temperature (lower page 0 bytes 22-23)

Transceiver module power supply

Reports the module +3.3V supply voltage (lower page 0 bytes 26-27)

Transmitter output power

Reports the average output optical power for each transmitter channel (lower page 0 bytes 50-51 for ch.1, bytes 52-53 for ch.2, bytes 54-55 for ch.3, bytes 56-57 for ch.4)

Transmitter laser bias current

Reports the DC laser bias current for each transmitter channel (lower page 0 bytes 42-43 for ch.1, bytes 44-45 for ch.2, bytes 46-47 for ch.3, bytes 48-49 for ch.4)

Receiver input power

Reports the average input optical power for each receiver channel (lower page 0 bytes 34-35 for ch.1, bytes 36-37 for ch.2, bytes 38-39 for ch.3, bytes 40-41 for ch.4)

All diagnostic monitor attributes are two-byte fields. To maintain coherency, the host must access these with single two-byte read sequences.

For each monitored attribute, alarm and warning thresholds are established. Flags are set and interrupts generated when the attributes are outside the thresholds. All flags are latched and will remain set even if the condition initiating the flag clears. A mask bit that can be set to prevent assertion of interrupt for each individual attribute exists for every monitor flag. Entries in the mask fields are volatile.

Package Outline

The module is designed to meet the package outline defined in the QSFP28 SFF-8661 specification. See the package outline for details.

Handling and Cleaning

The transceiver module can be damaged by exposure to current surges and over voltage events. Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Wave soldering, reflow soldering and/or aqueous wash process with the modules on board are not recommended. Normal handling precautions for electrostatic discharge sensitive devices should be observed.

Each module is supplied with an inserted port plug for protection of the optical ports. This plug should always be in place whenever a fiber cable is not inserted.

The optical connector includes recessed elements that are exposed whenever a cable or port plug is not inserted. Prior to insertion of a fiber optic cable, it is recommended that the cable end be cleaned to avoid contamination from the cable plug. The port plug ensures the optics remains clean and no additional cleaning should be needed. In the event of contamination, dry nitrogen or clean dry air at less than 20 psi can be used to dislodge the contamination. The optical port features (e.g. guide pins) preclude use of a solid instrument. Liquids are also not advised.

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Units	Reference
Storage Temperature	Ts	-40	85	°C	
3.3 V Power Supply Voltage	Vcc	-0.5	3.6	V	
Data Input Voltage – Single Ended		-0.5	Vcc + 0.5	V	
Data Input Voltage – Differential	|VDIp – VDIn|		0.8	V	1
Control Input Voltage	Vi	-0.5	Vcc + 0.5, 3.6	V	
Control Output Current	Io	-20	20	mA	
Relative Humidity	RH	5	95	%	

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Case Temperature	Tc	0		70	°C	2
3.3 V Power Supply Voltage	Vcc	3.1	3.3	3.465	V	
Signal Rate per Channel, 100GbE			25.78125		GBd	3
Power Supply Noise				66	mVpp	4
Receiver Differential Data Output Load			100		Ohm	
Fiber Length (OM3)		0.5		70	m	5
Fiber Length (OM4)		0.5		100	m	6
* Control signals, LVTTL (3.3 V) compatible						

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[1] This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. Per SFF-8679, the damage threshold of the module input shall be at least 1600 mV peak to peak differential.

[2] The position of case temperature measurement is shown in Figure 7. Continuous operation at the maximum Recommended Operating Case Temperature should be avoided in order not to degrade reliability.

[3] 64b/66b coding. This translates to a nominal unit interval of 38.787879 ps.

[4] Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 8 for recommended power supply filter.

[5] OM3 fiber effective modal bandwidth is 2000 MHz·km 50µm MMF (minimum). The RS-FEC correction function may not be bypassed for any operating distance. The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. The loss of a single connection shall not exceed 0.75 dB.

[6] OM4 fiber effective modal bandwidth is 4700 MHz·km 50µm MMF(minimum). The RS-FEC correction function may not be bypassed for any operating distance. The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. The loss of a single connection shall not exceed 0.75 dB.

General Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Symbols	Min	Typ	Max	Units	Reference
Transceiver Power Consumption			2.51	3.5	W	Power Class 4
Transceiver Power Supply Current			762		mA	
AC coupling capacitors (Internal)			0.1		µF	
* For control signal timing including ModSelL, LPMode, ResetL, ModPrsL, IntL, SCL and SDA see Control Interface Section.						

High Speed Electrical Module Input Characteristics

From CAUI-4, 802.3bm Clause 83E, Table 83E-7.

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Signaling Rate, Per Lane	TP1		25.78125		GBd	± 100 ppm
Differential pk-pk Input Voltage Tolerance	TP1a	900			mV	
Differential Input Return Loss	TP1	Eq 83E-5			dB	802.3bm
Differential to common mode input return loss	TP1	Eq 83E-6			dB	802.3bm
Differential Termination Mismatch	TP1			10	%	
Module stressed input test	TP1a		83E.3.4.1			802.3bm, below
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode voltage	TP1	-0.350		2.85	V	1

Parameter	Value	Units	Notes/Conditions
Module stressed input test			2
Eye width	0.46	UI	
Applied pk-pk sinusoidal jitter	Table IEEE 802.3bm 88-13		
Eye height	95	mV	

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Electrical Input LOS Assert Threshold, Differential Peak-to-Peak Voltage Swing	ΔVdi pp los	50			mVpp	
LOS Hysteresis		0.5		4	dB	3

[1] DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

[2] Module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1

[3] LOS Hysteresis is defined as 20*Log(LOS De-assert Level / LOS Assert Level).

Reference Points

Test Point	Description
TP0	Host ASIC transmitter output at ASIC package pin on a DUT board
TP1	Input to module compliance board through mated module compliance board and module connector. Used to test module input
TP1A	Host ASIC transmitter output across the Host Board and Host Edge Card connector at the output of the host compliance board
TP2	Optical transmitter output as measured at the end of a 2-5m patch cord mated to the optical module
TP3	Optical test point as measured at the end of an optical fiber cable; closest test point to the presumed optical receiver input.
TP4	Module output through mated module and host edge card connector through module compliance board
TP4A	Input to host compliance board through mated host compliance board and host edge card connector. Used to test host input
TP5	Input to host ASIC

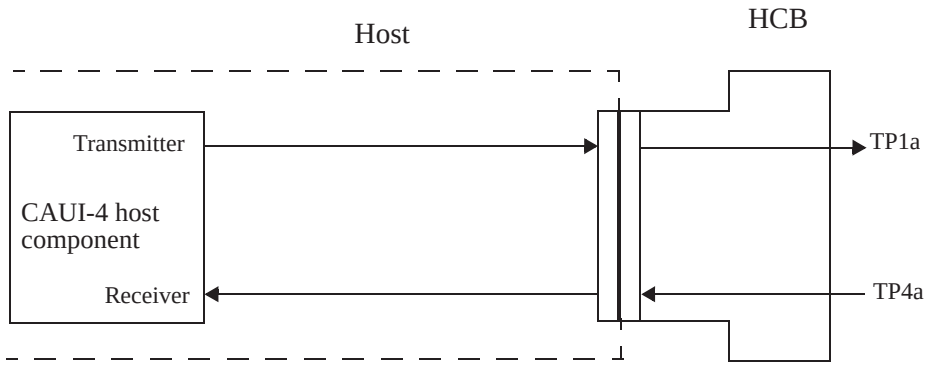


Figure 3: IEEE 802.3bm CAUI-4 Compliance Points TP1a, TP4a

Note a reference receiver is used to measure host eye width and eye height at TP1a. The reference receiver includes a selectable continuous time linear equalizer (CTLE) which is described by Equation (83E–4, below) with coefficients given in Table 83E–2.

$$H(f) = (G P_1 P_2) / Z_1$$

Where

H(f) is the CTLE transfer function, f is the frequency in GHz

G is the CTLE gain

P_1, P_2 are the CTLE poles in Grad/s

Z_1 is the CTLE zero in Grad/s

Reference CTLE Coefficients (Table 83E-2, IEEE 802.3bm)

25.78125GBd				
Peaking (dB)	**G**	**P/2π (GHz)**	**P2/2π (GHz)**	**Z1/2π (GHz)**
1	0.89125	18.6	14.1	8.364
2	0.79433	18.6	14.1	7.099
3	0.70795	15.6	14.1	5.676
4	0.63096	15.6	14.1	4.9601
5	0.56234	15.6	14.1	4.358
6	0.50119	15.6	14.1	3.844
7	0.44668	15.6	14.1	3.399
8	0.39811	15.6	14.1	3.012
9	0.35481	15.6	14.1	2.672

High Speed Electrical Module Output Characteristics

From CAUI-4, 802.3bm Clause 83E, Table 83E-3.

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min	Typ	Max	Units	Notes/Conditions
Signaling Rate, Per Lane	TP4		25.78125		GBd	+/- 100 ppm
AC common-mode output voltage (max, RMS)	TP4			17.5	mV, rms	
Differential Output Voltage	TP4			900	mV	
Eye Width	TP4	0.57			UI	
Eye Height, Differential	TP4	228			mV	
Vertical Eye Closure	TP4			5.5	dB	
Differential Output Return Loss, min	TP4		Eq 83E-2		dB	802.3bm
Common to differential mode conversion return loss (min)	TP4		Eq 83E-3		dB	802.3bm
Differential termination mismatch	TP4			10	%	
Transition Time (20% to 80%)	TP4	12			ps	
DC common mode voltage	TP4	-0.35		2.85	V	1

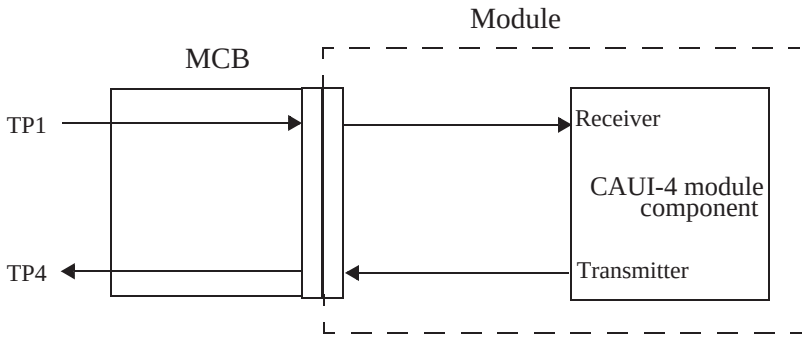


Figure 4: IEEE 802.3bm CAUI-4 Compliance Points TP1, TP4

[1] Capacitively coupled module output is compatible with DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

High Speed Optical Transmitter Characteristics

From 100GBASE-SR4, 802.3bm Clause 95, Table 95-6.

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point*	Min	Typ	Max		Notes/Conditions
Signaling Rate, Per Lane			25.78125			+/- 100ppm
Center wavelength range	TP2	840		860	nm	
RMS spectral width[1]	TP2			0.60	nm	
Average launch power, each lane	TP2	-8.4	—	+2.4	dBm	
Optical Modulation Amplitude (OMA) each lane	TP2	-6.4[2]	—	+3.0	dBm	
Launch Power in OMA minus TDEC, each lane	TP2	-7.3			dBm	
Transmitter and dispersion eye closure (TDEC), each lane	TP2			4.3	dB	
Average launch power of OFF transmitter, each lane	TP2	—		-30	dBm	
Extinction ratio	TP2	2	—	—	dB	
Optical return loss tolerance	TP2			12	dB	
Encircled Flux[3]	TP2	≥ 86% at 19 µm ≤ 30% at 4.5 µm				Type A1a.2 50 µm Fiber per IEC 61280-1-4
Transmitter Eye Mask definition: {X1, X2, X3, Y1, Y2, Y3}	TP2	SPECIFICATION VALUES {0.3, 0.38, 0.45, 0.35, 0.41, 0.5}				Hit Ratio 1.5×10^{-3} hits per sample

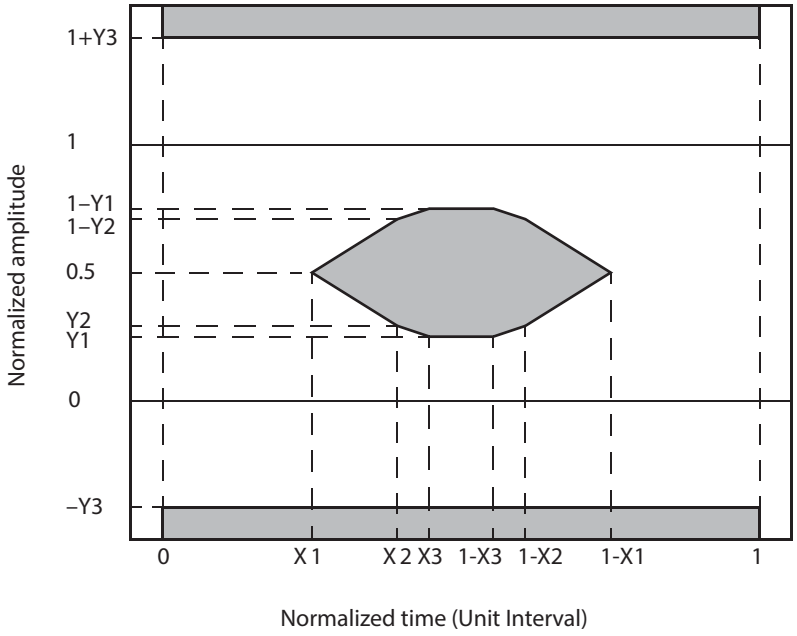


Figure 5: Transmitter Eye Mask Definitions

[1] RMS spectral width is the standard deviation of the spectrum.

[2] Even if the TDEC < 0.9dB, the OMA (min) must exceed this value.

[3] If measured into type A1a.2 50 µm fiber in accordance with IEC 61280-1-4.

High Speed Optical Receiver Characteristics

From 100GBASE-SR4, 802.3bm Clause 95, Table 95-7.

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point*	Min	Typ	Max	Units	Notes/Conditions
Signaling Rate, Per Lane			25.78125		Gbps	+/- 100ppm
Center wavelength range, each lane	TP3	840		860	nm	
Damage Threshold[1]	TP3	+3.4			dBm	
Average Receive Power, each lane[2]	TP3	-10.3		+2.4	dBm	
Receive Power (OMA), each lane	TP3			+3.0	dBm	
Receiver Reflectance	TP3			-12	dB	
Stressed Receiver Sensitivity OMA[3] , each lane	TP3			-5.2	dBm	
Conditions of stressed receiver sensitivity test[4]						
Stressed eye closure (SEC), lane under test			4.3		dB	
Stressed eye J2 jitter, lane under test			0.39		UI	
Stressed eye J4 jitter, lane under test			0.53		UI	
OMA of each aggressor lane			3		dBm	
Stressed Receiver Eye mask definition: X1, X2, X3, Y1, Y2, Y3		SPECIFICATION VALUES {0.28, 0.50, 0.50, 0.33, 0.33, 0.40}				Hit Ratio 5 x 10^{-5} hits per sample

Parameter	Test Point*	Min	Typ	Max	Units	Notes/Conditions
LOS Assert - OMA	TP3	-30			dBm	
LOS De-Assert - OMA	TP3			-9.1	dBm	
LOS Hysteresis	TP3	0.5			dB	

[1] The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power

[2] Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

[3] Measured with conformance test signal at TP3 (see 802.3bm section 95.8.8) for BER specified in 802.3bm section 95.1.1.

[4] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Regulatory Compliance

The AFBR-89CDDZ complies with all applicable laws and regulations as detailed in the Regulatory Compliance Table. Certification level is dependent on the overall configuration of the host equipment. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

The AFBR-89CDDZ is compatible with ESD levels found in typical manufacturing and operating environments as described in the Regulatory Compliance Table. In the normal handling and operation of optical transceivers, ESD is of concern in two circumstances.

The first case is during handling of the transceiver prior to insertion into a QSFP compliant cage. To protect the device, it is important to use normal ESD handling precautions. These include use of grounded wrist straps, workbenches and floor wherever a transceiver is handled.

The second case to consider is static discharges to the exterior of the host equipment chassis after installation. If the optical interface is exposed to the exterior of the host equipment cabinet, the transceiver may be subject to system level ESD requirements.

Electromagnetic Interference (EMI)

Equipment incorporating multi-gigabit transceivers is typically subject to regulation by the FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. The AFBR-89CDDZ compliance to these standards is detailed in the Regulatory Compliance Table. The metal housing and shielded design of the AFBR-89CDDZ minimizes the EMI challenge facing the equipment designer.

Flammability

The AFBR-89CDDZ optical transceiver is made of metal and high strength, heat resistant, chemical resistant and UL94V-0 flame retardant plastic.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	EN61000-4-2, Criterion B	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing 	US FDA CDRH AEL Class 1 US21 CFR, Subchapter J per Paragraphs 1002.10 and 1002.12 (IEC) EN60825-1:2007 (IEC) EN60825-2:2004 +A1+A2 (IEC) EN60950-1:2006 +A11 +A1+A12 +A2	CDRH Certification: 9720151-148 TUV File: R 72141786
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E173874
RoHS Compliance		Less than 1000 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls (PPB) and polybrominated biphenyl ethers (PBDE).

QSFP28 Transceiver Pad Layout

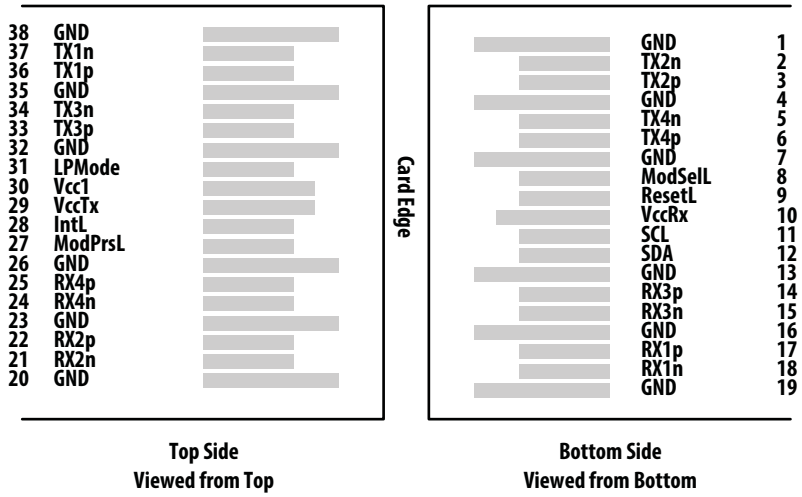


Figure 6: QSFP28 Module Pin Layout

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	3
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	3
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	3
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select, When held low by the host, the module responds to 2-wire serial communication commands.	3	
9	LVTTL-I	ResetL	Module Reset, The ResetL signal is pulled up to Vcc in the QSFP28 module.	3	
10		Vcc Rx	+3.3V Power supply receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock, Requires pull-up resistor to 3.3V on the host board.	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data, Requires pull-up resistor to 3.3V on the host board.	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3	3
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	3
18	CML-O	Rx1n	Receiver Inverted Data Output	3	3
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	3
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	3
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	3

Pin	Logic	Symbol	Description	Plug Sequence	Notes
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	3
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present, Requires pull-up resistor to 3.3V on the host board. Module Present is pulled low in the module.	3	
28	LVTTL-O	IntL	Interrupt, the IntL signal is an open collector output and must be pulled to host supply voltage (3.3V) on the host board.	3	
29		Vcc Tx	+3.3V Power Supply	2	2
30		Vcc1	+3.3V Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode. LPMode is pulled up to Vcc in the module.	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	3
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	3
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	3
38		GND	Ground	1	1

Note 1: GND is the symbol for signal supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

Note 3: For all Tx and Rx High-Speed differential inputs/outputs, there are 0.1uF AC coupling capacitors located inside the QSFP28 module and are not required on the host board.

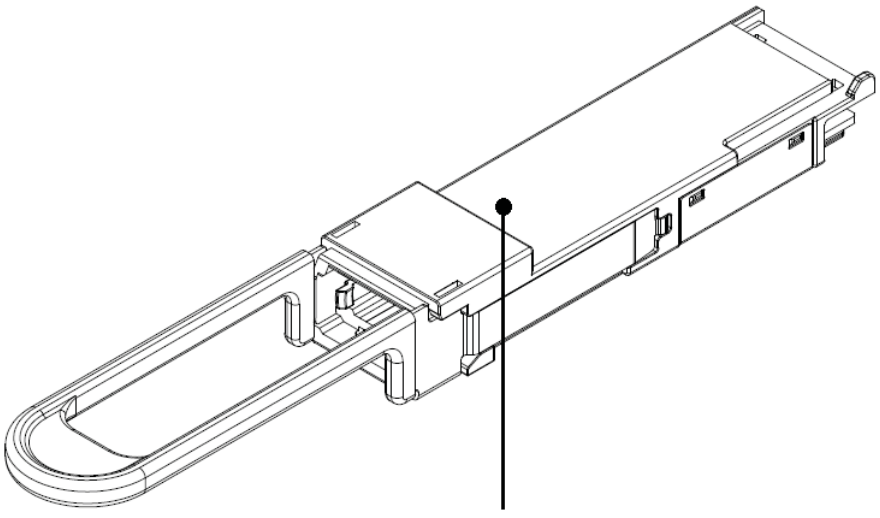


Figure 7: Case Temperature Measurement Point

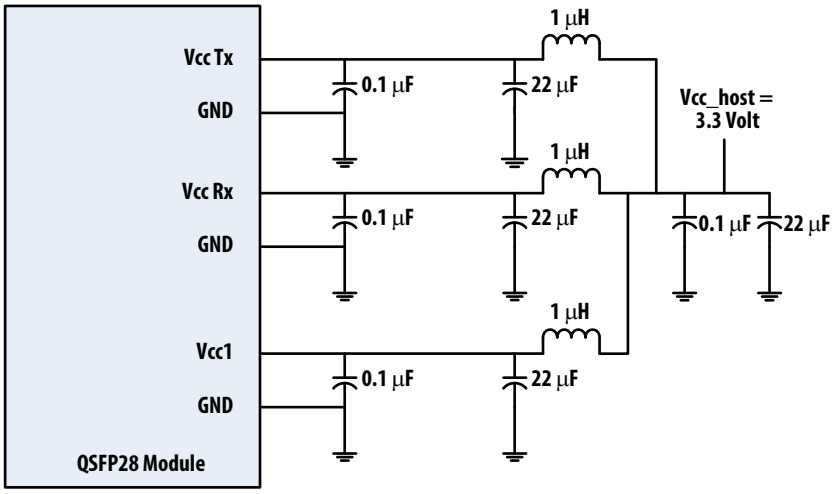


Figure 8: Recommended Power Supply Filter

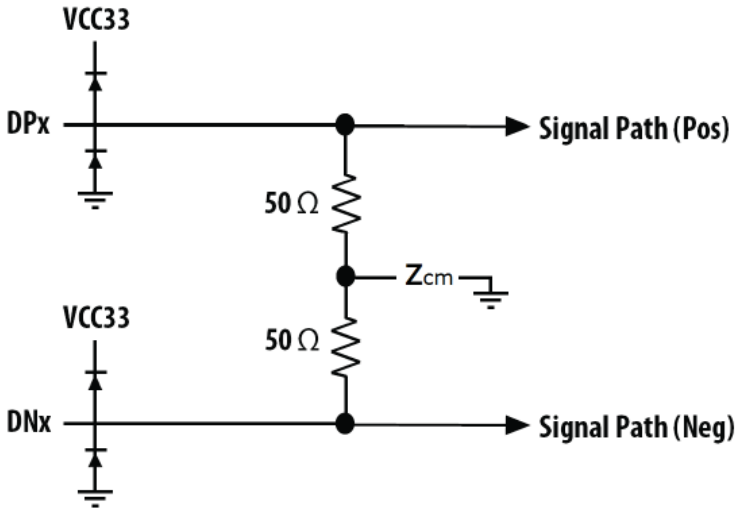


Figure 9: Transmitter Data Input Equivalent Circuit

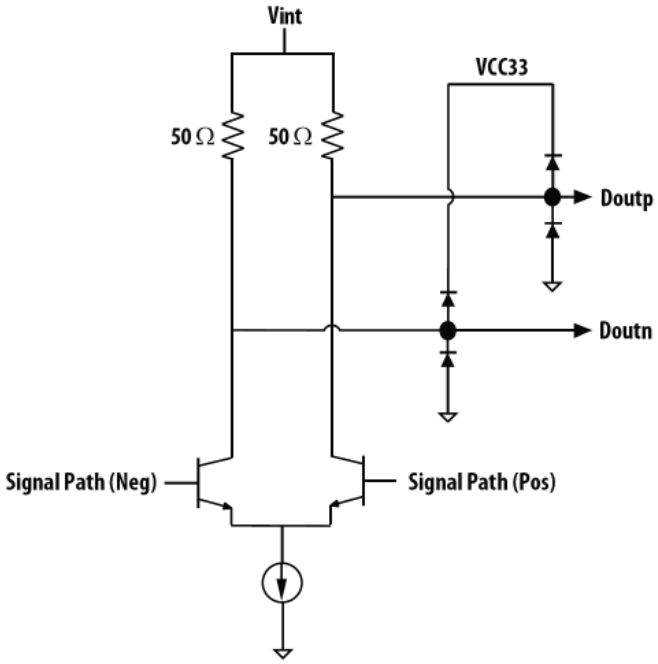


Figure 10: Receiver Data Output Equivalent Circuit

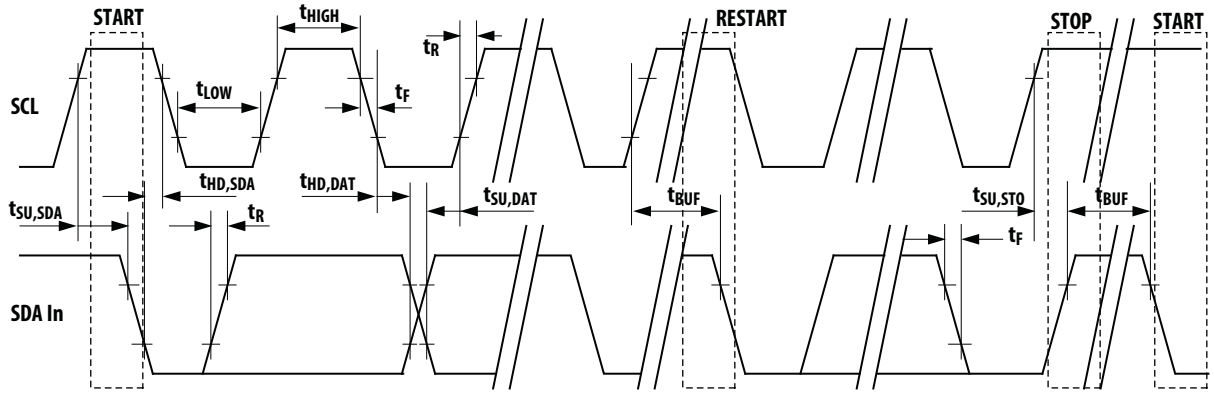
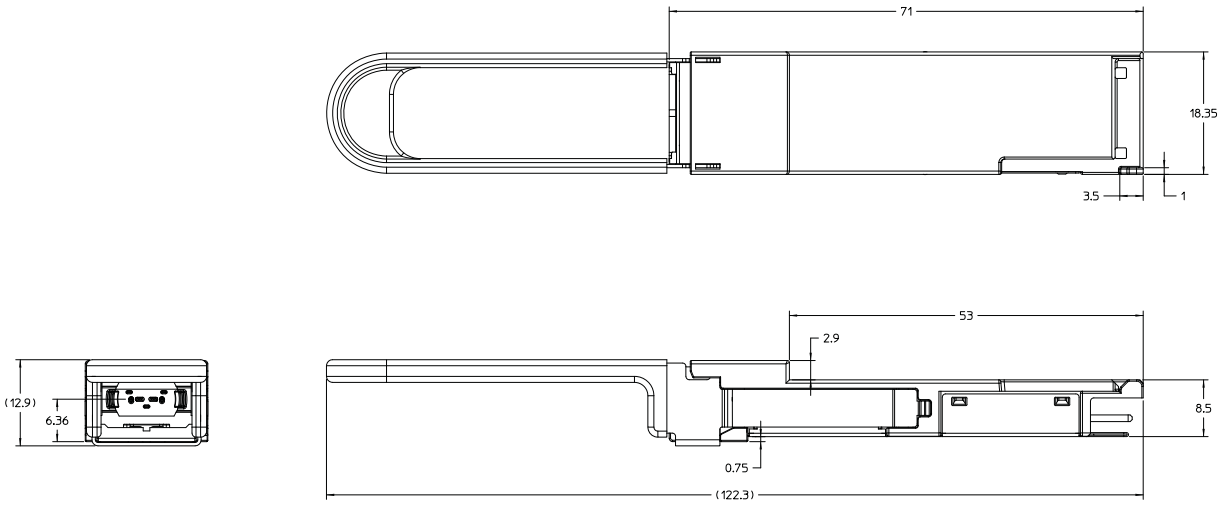


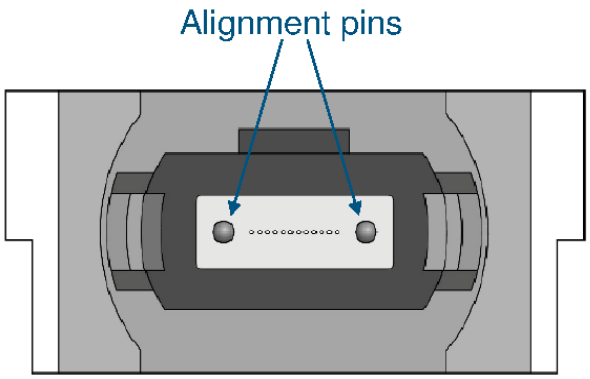
Figure 11: TWS Interface Bus Timing

Package Outline



Per SFF-8679, the pull-tab is color coded as Beige for 850nm optical devices

Figure 12: Mechanical Package Outline (All dimensions in mm)



Transmit Channels: 1 2 3 4
Unused positions: x x x x
Receive Channels: 4 3 2 1

The optical interface port is a male MPO connector as specified in IEC 61754-7. Aligned key MTP/MPO patch cords should be used to ensure alignment of the signals between the modules. The aligned key patch cord is defined in TIA-568.

Figure 13: Module Optical Interface (looking into the optical port)

Control Interface & Memory Map

The control interface combines dedicated signal lines for ModSelL, LP Mode, ResetL, ModPrsL, IntL with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. It is scaled for 3.3 volt LVTTL. Outputs are high-Z in the high state to support busing of these signals. Signal and timing characteristics are further defined in the Control I/O Characteristics section. For more details, see QSFP28 SFF-8436.

ModSelL

The ModSelL is an input signal. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node is biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP28 modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal is pulled up to Vcc in the QSFP28 module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode

Low power mode. LPMode is pulled up to Vcc in the QSFP28 module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host controls how much power a module can dissipate.

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL

IntL is an output signal. When "Low", indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is an open collector output and must be pulled to host supply voltage on the host board.

The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

The user can read the present value of the various diagnostic monitors. Case module temperature, supply voltage, laser bias current for each channel and receiver input power (Pave) for each channel are reported. All monitor items are two-byte fields and to maintain coherency, the host must access these with single two-byte read sequences. For each monitored item, alarm and warning thresholds are established. If an item moves past a threshold, a flag is set, and, provided the item is not masked, IntL is asserted. A mask bit that can be set to prevent assertion of IntL for the individual item exists for every LOS, Tx fault and monitor flag. Entries in the mask fields are volatile.

Soft Status and Control

A number of soft status signals and controls are available in the AFBR-89CDDZ transceiver memory and accessible through the TWS interface. Some soft status signals include receiver LOS, transmitter LOS, and diagnostic monitor alarms and warnings. Some soft controls include transmitter disable (Tx_Dis), receiver output disable (Rx_Dis), transmitter squelch disable (Tx_SqDis), receiver squelch disable (Rx_SqDis), and masking of status signal in triggering IntL. All soft status signals and controls are per channel basis. All soft control entries are volatile.

Transmitter LOS

The transmitter LOS status signal is on page 0 address 3 bits 4-7 for channels 1-4 respectively. Transmitter LOS is based on input differential voltage. This status register is latched and it is cleared on read.

Receiver LOS

The receiver LOS status signal is on page 0 address 3 bits 0-3 for channels 1-4 respectively. Receiver LOS is based on input optical modulation amplitude (OMA). This status register is latched and it is cleared on read.

Transmitter LOL

The transmitter loss of lock status signal is on page 0 address 5 bits 4-7 for channels 1-4 respectively. The loss of lock flag will assert if an enabled Tx-side CDR is not locked to the input data signal. This status register is latched and it is cleared on read.

Receiver LOL

The receiver loss of lock status signal is on page 0 address 5 bits 0-3 for channels 1-4 respectively. The loss of lock flag will assert if an enabled Rx-side CDR is not locked to the input data signal. This status register is latched and it is cleared on read.

Transmitter Fault

The transmitter fault status signal is on page 0 address 4 bits 0-3 for channels 1-4 respectively. The transmitter fault condition will flag if the laser output power is too high – i.e. approaching eye safety levels. When fault is triggered, the corresponding transmitter channel output will be disabled. Module reset or toggling of soft transmitter disable (Address 86 decimal) can restore the transmitter channel function unless fault condition persists. This status register is latched and it is cleared on read.

Transmitter Disable

The transmitter disable control is on page 0 address 86 bits 0-3 for channels 1-4 respectively. When the Tx is disabled the transmitter power shall be less than -30 dBm.

Receiver Disable

The receiver disable control is on page 3 address 241 bits 4-7 for channels 1-4 respectively. If the receiver output is disabled, the output differential voltage swing shall be less than 50 mVpp.

Transmitter Squelch Disable

The transmitter squelch disable control is on page 3 address 240 bits 0-3 for channels 1-4 respectively. AFBR-89CDDZ transceivers have transmitter output squelch function enabled as default. If the transmitter output is in the Squelched state, the laser output power will be turned off.

Receiver Squelch Disable

The receiver squelch disable control is on page 3 address 240 bits 4-7 for channels 1-4 respectively. AFBR-89CDDZ transceivers have receiver output squelch function enabled as default. If the receiver output is in the Squelched state, the output differential voltage swing shall be less than 50 mVpp.

Module Start-Up Behavior

Default Host Conditions:

The host system should ensure the following default conditions are present at an empty QSFP28 connector. This ensures the transceiver will see a known state for power up and initialization.

IntL (pin 28) Pulled high by host via resistor.

ModPrsL (pin 27) Pulled high by host via resistor.

ResetL (pin 9) = Tri-state on host (or pulled high by GPIO)

LPMode (pin 31) = Tri-state on host (or pulled high by GPIO)

ModSelL (pin 8) = Tri-state on host (or pulled high by GPIO)

Module Insertion (Hot Plug) or Power On (Cold Start):

Upon insertion of a QSFP28 transceiver (or upon power up of a pre-installed transceiver), the QSFP28 will immediately result in the following conditions at the connector.

ModPrsL (pin 27) Pulled low internally by QSFP28 (internally grounded)

ResetL (pin 9) Pulled high internally by QSFP28 (default to Normal Operation Enabled)

LPMode (pin 31) Pulled high internally by QSFP28 (default to Low Power Mode Enabled)

Host Reads Transceiver Vitals and Enables Operation

When QSFP28 powers up and initializes, the host should use the following to enable normal operation. AFBR-89CDDZ requires more than 1.5W to operate, requiring LPMode management to enable.

ModSelL (pin 8) pulled low by host GPIO to enable QSFP28 Two-Wire Serial (TWS) communication.

IntL (pin 28) will be pulled low by the QSFP28 after initialization (alarming).

Host reads TWS Page 00h 128-255. Check Power Class requirements and confirm compatibility.

Host clears LPMode – pull pin 31 low with GPIO, or use TWS Page 00h Address 93 bits 0-1

Host reads TWS Page 00h Address 2 bit 0 (Data_Not_Ready Flag)

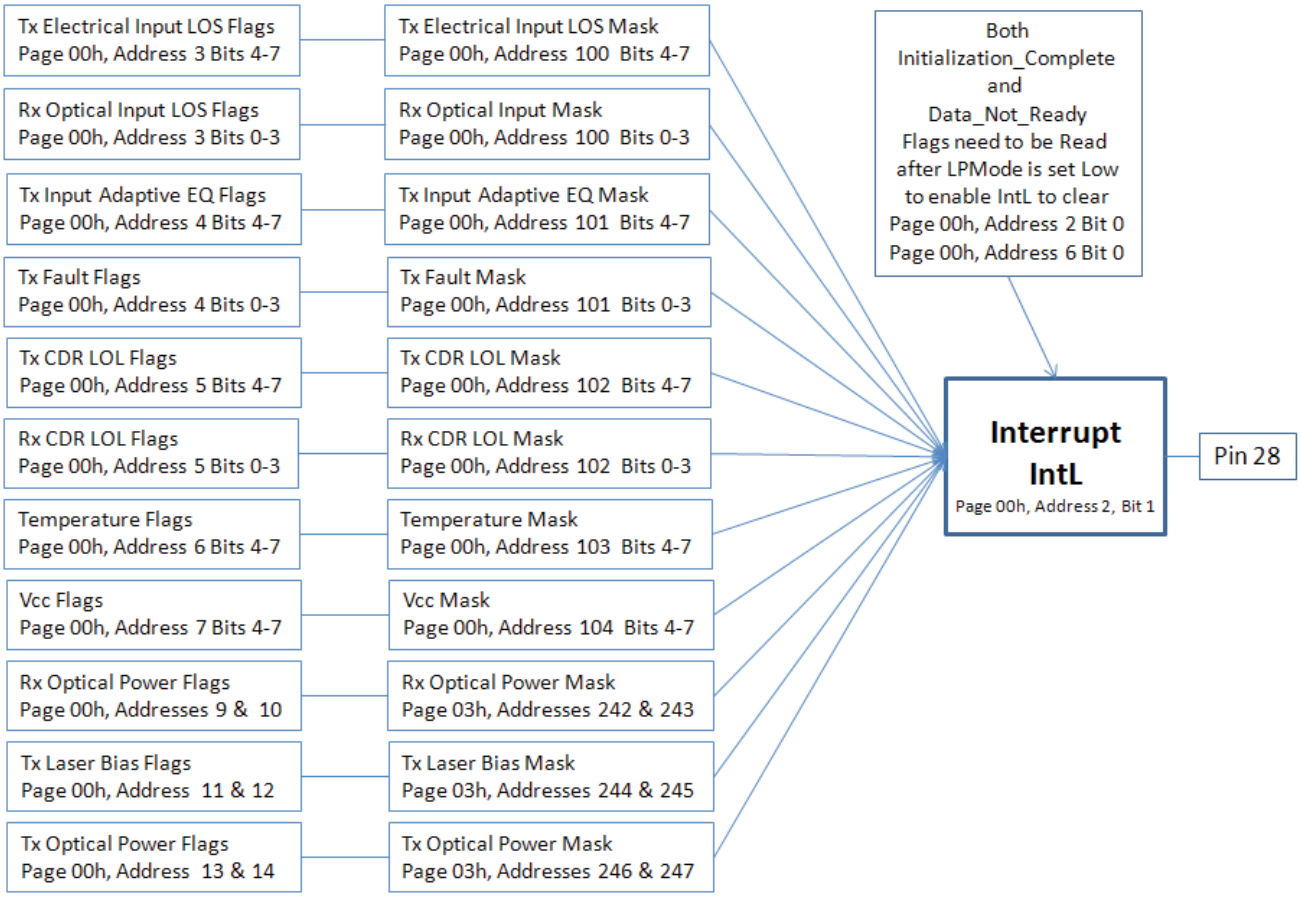
Host reads TWS Page 00h Address 6 bit 0 (Initialization Complete Flag)

IntL (pin 28) is allowed high by QSFP28 after LPMode released and Flag Bits read.

Diagnostics can now be polled. Control/Status registers are now active.

If IntL (pin 28) alarms again (i.e. pulled low by QSFP28), flags and masks are now active.

Flags, Masks, and Interrupt Condition



I/O Timing for Control and Status Functions

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Per SFF-8679.

Parameter	Symbol	Min	Max	Units	Reference
Initialization Time	t_init		2000	ms	Time from power on, hot plug or rising edge of Reset until the module is fully functional. This time does not apply to non Power level 1 modules in the Low Power state
Reset Init Assert Time	t_reset_init		2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on ResetL
Serial Bus Hardware Ready Time	t_serial		2000	ms	Time from power on until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data		2000	ms	Time from power on to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset		2000	ms	Time from rising edge on the ResetL pin until the module is fully functional
LPMode Assert Time	ton_LPMode		100	µs	Time from assertion of LPMode until the module power consumption enters power level 1
LPMode De-Assert Time	toff_LPMode		300	ms	Time from deassertion of LPMode until module is fully functional.
Interrupt Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
Interrupt De-assert Time	Toff_IntL		500	µs	Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for RX LOS, TX Fault and other flag bits
RX LOS Assert Time	ton_los		100	ms	Time from RX LOS state to RX LOS bit set and IntL asserted
TX Fault Assert Time	ton_Txfault		200	ms	Time from TX Fault state to TX fault bit set and IntL asserted
Flag Assert Time	ton_Flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted.
Mask Assert Time	ton_Mask		100	ms	Time from mask bit set until associated IntL assertion is inhibited
Mask Deassert Time	toff_Mask		100	ms	Time from mask bit cleared until associated IntL operation resumes
Power_override or Power_set					
Assert Time	ton_Pdown		100	ms	Time from P_Down bit set (value =1b) until module power consumption reaches Power Level 1
Power_override or Power_set					
Deassert Time	toff_Pdown		300	ms	Time from P_Down bit cleared (value = 0b) until module is fully functional.
RX Squelch Assert Time	ton_Rxsq		80	µs	Time from loss of RX input signal until the squelched output condition is reached
RX Squelch Deassert Time	toff_Rxsq		80	µs	Time from resumption of RX input signals until normal RX output condition is reached
TX Squelch Assert Time	ton_Txsq		400	ms	Time from loss of TX input signal until the squelched output condition is reached
TX Squelch Deassert Time	toff_Txsq		400	ms	Time from resumption of TX input signals until nominal TX output condition is reached
TX Disable Assert Time	ton_txdis		100	ms	Time from TX Disable bit set until optical output falls below 10% of nominal

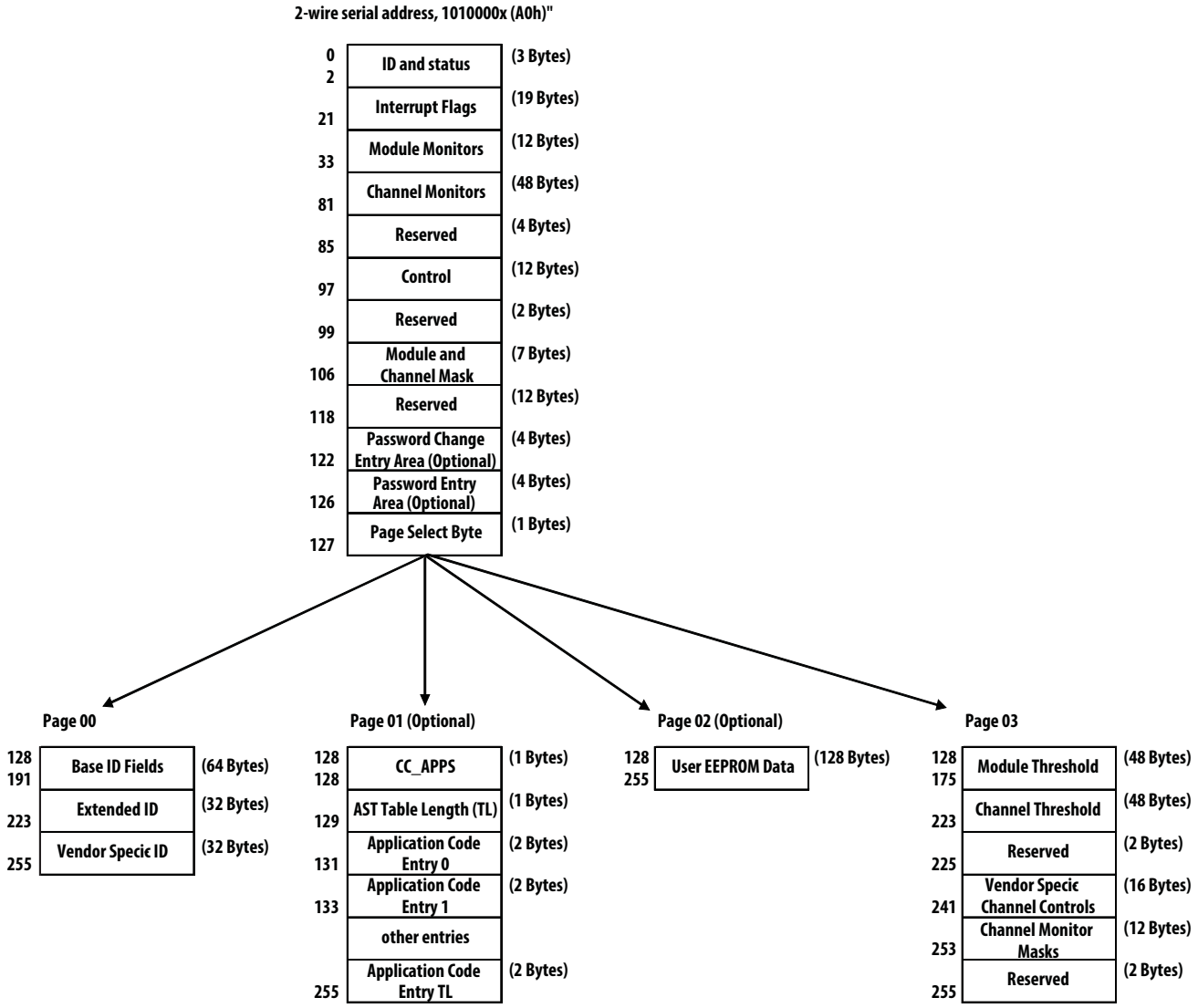
Parameter	Symbol	Min	Max	Units	Reference
TX Disable Deassert Time	toff_txdis		400	ms	Time from TX Disable bit cleared until optical output rises above 90% of nominal
RX Output Disable Assert Time	ton_rxdis		100	ms	Time from RX Output Disable bit set until RX output falls below 10% of nominal
RX Output Disable Deassert Time	toff_rxdis		100	ms	Time from RX Output Disable bit cleared until RX output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis		100	ms	This applies to RX and TX Squelch and is the time from bit set until squelch functionality is disabled
Squelch Disable Deassert Time	toff_sqdis		100	ms	This applies to RX and TX Squelch and is the time from bit cleared until squelch functionality enabled

Low Speed Pin Electrical Specifications

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA
	VOH	Vcc –0.5	Vcc + 0.3	V	
SCL and SDA	VIL	-0.3	Vcc × 0.3	V	
	VIH	Vcc × 0.7	Vcc + 0.5	V	
LPMode, ResetL and ModSelL	VIL	-0.3	0.8	V	|Iin|<=125 µA for 0V<Vin,Vcc
	VIH	2	Vcc + 0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	Vcc – 0.5	Vcc + 0.3	V	
Two Wire Serial (TWS) Interface Clock Rate			400	kHz	

Memory Map

The memory is structured as a single address, multiple page approach. The 7 bit device address on the two wire interface is 1010000b. The structure of the memory is shown below. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. For a more detailed description of the QSFP28 memory map see the QSFP28 SFF-8636 Specification.



Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Lower Page 00h	0	0h	7-0	Identifier (11h = QSFP28 Device) Per SFF-8024 Table 4-1	Read Only	11h
	1	1h	7-0	Revision Compliance (00h = Revision not specified). Code for SFF-8636 rev 2.5 or Higher.	Read Only	00h
	2	2h	7-3	Reserved	Read Only	00h
			2	Flat_mem: 0=Paging, 1=Flat	Read Only	
			1	IntL – Digital state of Interrupt Flag	Read Only	
			0	Data_Not_Ready 0= Ready, 1= Not Flag Indicates module has not yet achieved power up and monitor data is not ready. Bit remains high until data is ready to be read at which time the module sets the bit low.	Read Only	
	3	3h	7	Channel 4 Latched Tx LOS Flag	Read Only	00h
			6	Channel 3 Latched Tx LOS Flag		
			5	Channel 2 Latched Tx LOS Flag		
			4	Channel 1 Latched Tx LOS Flag		
			3	Channel 4 Latched Rx LOS Flag	Read Only	
			2	Channel 3 Latched Rx LOS Flag		
			1	Channel 2 Latched Rx LOS Flag		
			0	Channel 1 Latched Rx LOS Flag		
	4	4h	7	Channel 4 Latched TX, Adaptive EQ fault indicator [not used]	Read Only	00h
			6	Channel 3 Latched TX, Adaptive EQ fault indicator [not used]		
			5	Channel 2 Latched TX, Adaptive EQ fault indicator [not used]		
			4	Channel 1 Latched TX, Adaptive EQ fault indicator [not used]		
			3	Channel 4 Latched Tx Fault Flag	Read Only	
			2	Channel 3 Latched Tx Fault Flag		
			1	Channel 2 Latched Tx Fault Flag		
			0	Channel 1 Latched Tx Fault Flag		
	5	5h	7	Channel 4 Tx CDR Loss of Lock Flag	Read Only	00h
			6	Channel 3 Tx CDR Loss of Lock Flag		
			5	Channel 2 Tx CDR Loss of Lock Flag		
			4	Channel 1 Tx CDR Loss of Lock Flag		
			3	Channel 4 Rx CDR Loss of Lock Flag	Read Only	
			2	Channel 3 Rx CDR Loss of Lock Flag		
			1	Channel 2 Rx CDR Loss of Lock Flag		
			0	Channel 1 Rx CDR Loss of Lock Flag		
	6	6h	7	Latched High Temperature Alarm Flag	Read Only	00h
			6	Latched Low Temperature Alarm Flag		
			5	Latched High Temperature Warning Flag		
			4	Latched Low Temperature Warning Flag		
			3-1	Reserved	Read Only	
			0	Initialization/Reset Complete Flag Asserted (one) after initialization and/or reset has completed. Returns to Zero when read	Read Only Clear on Read	

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Lower Page 00h	7	7h	7	Latched High Supply Voltage Alarm Flag	Read Only	00h
			6	Latched Low Supply Voltage Alarm Flag		
			5	Latched High Supply Voltage Warn Flag		
			4	Latched Low Supply Voltage Warn Flag		
			3-0	Reserved	Read Only	
	8	8h	7-0	Vendor Specific	Read Only	00h
	9	9h	7	Chan 1 Latched High Rx PWR Alarm Flag	Read Only	00h
			6	Chan 1 Latched Low Rx PWR Alarm Flag		
			5	Chan 1 Latched High Rx PWR Warn Flag		
			4	Chan 1 Latched Low Rx PWR Warn Flag		
			3	Chan 2 Latched High Rx PWR Alarm Flag	Read Only	
			2	Chan 2 Latched Low Rx PWR Alarm Flag		
			1	Chan 2 Latched High Rx PWR Warn Flag		
			0	Chan 2 Latched Low Rx PWR Warn Flag		
	10	Ah	7	Chan 3 Latched High Rx PWR Alarm Flag	Read Only	00h
			6	Chan 3 Latched Low Rx PWR Alarm Flag		
			5	Chan 3 Latched High Rx PWR Warn Flag		
			4	Chan 3 Latched Low Rx PWR Warn Flag		
			3	Chan 4 Latched High Rx PWR Alarm Flag	Read Only	
			2	Chan 4 Latched Low Rx PWR Alarm Flag		
			1	Chan 4 Latched High Rx PWR Warn Flag		
			0	Chan 4 Latched Low Rx PWR Warn Flag		
	11	Bh	7	Chan 1 Latched High Tx Bias Alarm Flag	Read Only	00h
			6	Chan 1 Latched Low Tx Bias Alarm Flag		
			5	Chan 1 Latched High Tx Bias Warn Flag		
			4	Chan 1 Latched Low Tx Bias Warn Flag		
			3	Chan 2 Latched High Tx Bias Alarm Flag	Read Only	
			2	Chan 2 Latched Low Tx Bias Alarm Flag		
			1	Chan 2 Latched High Tx Bias Warn Flag		
			0	Chan 2 Latched Low Tx Bias Warn Flag		
	12	Ch	7	Chan 3 Latched High Tx Bias Alarm Flag	Read Only	00h
			6	Chan 3 Latched Low Tx Bias Alarm Flag		
			5	Chan 3 Latched High Tx Bias Warn Flag		
			4	Chan 3 Latched Low Tx Bias Warn Flag		
			3	Chan 4 Latched High Tx Bias Alarm Flag	Read Only	
			2	Chan 4 Latched Low Tx Bias Alarm Flag		
			1	Chan 4 Latched High Tx Bias Warn Flag		
			0	Chan 4 Latched Low Tx Bias Warn Flag		

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Lower Page 00h	13	Dh	7	Chan 1 Latched High Tx PWR Alarm Flag	Read Only	00h
			6	Chan 1 Latched Low Tx PWR Alarm Flag		
			5	Chan 1 Latched High Tx PWR Warn Flag		
			4	Chan 1 Latched Low Tx PWR Warn Flag		
			3	Chan 2 Latched High Tx PWR Alarm Flag	Read Only	
			2	Chan 2 Latched Low Tx PWR Alarm Flag		
			1	Chan 2 Latched High Tx PWR Warn Flag		
			0	Chan 2 Latched Low Tx PWR Warn Flag		
	14	Eh	7	Chan 3 Latched High Tx PWR Alarm Flag	Read Only	00h
			6	Chan 3 Latched Low Tx PWR Alarm Flag		
			5	Chan 3 Latched High Tx PWR Warn Flag		
			4	Chan 3 Latched Low Tx PWR Warn Flag		
			3	Chan 4 Latched High Tx PWR Alarm Flag	Read Only	
			2	Chan 4 Latched Low Tx PWR Alarm Flag		
			1	Chan 4 Latched High Tx PWR Warn Flag		
			0	Chan 4 Latched Low Tx PWR Warn Flag		
	15-16	Fh-10h	7-0	Reserved	Read Only	00h
	17-18	11h-12h	7-0	Reserved	Read Only	00h
	19-21	13h-15h	7-0	Vendor Specific	Read Only	00h
	22	16h	7-0	Temperature Diagnostic Monitor MSB Temperature accuracy is ±3C over the recommended operating conditions. Corresponds to the case temperature thermal control location.	Read Only	N/A
	23	17h	7-0	Temperature Diagnostic Monitor LSB		
	24-25	18h-19h	7-0	Reserved	Read Only	00h
	26	1Ah	7-0	Supply Voltage Diagnostic Monitor MSB Supply voltage accuracy is ±3% over the recommended operating conditions.	Read Only	N/A
	27	1Bh	7-0	Supply Voltage Diagnostic Monitor LSB		
	28-29	1Ch-1Dh	7-0	Reserved	Read Only	00h
	30-33	1Eh-21h	7-0	Vendor Specific	Read Only	00h
	34	22h	7-0	Channel 1 Rx Optical Input Power MSB Rx optical power accuracy is ±3 dB over the recommended operating conditions.	Read Only	N/A
	35	23h	7-0	Channel 1 Rx Optical Input Power LSB		
	36	24h	7-0	Channel 2 Rx Optical Input Power MSB	Read Only	N/A
	37	25h	7-0	Channel 2 Rx Optical Input Power LSB		
	38	26h	7-0	Channel 3 Rx Optical Input Power MSB	Read Only	N/A
	39	27h	7-0	Channel 3 Rx Optical Input Power LSB		
	40	28h	7-0	Channel 4 Rx Optical Input Power MSB	Read Only	N/A
	41	29h	7-0	Channel 4 Rx Optical Input Power LSB		
	42	2Ah	7-0	Channel 1 Tx Bias Diagnostic MSB Tx Bias accuracy is ±10% over the recommended operating conditions.	Read Only	N/A
	43	2Bh	7-0	Channel 1 Tx Bias Diagnostic LSB		

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Lower Page 00h	44	2Ch	7-0	Channel 2 Tx Bias Diagnostic MSB	Read Only	N/A
	45	2Dh	7-0	Channel 2 Tx Bias Diagnostic LSB		
	46	2Eh	7-0	Channel 3 Tx Bias Diagnostic MSB	Read Only	N/A
	47	2Fh	7-0	Channel 3 Tx Bias Diagnostic LSB		
	48	30h	7-0	Channel 4 Tx Bias Diagnostic MSB	Read Only	n/a
	49	31h	7-0	Channel 4 Tx Bias Diagnostic LSB		
	50	32h	7-0	Channel 1 Tx Optical Output Power MSB Tx optical power accuracy is ±3 dB over the recommended operating conditions.	Read Only	N/A
	51	33h	7-0	Channel 1 Tx Optical Output Power LSB		
	52	34h	7-0	Channel 2 Tx Optical Output Power MSB	Read Only	N/A
	53	35h	7-0	Channel 2 Tx Optical Output Power LSB		
	54	36h	7-0	Channel 3 Tx Optical Output Power MSB	Read Only	N/A
	55	37h	7-0	Channel 3 Tx Optical Output Power LSB		
	56	38h	7-0	Channel 4 Tx Optical Output Power MSB	Read Only	N/A
	57	39h	7-0	Channel 4 Tx Optical Output Power LSB		
	58-65	3Ah-41h	7-0	Reserved	Read Only	00h
	66-81	42h-51h	7-0	Vendor Specific	Read Only	00h
	82-85	52h-55h	7-0	Reserved	Read Only	00h
	86	56h	7-4	Reserved	Read Write	00h
			3	Channel 4 TX Disable Control	Read Write	
			2	Channel 3 TX Disable Control		
			1	Channel 2 TX Disable Control		
			0	Channel 1 TX Disable Control		
	87	57h	7-6	Channel 4 RX Rate_Select Control	Read Write	00h
			5-4	Channel 3 RX Rate_Select Control		
			3-2	Channel 2 RX Rate_Select Control		
			1-0	Channel 1 RX Rate_Select Control		
	88	58h	7-6	Channel 4 TX Rate_Select Control	Read Write	00h
			5-4	Channel 3 TX Rate_Select Control		
			3-2	Channel 2 TX Rate_Select Control		
			1-0	Channel 1 TX Rate_Select Control		
	89	59h	7-0	Channel 4 RX Application Select Control	Read Write	00h
	90	5Ah	7-0	Channel 3 RX Application Select Control		00h
	91	5Bh	7-0	Channel 2 RX Application Select Control		00h
	92	5Ch	7-0	Channel 1 RX Application Select Control		00h
	93	5Dh	7-3	Reserved	Read Write	00h
			2	High Power Class Enable (Class 5-7)	Read Write	
			1	Power Set (Low Power Mode)	Read Write	
			0	Override Low Power Mode Control	Read Write	
	94	5Eh	7-0	Channel 4 TX Application Select Control	Read Write	00h
	95	5Fh	7-0	Channel 3 TX Application Select Control		00h
	96	60h	7-0	Channel 2 TX Application Select Control		00h

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Lower Page 00h	97	61h	7-0	Channel 1 TX Application Select Control		00h
	98	62h	7	Channel 4 TX CDR Control (1b = on)	Read Write	FFh
			6	Channel 3 TX CDR Control (1b = on)		
			5	Channel 2 TX CDR Control (1b = on)		
			4	Channel 1 TX CDR Control (1b = on)		
			3	Channel 4 RX CDR Control (1b = on)	Read Write	
			2	Channel 3 RX CDR Control (1b = on)		
			1	Channel 2 RX CDR Control (1b = on)		
			0	Channel 1 RX CDR Control (1b = on)		
	99	63h	7-0	Reserved	Read Only	00h
	100	64h	7	Channel 4 TX LOS Masking Bit to IntL	Read Write	00h
			6	Channel 3 TX LOS Masking Bit to IntL		
			5	Channel 2 TX LOS Masking Bit to IntL		
			4	Channel 1 TX LOS Masking Bit to IntL		
			3	Channel 4 RX LOS Masking Bit to IntL	Read Write	
			2	Channel 3 RX LOS Masking Bit to IntL		
			1	Channel 2 RX LOS Masking Bit to IntL		
			0	Channel 1 RX LOS Masking Bit to IntL		
	101	65h	7	Channel 4 Masking Bit for TX Adaptive EQ fault indicator to IntL [not used]	Read Write	00h
			6	Channel 3 Masking Bit for TX Adaptive EQ fault indicator to IntL [not used]		
			5	Channel 2 Masking Bit for TX Adaptive EQ fault indicator to IntL [not used]		
			4	Channel 1 Masking Bit for TX Adaptive EQ fault indicator to IntL [not used]		
			3	Channel 4 TX Fault Masking Bit to IntL	Read Write	
			2	Channel 3 TX Fault Masking Bit to IntL		
			1	Channel 2 TX Fault Masking Bit to IntL		
			0	Channel 1 TX Fault Masking Bit to IntL		
	102	66h	7	Channel 4 Tx CDR Loss of Lock Mask	Read Write	00h
			6	Channel 3 Tx CDR Loss of Lock Mask		
			5	Channel 2 Tx CDR Loss of Lock Mask		
			4	Channel 1 Tx CDR Loss of Lock Mask		
			3	Channel 4 Rx CDR Loss of Lock Mask	Read Write	
			2	Channel 3 Rx CDR Loss of Lock Mask		
			1	Channel 2 Rx CDR Loss of Lock Mask		
			0	Channel 1 Rx CDR Loss of Lock Mask		
	103	67h	7	High Temp Alarm Masking Bit to IntL	Read Write	00h
			6	Low Temp Alarm Masking Bit to IntL		
			5	High Temp Warning Masking Bit to IntL		
			4	Low Temp Warning Masking Bit to IntL		
			3-0	Reserved		

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Lower Page 00h	104	68h	7	High Vcc Alarm Masking Bit to IntL	Read Write	00h
			6	Low Vcc Alarm Masking Bit to IntL		
			5	High Vcc Warning Masking Bit to IntL		
			4	Low Vcc Warning Masking Bit to IntL		
			3-0	Reserved		
	105-106	69h-6Ah	7-0	Vendor Specific	Read Only	00h
	107	6Bh	7-0	Reserved	Read Only	00h
	108	6Ch	7-0	Propagation Delay MSB Not Applicable (Transceiver) leave as 00h	Read Only	00h
	109	6Dh	7-0	Propagation Delay LSB Not Applicable (Transceiver) leave as 00h	Read Only	00h
	110	6Eh	7-4	Advanced Low Power Mode 0000b (value of 0000 shall indicate that a power consumption limit below 1.5 W is not available)	Read Only	00h
			3	Far Side Managed Not Applicable (Transceiver) leave as 0b	Read Only	
			2-0	Min Operating Voltage 000b indicates the feature is disabled (not supported)	Read Only	
	111-112	6Fh-70h	7-0	Assigned for use by PCI Express (not used)	Read Only	00h
	113	71h	7	Reserved	Read Only	00h
			6-4	Far End Implementation. Coded as 000, Far end is unspecified.	Read Only	
			3-0	Near End Implementation. Coded as 0000, Channels 1-4 are implemented.	Read Only	
	114-118	72h-76h	7-0	Reserved	Read Only	00h
	119-122	77h-7Ah	7-0	Password Change Entry Area (4 Bytes)	Write Only	00h
	123-126	7Bh-7Eh	7-0	Password Entry Area (4- Bytes)	Write Only	00h
	127	7Fh	7-0	Page Select Byte	Read Write	00h

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Upper Page 00h	128	80h	7-0	Identifier (11h = QSFP28 Device) Per SFF-8024 Table 4-1	Read Only	11h
	129	81h	7-6	Power Class (11b = 3.5W max)	Read Only	CCh
			5	Reserved		
			4	CLEI Code. 0b = Not Present in Page 02h		
			3	TX CDR. 1b=CDR Present		
			2	Rx CDR. 1b=CDR Present		
			1-0	Higher Power Classes: (00b =Unused)		
	130	82h	7-0	Connector Value. (0Ch=MPO)	Read Only	0Ch
	131	83h	7-0	10G/40G Ethernet Compliance Codes	Read Only	80h
	132	84h	7-0	Sonet Compliance Codes	Read Only	00h
	133	85h	7-0	SATA/SAS Compliance Codes	Read Only	00h
	134	86h	7-0	1G Gigabit Ethernet Compliance Codes	Read Only	00h
	135-136	87h-88h	7-0	Fibre Channel Link / Transmitter Codes	Read Only	0000h
	137	89h	7-0	Fibre Channel Media Codes	Read Only	00h
	138	8Ah	7-0	Fibre Channel Speed Codes	Read Only	00h
	139	8Bh	7-0	Encoding Values.[05h – 64B/66B]	Read Only	05h
	140	8Ch	7-0	Bit Rate Nominal (Units of 100MBd)	Read Only	FFh
	141	8Dh	7-0	Extended Rate Select Compliance	Read Only	00h
	142	8Eh	7-0	SMF Link Length (1km per bit)	Read Only	00h
	143	8Fh	7-0	MMF OM3 Link Length (2m per bit) 70m	Read Only	23h
	144	90h	7-0	MMF OM2 Link Length (1m per bit)	Read Only	00h
	145	91h	7-0	MMF OM1 Link Length (1m per bit)	Read Only	00h
	146	92h	7-0	MMF OM4 Link Length (2m per bit) 100m	Read Only	32h
	147	93h	7-0	Device Technology. 850nm VCSEL+PIN	Read Only	00h
	148	94h	7-0	Vendor Name – ASCII "A"	Read Only	41h
	149	95h	7-0	Vendor Name – ASCII "V"		56h
	150	96h	7-0	Vendor Name – ASCII "A"		41h
	151	97h	7-0	Vendor Name – ASCII "G"		47h
	152	98h	7-0	Vendor Name – ASCII "O"		4Fh
	153	99h	7-0	Vendor Name – ASCII " "		20h
	154	9Ah	7-0	Vendor Name – ASCII " "		20h
	155	9Bh	7-0	Vendor Name – ASCII " "	Read Only	20h
	156	9Ch	7-0	Vendor Name – ASCII " "		20h
	157	9Dh	7-0	Vendor Name – ASCII " "		20h
	158	9Eh	7-0	Vendor Name – ASCII " "		20h
	159	9Fh	7-0	Vendor Name – ASCII " "		20h
	160	A0h	7-0	Vendor Name – ASCII " "		20h
	161	A1h	7-0	Vendor Name – ASCII " "		20h
	162	A2h	7-0	Vendor Name – ASCII " "		20h
	163	A3h	7-0	Vendor Name – ASCII " "		20h
	164	A4h	7-0	InfiniBand Compliance Codes	Read Only	00h
	165	A5h	7-0	Vendor OUI	Read Only	00h

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Upper Page 00h	166	A6h	7-0	Vendor OUI		17h
	167	A7h	7-0	Vendor OUI		6Ah
	168	A8h	7-0	Vendor Part Number – ASCII "A"	Read Only	41h
	169	A9h	7-0	Vendor Part Number – ASCII "F"		46h
	170	AAh	7-0	Vendor Part Number – ASCII "B"		42h
	171	ABh	7-0	Vendor Part Number – ASCII "R"		52h
	172	ACh	7-0	Vendor Part Number – ASCII "-"		2Dh
	173	ADh	7-0	Vendor Part Number – ASCII "8"		38h
	174	AEh	7-0	Vendor Part Number – ASCII "9"		39h
	175	AFh	7-0	Vendor Part Number – ASCII "C"		43h
	176	B0h	7-0	Vendor Part Number – ASCII "D"		44h
	177	B1h	7-0	Vendor Part Number – ASCII "D"		44h
	178	B2h	7-0	Vendor Part Number – ASCII "Z"		5Ah
	179	B3h	7-0	Vendor Part Number – ASCII " "		20h
	180	B4h	7-0	Vendor Part Number – ASCII " "		20h
	181	B5h	7-0	Vendor Part Number – ASCII " "		20h
	182	B6h	7-0	Vendor Part Number – ASCII " "		20h
	183	B7h	7-0	Vendor Part Number – ASCII " "		20h
	184	B8h	7-0	Vendor Part Revision – ASCII " "	Read Only	30h
	185	B9h	7-0	Vendor Part Revision – ASCII " "		31h
	186-187	BAh-BBh	7-0	Wavelength (units of 0.05nm) = 850nm	Read Only	4268h
	188-189	BCh-BDh	7-0	Wavelength Tolerance (units of 0.005nm)	Read Only	07D0h
	190	BEh	7-0	Maximum Temperature (00h= 70C)	Read Only	00h
	191	BFh	7-0	Checksum (Page00h Bytes 128-190)	Read Only	
	192	C0h	7-0	Extended Ethernet Compliance Codes (See SFF-8024 Table 4-4)	Read Only	02h
	193	C1h	7-4	Reserved	Read Only	07h
			3	Adaptive Tx EQ Capable (0b=No)		
			2	Variable Tx EQ Capable (1b=Yes)		
			1	Variable Rx Emphasis Capable (1b=Yes)		
			0	Variable Rx Amplitude Capable (1b=Yes)		
	194	C2h	7	Tx CDR Bypass Present (1b=Yes)	Read Only	FFh
			6	Rx CDR Bypass Present (1b=Yes)		
			5	Tx CDR LOL Flag Present (1b=Yes)		
			4	Rx CDR LOL Flag Present (1b=Yes)		
			3	Rx Squelch Disable Capable (1b=Yes)		
			2	Rx Out Disable Capable (1b=Yes)		
			1	Tx Squelch Disable Capable (1b=Yes)		
			0	Tx Squelch Implemented (1=Yes)		

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Upper Page 00h	195	C3h	7	Upper Memory Page 02 Present (1=Yes)	Read Only	DEh
			6	Upper Memory Page 01 Present (1=Yes)		
			5	Rate_Select Capable (0=No)		
			4	Tx_Disable Capable (1=Yes)		
			3	Tx_Fault Capable (1=Yes)		
			2	Tx Squelch Power Type (0=OMA, 1=Avg)		
			1	Tx_LOS Capable (1=Yes)		
			0	Reserved		
	196	C4h	7-0	Vendor Serial Number – ASCII " "	Read Only	
	197	C5h	7-0	Vendor Serial Number – ASCII " "		
	198	C6h	7-0	Vendor Serial Number – ASCII " "		
	199	C7h	7-0	Vendor Serial Number – ASCII " "		
	200	C8h	7-0	Vendor Serial Number – ASCII " "		
	201	C9h	7-0	Vendor Serial Number – ASCII " "		
	202	CAh	7-0	Vendor Serial Number – ASCII " "		
	203	CBh	7-0	Vendor Serial Number – ASCII " "		
	204	CCh	7-0	Vendor Serial Number – ASCII " "		
	205	CDh	7-0	Vendor Serial Number – ASCII " "		
	206	CEh	7-0	Vendor Serial Number – ASCII " "		
	207	CFh	7-0	Vendor Serial Number – ASCII " "		
	208	D0h	7-0	Vendor Serial Number – ASCII " "		
	209	D1h	7-0	Vendor Serial Number – ASCII " "		
	210	D2h	7-0	Vendor Serial Number – ASCII " "		
	211	D3h	7-0	Vendor Serial Number – ASCII " "		
	212	D4h	7-0	Vendor Date Code YY – ASCII " "		
	213	D5h	7-0	Vendor Date Code YY– ASCII " "		
	214	D6h	7-0	Vendor Date Code MM– ASCII " "		
	215	D7h	7-0	Vendor Date Code MM– ASCII " "		
	216	D8h	7-0	Vendor Date Code DD– ASCII " "		
	217	D9h	7-0	Vendor Date Code DD– ASCII " "		
	218	DAh	7-0	Vendor Date Code – ASCII " "		
	219	DBh	7-0	Vendor Date Code – ASCII " "		
	220	DCh	7-4	Reserved	Read Only	0Ch
			3	Rx Power DMI Type (1b=AVG)		
			2	Tx Avg Power DMI (1b=supported)		
			1-0	Reserved		

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Upper Page 00h	221	DDh	7-5	Reserved	Read Only	00h
			4	Initialization Complete Flag implemented. This flag was introduced in rev 2.5. When this bit is 1, the initialization complete flag at byte 6, bit 0 is implemented independent of t_init. When this bit is 0, the initialization complete flag is either not implemented or if implemented has a response time less than t_init, max as specified for the module.		
			3	Rate_Select Declaration		
			2	Application_Select Declaration		
			1-0	Reserved		
	222	DEh	7-0	Bit Rate Nominal (units of 250MBd)	Read Only	67h
	223	DFh	7-0	Checksum (Page00h Bytes 192-222)	Read Only	
	224-255	E0h-FFh	7-0	Vendor Specific EEPROM	Read Only	00h

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Upper Page 01h	128	80h	7-0	Checksum (Page01h Bytes 129-255)	Read Only	00h
	129	81h	7-6	Reserved	Read Only	00h
			5-0	Application Select Table Length (Entries)		
	130-255	82h-FFh	7-0	Application Code Definitions	Read Only	00h

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Upper Page 02h	128-255	80h-FFh	7-0	Optional User Writable EE-PROM	Read, Write, non-volatile Write with Pass-word	00h

The User can read the Upper Page 2 "User scratchpad" without a password and can write to this Upper Page 2 User scratchpad without inputting the Host password. However, inputs will be volatile and will return to the default state values upon Module Reset / Power cycle.

If the User inputs the Host password (Lower Page 0), this allows the user to make non-volatile writes to this Upper Page 2 User Scratch pad. The SFF-8636 defines the initial password as 00001011h. Inputted into Lower Pg 0 Registers 123-126 (7Bh-7Eh) 4-Byte Password Entry Area.

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Upper Page 03h	128-129	80h-81h	7-0	Temperature High Alarm Threshold 4B00h = 75 °C	Read Only	4800h
	130-131	82h-83h	7-0	Temperature Low Alarm Threshold FB00h = -5 °C		FB00h
	132-133	84h-85h	7-0	Temperature High Warning Threshold 4600h = 70 °C		4600h
	134-135	86h-87h	7-0	Temperature Low Warning Threshold 0000h = 0 °C		0000h
	136-143	88h-8Fh	7-0	Reserved	Read Only	00h
	144-145	90h-91h	7-0	Vcc High Alarm Threshold 8DCCh = 3.63V	Read Only	8DCCh
	146-147	92h-93h	7-0	Vcc Low Alarm Threshold 7404h = 2.97V		7404h
	148-149	94h-95h	7-0	Vcc High Warning Threshold 875Ah = 3.465V		875Ah
	150-151	96h-97h	7-0	Vcc Low Warning Threshold 7A76h = 3.135V		7A76h
	152-159	98h-9Fh	7-0	Reserved	Read Only	00h
	160-175	A0h-AFh	7-0	Vendor Specific	Read Only	00h
	176-177	B0h-B1h	7-0	Rx Power High Alarm Threshold 5576h = 3.4dBm	Read Only	5576h
	178-179	B2h-B3h	7-0	Rx Power Low Alarm Threshold 025Bh = -12.2 dBm		025Bh
	180-181	B4h-B5h	7-0	Rx Power High Warning Threshold 43E2h = 2.4 dBm		43E2h
	182-183	B6h-B7h	7-0	Rx Power Low Warning Threshold 02F7h = -11.2 dBm		02F7h
	184-185	B8h-B9h	7-0	Tx Bias High Alarm Threshold 1388h = 10 mA	Read Only	1388h
	186-187	BAh-BBh	7-0	Tx Bias Low Alarm Threshold 03E8h = 2 mA		03E8h
	188-189	BCh-BDh	7-0	Tx Bias High Warning Threshold 109Ah = 8.5 mA		109Ah
	190-191	BEh-BFh	7-0	Tx Bias Low Warning Threshold 05DCh = 3 mA		05DCh
	192-193	C0h-C1h	7-0	Tx PWR High Alarm Threshold 8772h = 5.4 dBm	Read Only	8772h
	194-195	C2h-C3h	7-0	Tx PWR Low Alarm Threshold 01EAh = -13.1 dBm		01EAh
	196-197	C4h-C5h	7-0	Tx PWR High Warning Threshold 43E2h = 2.4 dBm		43E2h
	198-199	C6h-C7h	7-0	Tx PWR Low Warning Threshold 04CEh = -9.1 dBm		04CEh
	200-207	C8h-CFh	7-0	Reserved for Channel Set 4 Thresholds	Read Only	00h
	208-223	D0h-DFh	7-0	Vendor Specific Thresholds	Read Only	00h
	224	E0h	7-4	Tx EQ Maximum Capability	Read Only	A7h
			3-0	Rx EMPHASIS Maximum Capability		

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Upper Page 03h	225	E1h	7-6	7:4 Reserved	Read Only	0Fh
			5-4	Rx output emphasis type. Code as 00 for Peak-to-peak amplitude stays constant, or not implemented.		
			3	RX output amplitude support. Amplitude code 0011 supported (see Table 6-32 SFF-8636)		
			2	RX output amplitude support Amplitude code 0010 supported (see Table 6-32 SFF-8636)		
			1	RX output amplitude support Amplitude code 0001 supported (see Table 6-32 SFF-8636)		
			0	RX output amplitude support Amplitude code 0000 supported (see Table 6-32 SFF-8636)		
	226-233	E2h-E9h	7-0	Vendor Specific Channel Controls	Read Only	00h
	234	EAh	7-4	Channel 1 Tx Input EQ Control	Read Write	66h
			3-0	Channel 2 Tx Input EQ Control		
	235	EBh	7-4	Channel 3 Tx Input EQ Control	Read Write	66h
			3-0	Channel 4 Tx Input EQ Control		
	236	ECh	7-4	Channel 1 Rx Output Emphasis Control	Read Write	11h
			3-0	Channel 2 Rx Output Emphasis Control		
	237	EDh	7-4	Channel 3 Rx Output Emphasis Control	Read Write	11h
			3-0	Channel 4 Rx Output Emphasis Control		
	238	EEh	7-4	Channel 1 Rx Amplitude Control	Read Write	33h
			3-0	Channel 2 Rx Amplitude Control		
	239	EFh	7-4	Channel 3 Rx Amplitude Control	Read Write	33h
			3-0	Channel 4 Rx Amplitude Control		
	240	F0h	7	Channel 4 Rx Squelch Disable Control	Read Write	00h
			6	Channel 3 Rx Squelch Disable Control		
			5	Channel 2 Rx Squelch Disable Control		
			4	Channel 1 Rx Squelch Disable Control		
			3	Channel 4 Tx Squelch Disable Control	Read Write	
			2	Channel 3 Tx Squelch Disable Control		
			1	Channel 2 Tx Squelch Disable Control		
			0	Channel 1 Tx Squelch Disable Control		
	241	F1h	7	Channel 4 Rx Output Disable Control	Read Write	00h
			6	Channel 3 Rx Output Disable Control		
			5	Channel 2 Rx Output Disable Control		
			4	Channel 1 Rx Output Disable Control		
			3	Channel 4Tx Adaptive EQ Control [not used]	Read Write	
			2	Channel 3Tx Adaptive EQ Control [not used]		
			1	Channel 2Tx Adaptive EQ Control [not used]		
			0	Channel 1Tx Adaptive EQ Control [not used]		

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Upper Page 03h	242	F2h	7	Channel 1 Rx Power High Alarm Mask	Read Write	00h
			6	Channel 1 Rx Power Low Alarm Mask		
			5	Channel 1 Rx Power High Warning Mask		
			4	Channel 1 Rx Power Low Warning Mask		
			3	Channel 2 Rx Power High Alarm Mask		
			2	Channel 2 Rx Power Low Alarm Mask		
			1	Channel 2 Rx Power High Warning Mask		
			0	Channel 2 Rx Power Low Warning Mask		
	243	F3h	7	Channel 3 Rx Power High Alarm Mask	Read Write	00h
			6	Channel 3 Rx Power Low Alarm Mask		
			5	Channel 3 Rx Power High Warning Mask		
			4	Channel 3 Rx Power Low Warning Mask		
			3	Channel 4 Rx Power High Alarm Mask		
			2	Channel 4 Rx Power Low Alarm Mask		
			1	Channel 4 Rx Power High Warning Mask		
			0	Channel 4 Rx Power Low Warning Mask		
	244	F4h	7	Channel 1 Tx Bias High Alarm Mask	Read Write	00h
			6	Channel 1 Tx Bias Low Alarm Mask		
			5	Channel 1 Tx Bias High Warning Mask		
			4	Channel 1 Tx Bias Low Warning Mask		
			3	Channel 2 Tx Bias High Alarm Mask		
			2	Channel 2 Tx Bias Low Alarm Mask		
			1	Channel 2 Tx Bias High Warning Mask		
			0	Channel 2 Tx Bias Low Warning Mask		
	245	F5h	7	Channel 3 Tx Bias High Alarm Mask	Read Write	00h
			6	Channel 3 Tx Bias Low Alarm Mask		
			5	Channel 3 Tx Bias High Warning Mask		
			4	Channel 3 Tx Bias Low Warning Mask		
			3	Channel 4 Tx Bias High Alarm Mask		
			2	Channel 4 Tx Bias Low Alarm Mask		
			1	Channel 4 Tx Bias High Warning Mask		
			0	Channel 4 Tx Bias Low Warning Mask		
	246	F6h	7	Channel 1 Tx PWR High Alarm Mask	Read Write	00h
			6	Channel 1 Tx PWR Low Alarm Mask		
			5	Channel 1 Tx PWR High Warning Mask		
			4	Channel 1 Tx PWR Low Warning Mask		
			3	Channel 2 Tx PWR High Alarm Mask		
			2	Channel 2 Tx PWR Low Alarm Mask		
			1	Channel 2 Tx PWR High Warning Mask		
			0	Channel 2 Tx PWR Low Warning Mask		

Block Name	Address Decimal	Address Hex	Bits	Description	Access Type	Initial Value
Upper Page 03h	247	F7h	7	Channel 3 Tx PWR High Alarm Mask	Read Write	00h
			6	Channel 3 Tx PWR Low Alarm Mask		
			5	Channel 3 Tx PWR High Warning Mask		
			4	Channel 3 Tx PWR Low Warning Mask		
			3	Channel 4 Tx PWR High Alarm Mask		
			2	Channel 4 Tx PWR Low Alarm Mask		
			1	Channel 4 Tx PWR High Warning Mask		
			0	Channel 4 Tx PWR Low Warning Mask		
	248-249	F8h-F9h	7-0	Reserved Channel Monitor Mask – Set 4	Read Only	00h
	250-251	FAh-FBh	7-0	Reserved Channel Monitor Mask – Set 5	Read Only	00h
	252-255	FCh-FFh	7-0	Reserved	Read Only	00h

Transmitter Input Equalization Control Upper Memory Page 03h Bytes 234-235 (EAh-EBh)

From Table 6-34 of SFF-8636

Code	Transmitter Input Equalization	
	Nominal	Units
11xx	Reserved, Equalization equal to 1010 setting	dB
1011	Reserved, Equalization equal to 1010 setting	dB
1010	10	dB
1001	9	dB
1000	8	dB
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	No Equalization

Receiver Output Emphasis Control Upper Memory Page 03h Bytes 236-237 (ECh-EDh)

From Table 6-35 of SFF-8636

Code	Receiver Output Emphasis At nominal Output Amplitude	
	Nominal	Units
1xxx	Reserved, Emphasis equal to 0111 setting	dB
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	No Emphasis

Receiver Output Amplitude Control Upper Memory Page 03h Bytes 238-239 (EEh-EFh)

From Table 6-33 of SFF-8636

Code	Receiver Output Amplitude No Output Equalization	
	Nominal	Units
1xxx – 0100	Reserved. Stays at Max; equal to 0011 level	mV(P-P)
0011	600-1200 Range not supported Amplitude set to Max, range stays within 400-800	
	mV(P-P)	
0010	400-800	mV(P-P)
0001	300-600	mV(P-P)
0000	100-400	mV(P-P)

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