BROADCOM®

Application Note

Broadcom Evaluation Board for SFP Transceivers

Application Note 1237

SFP Evaluation Board

The purpose of this small form-factor pluggable (SFP) evaluation board is to provide the designer with a convenient means for evaluating SFP fiber-optic transceivers such as those from the AFBR-57Lx and AFBR-57Ex product families as well as those from future SFP MSA compatible product offerings. This document describes the details of the evaluation printed circuit board (PCB) and the test equipment and methods for evaluating SFP modules. The detailed operation of the SFP modules and test equipment used with this evaluation PCB is not described in this document, but can be found by obtaining the appropriate documents from the References section.

Equipment List

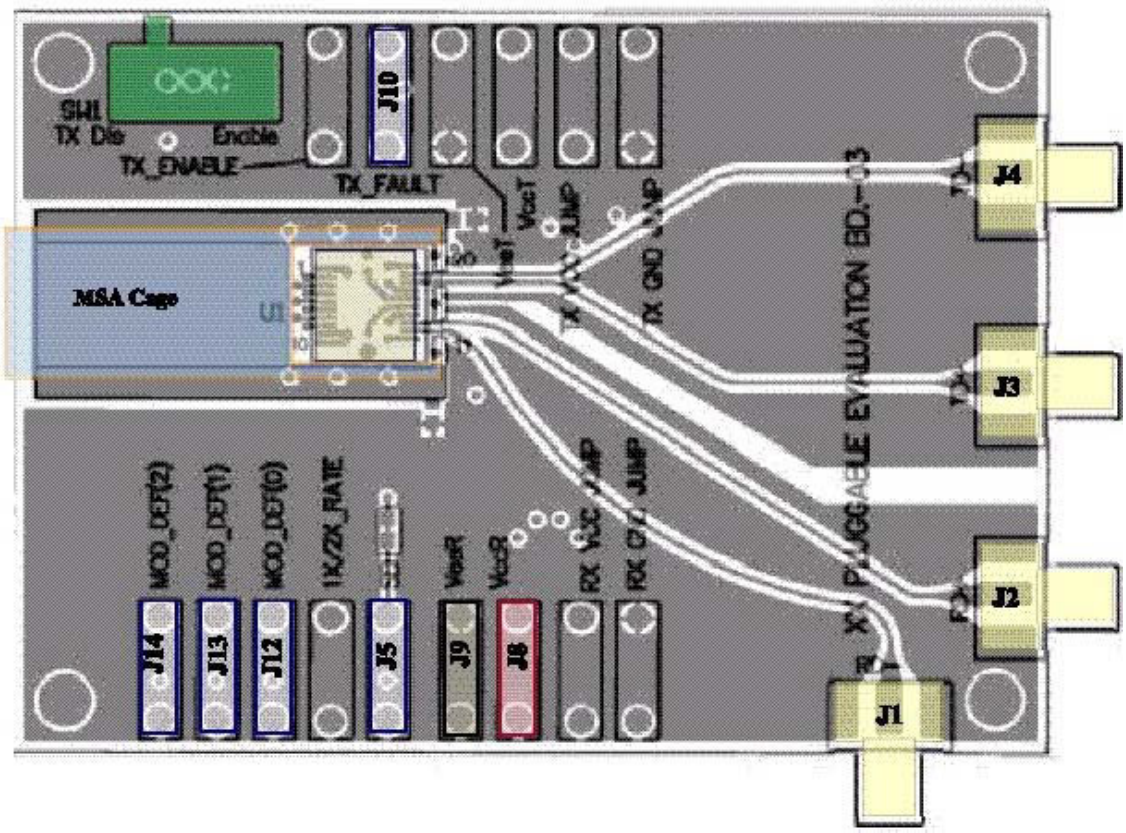
Included:

1. Evaluation PCB
2. SFP transceiver module(s)

Not Included:

1. 3.3V DC power supply
2. Fiber optic cables:
   - LC to SC
     1 meter (50/125 µm) or 1 meter (62.5/125 µm)
   - LC to LC loopback
     <1 meter (50/125 µm) or <1 meter (62.5/125 µm)
3. Keysight 86100A Digital Communications Analyzer (DCA)
4. Keysight Optical/Electrical DCA Plug-In Module 86101A Option H41 or H21 (2125 FC)
5. Keysight 86130A BitAlyzer
   3-Gb/s bit error rate tester (BERT)
   - Pattern generator, error detector/analyzer
6. Fiber optic attenuator (optional)
7. EEPROM reader (optional)
8. PC (optional)

Figure 1: SFP Evaluation Board: Top and Bottom Views



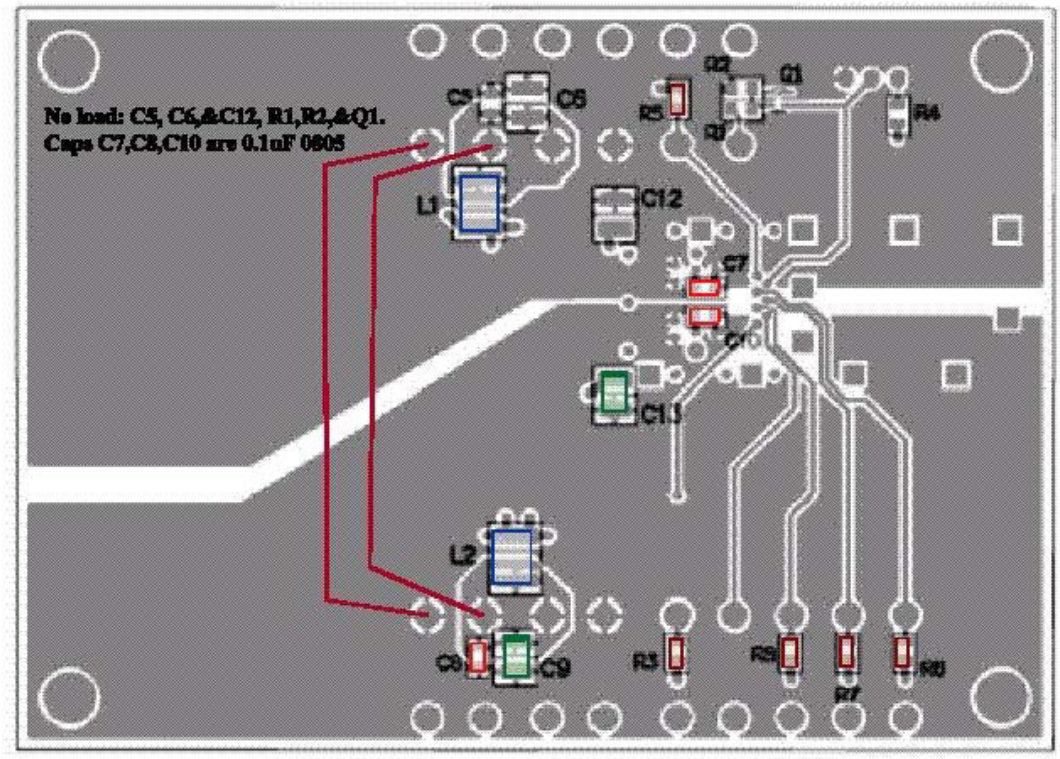


Table 1: I/O Description

Reference Designator	Name	Description	Signal Level
J1	RD -	Differential receiver outputs.	Note [a]
J2	RD +		
J3	TD +	Differential transmitter inputs (< 2.4V).	Note [a]
J4	TD -		
J5	SD(LOS)	Signal detect (LOS) output. Low indicates sufficient optical power; high indicates insufficient optical power.	LVTTL [b]
J6	VccT	Transmitter power, no part. Jumped to J8.	3.3 V
J7	VeeT	Transmitter ground.	GND
J7	VeeT	Transmitter ground, no part. Jumped to J9.	GND
J8	VccR	Receiver power.	3.3 V
J9	VeeR	Receiver ground.	GND
J10	TX Fault	Transmitter fault output. High output indicates a laser fault; low output indicates normal laser operation.	LVTTL [b]
J12	MOD_DEF (0)	Module definition 0. Grounded by module to indicate that the module is present.	LVTTL [b]
J13	MOD_DEF (1)	Module definition 1. Interfaces to the EEPROM. Clock line of the serial interface.	LVTTL [b]
J14	MOD_DEF (2)	Module definition 2. Interfaces to the EEPROM. Data line of the serial interface.	LVTTL [b]
J15	TX VCC JUMP	Not connected. Jump between the left and right sides of the board implemented with wire on the underside.	—
J16	TX GND JUMP		
J17	RX VCC JUMP		
J18	RX GND JUMP		
J19	TX_ENABLE	Not connected. Can be used to electrically switch TX_DISABLE.	—
SW1	TX_DISABLE Switch	Transmitter disable input. Enable (low signal) enables the transmitter; disable position (high signal) disables the transmitter.	LVTTL [b]
U1	SFP Cage Pad	Module plugs in here.	—
—	1X/2X Rate	Rate select pin, not connected.	—

a. Refer to the specific transceiver data sheet for recommended maximums and further information.

b. LVTTL defines a 3.3 voltage level with transitions at 0.8V and 2.0V.

Evaluation PCB Description

Figure 1 shows the top and bottom views of the evaluation PCB. Table 1 shows a description of all input/output (I/O) interfaces on the PCB, all of which are found on the topside of the PCB. The evaluation PCB is a 4-layer design that is compatible with high-speed signal I/O rates required by 2.125-Gbaud Fibre Channel.

Electro-Optical Test Configurations

Figure 2 (transmitter) and Figure 3 (receiver or loopback) show the two basic test configurations for evaluating the SFPs. These test configurations use one evaluation board, 1-meter fiber or <1-meter fiber, together with an attenuator, some 50Ω loads, a power supply, and the test instruments from the equipment list, such as a bit error rate tester (BERT) and a digital communications analyzer (DCA). General considerations from the test configuration follow, but more specific details on SFP transceiver testing can be found in the documents listed in the References section.

Transmitter Configuration

Figure 2 shows the transmitter configuration. The SFP's optical characteristics can be tested, including the eye diagram, jitter, and rise/fall time. Figure 4 shows a representative eye diagram for an SFP. In this configuration, the receiver is not used; however it is recommended that RD- and RD+ be terminated by 50-ohm matched loads. It is also recommended that low-loss, low-dispersion, and equal-length RF cables be used to connect TD+/- to the test equipment.

Receiver Configuration

Figure 3 shows the receiver configuration. The SFP's electrical characteristics can be tested, including the receiver electrical eye diagram, jitter, and rise/fall time. Figure 5 shows a representative eye diagram for an SFP.

Results

The following example measurements were made using the configurations illustrated in Figure 2 and Figure 3.

Figure 2: Recommended Transmitter Test Configuration

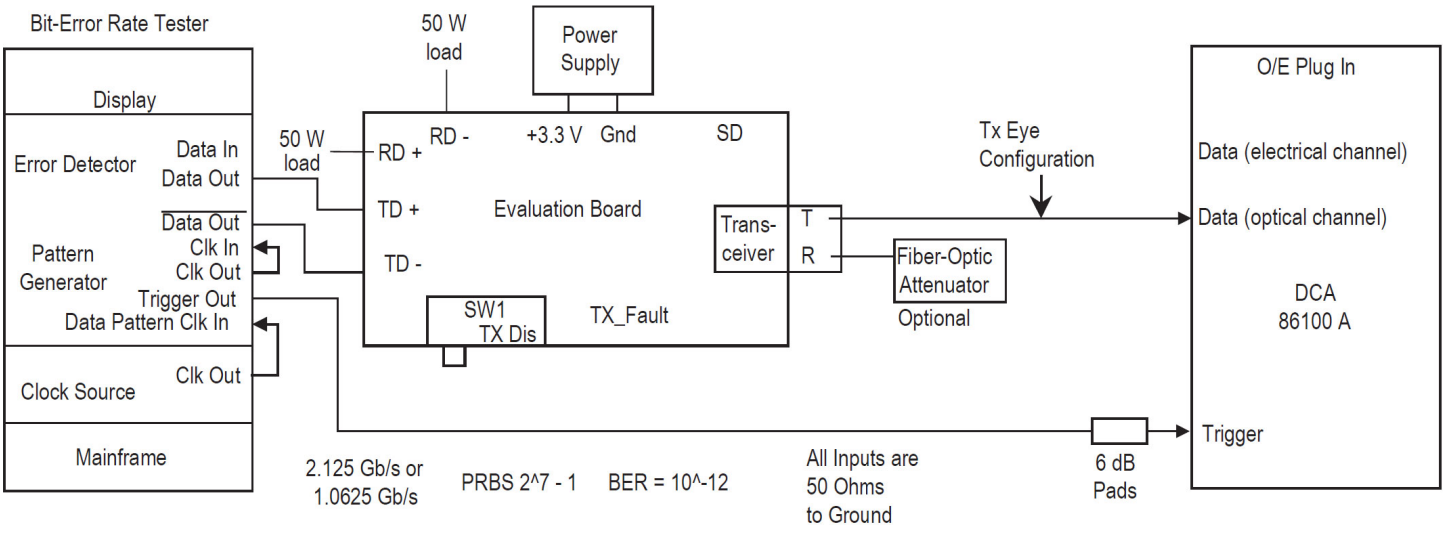
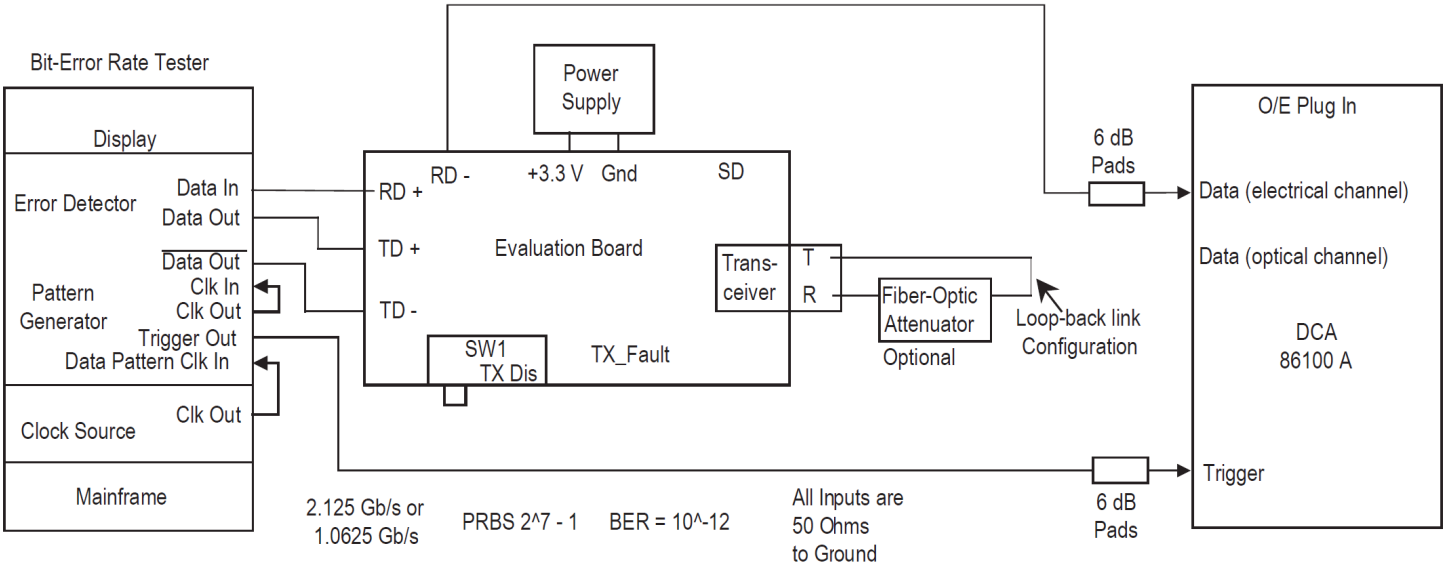


Figure 3: Recommended Receiver Test Configuration



EEPROM Test Configuration

The SFP MSA specifies an EEPROM internal to the transceiver that meets the ATMEL AT24C01A industry standard. The standard two-wire serial protocol can be implemented to allow the user to read the contents of the EEPROM by using the MOD_DEF (1) and MOD_DEF (2) connections on the evaluation board. Note that MOD_DEF (0) is grounded by the module to indicate that the module is present and is not used during the read operation of the EEPROM.

Figure 6 shows a typical test configuration reading the EEPROM. This configuration includes an optional EEPROM reader such as that from ChipMax and Control PC. This EEPROM reader uses a standard 40-pin Textool socket to interface to the device under test and a parallel port to interface to a control computer to use the software provided with the ChipMax unit. The Textool socket is divided into slots for a 24-pin DIP and slots for an 8-pin DIP. The pins referenced in Figure 6 refer to the slots for the 8-pin DIP.

Information regarding pin definitions and contents for the EEPROM can be found in the specific Broadcom SFP module data sheets or by checking the SFP MultiSource Agreement.

Figure 4: Example Transmitter Eye Diagram

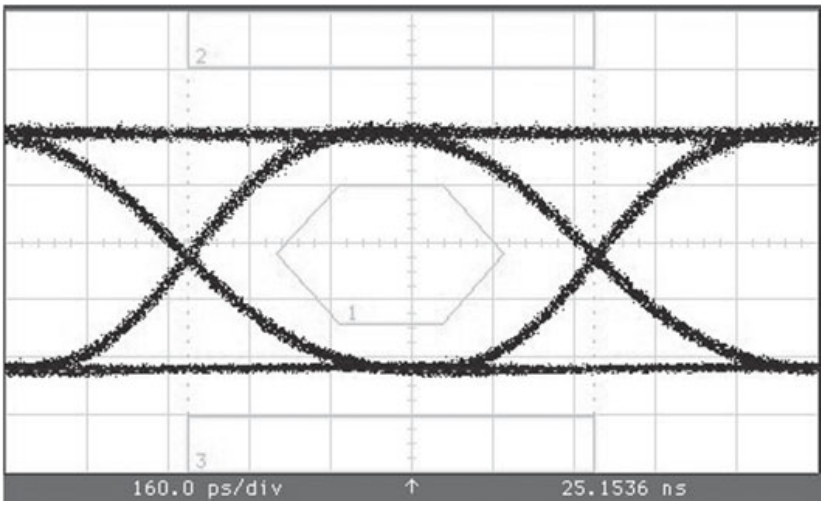


Figure 5: Example Loopback Receiver Eye Diagram: –17-dBm Power

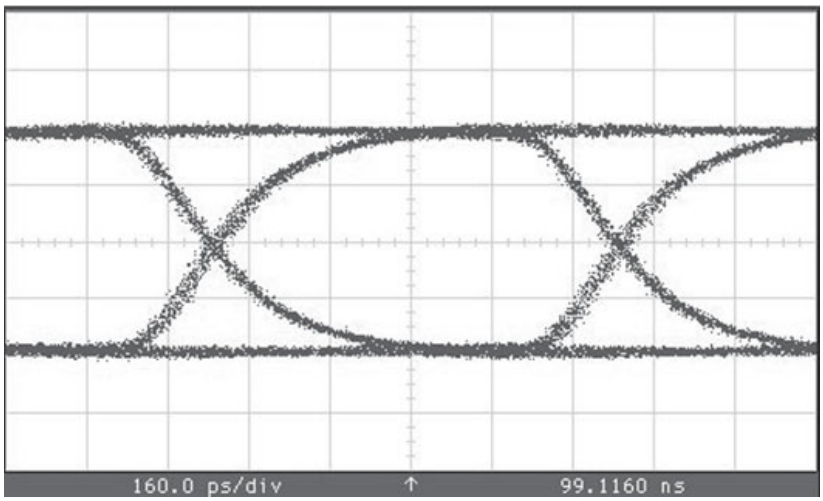
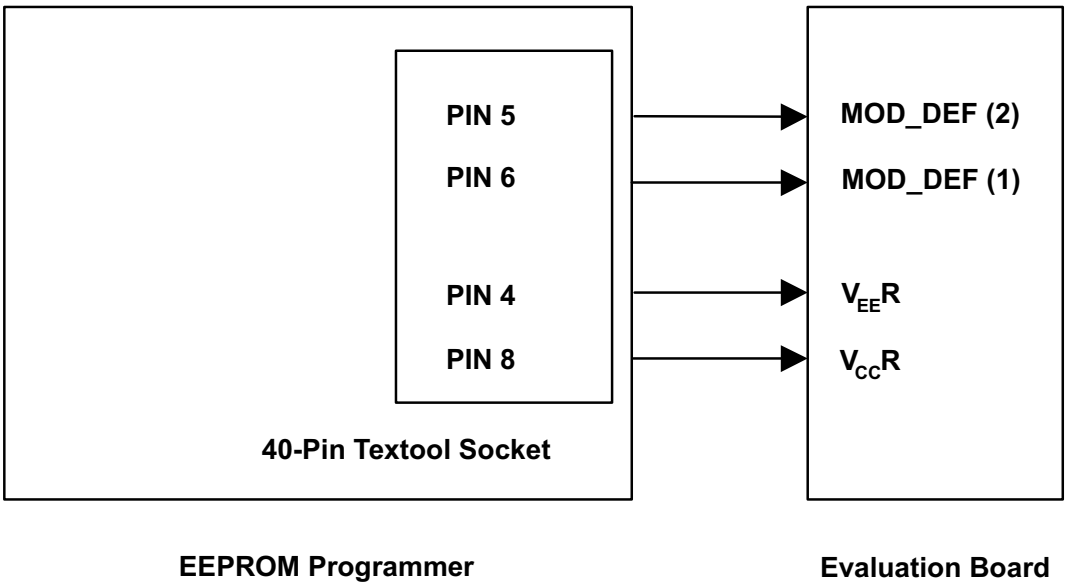


Figure 6: EEPROM Test Configuration



Evaluation Board Schematic and Bill of Materials

Figure 7 shows the SFP evaluation board electrical schematic. The user may notice connections on the board that are not represented on this schematic (Figure 7) or in the pin description (Table 1). This is due to optional functionality of the board. For simplicity and ease of application, only those connections and parts included are described in the schematic and bill of materials (Table 2).

References

1. AFBR-57xx Product Data Sheets: http://www.broadcom.com
2. Broadcom Application Notes: http://www.broadcom.com
3. Test Equipment User Manuals: http://www.broadcom.com

Table 2: SFP Evaluation Board Bill of Materials

Component	Type	Value	Footprint	Comments
PCB	SFP Evaluation Board	—	—	Unpopulated 4-layer circuit board
U1	Surface-mount socket (20 pin)	—	—	AMP 1367073-1
—	Case jacks	—	—	0 (4 off), Advance Interconnect part 1718 or Cambion part 450-3704-01-03-00
Q1	Transistor	—	UMX3N	Rohm dial npn transistor, not included
—	Device jacks	—	—	—
—	Nose jacks	—	—	0 (2 off), Cambion part 450-3704-01-03-00
R3, R5, R6, R7, R8	Resistor	4.7K	805	—
C5, C7, C8, C10	Capacitor	0.1 µF	805	10% tolerance
C6, C9	Capacitor	10 µF	Case code B	Tantalum 20% tolerance
C13	Capacitor	10 µF	Case code B	Tantalum 20% tolerance
L1, L2	Inductor	1 µF	1812	—
SW1	Switch	—	—	Apem 25336NA
J1, J2, J3, J4	End launch SMA jack (tab contact)	—	—	DigiKey part number 142-0701-851
J5	Jack, 2 mm white	—	—	SD, Signal Detect
J8	Jack, 2 mm red	—	—	VccR
J9	Jack, 2 mm black	—	—	VeeR, RX_GND
J10	Jack, 2 mm white	—	—	TX_FAULT
J12, J13, J14	Jack, 2 mm white	—	—	MOD_DEF

Figure 7: SFP Evaluation Board Circuit