BROADCOM®

Data Sheet

BCM88830

3.2-Tb/s Integrated Packet Processor, Traffic Manager, and Fabric Interface Single-Chip Device

Overview

The Broadcom® BCM88830 series is an optimized switching solution for fifth generation (5G) mobile backhaul, routing, transport, and data center interconnect (DCI) applications. The product series enables switching platforms with a mix of Ethernet and Flexible Ethernet (FlexE) ports.

The BCM88830 series belongs to the seventh generation of the StrataDNX™ scalable switching product line and processes up to 3.2 Tb/s of traffic, operating at Layer 1 through Layer 4.

Because it is optimized for 5G mobile backhaul, the BCM88830 implements a fully-featured, large-scale network-slicing solution at wire speed. It supports the fast creation of slices and the isolation of these services in the converged network. When configuring network slices, the user can leverage flexible forwarding classification, virtual databases, and large-scale segment routing. Bandwidth management per-slice is programmable and supports hierarchical quality-of-service (HQoS), scheduling, and shaping. Latency-sensitive slices, such as radio traffic, can be assigned low-latency and lossless resources.

The Elastic Pipe™ packet classification engine is software programmable, with built-in support for carrier and data center networking applications. The large on-chip classification databases are scaled to support any switching or routing application.

The traffic manager integrates deep-packet buffers with a distributed scheduling scheme that allows state-of-the-art HQoS, transmission scheduling per customer and per service, as well as tunneling and overlay networks. Flexible flow control mechanisms support Priority-based Flow Control (PFC), Enhanced Transmission Selection (ETS), and Explicit Congestion Notification (ECN).

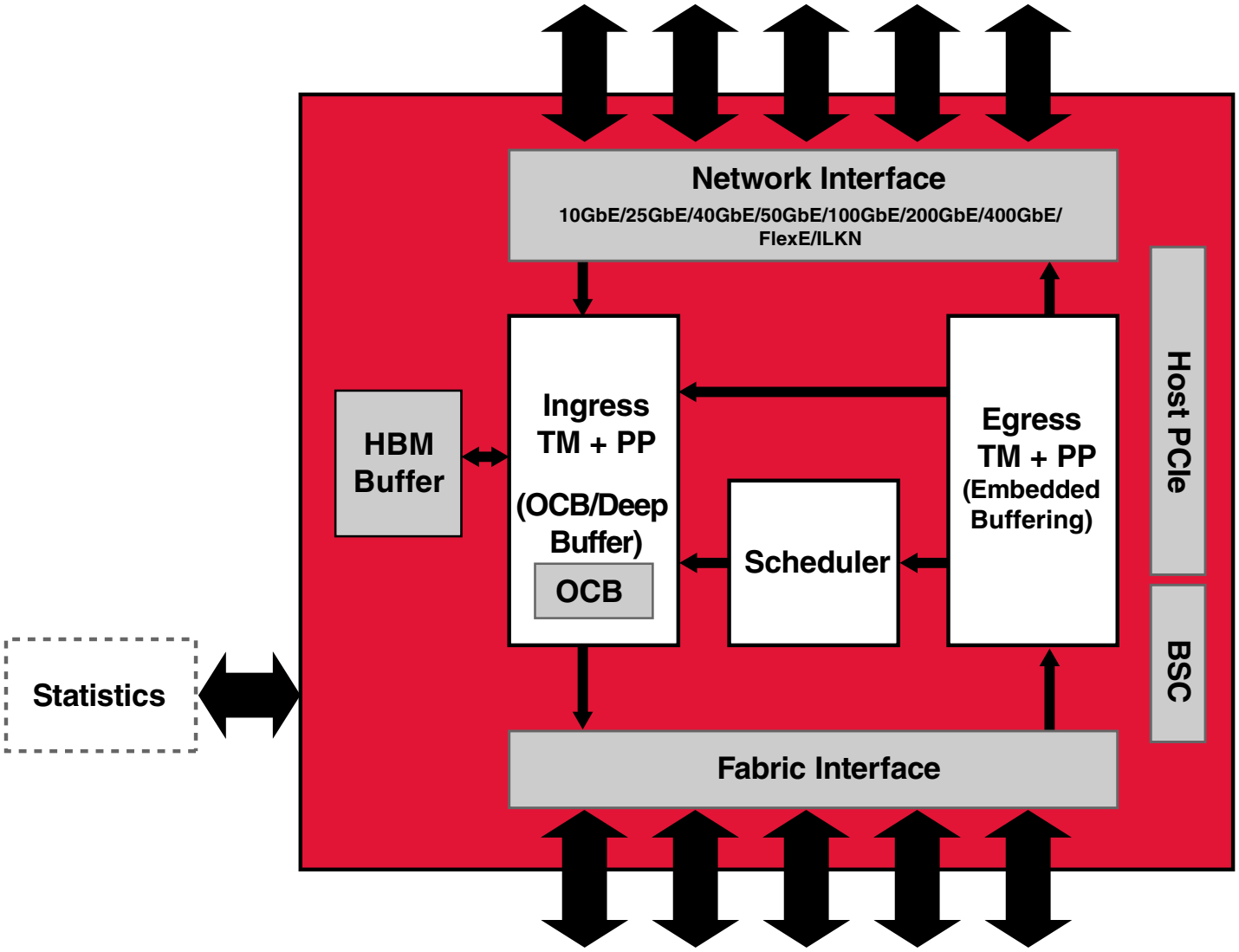
The BCM88830 integrated FlexE core provides an additional way to optimize the uplink bandwidth in backhaul, transport, and DCI applications. FlexE clients can manage the bandwidth allocation per service. An integrated FlexE cross-connect unit minimizes the latency of sensitive services, such as ultra-reliable and low-latency communication (URLLC), through a dedicated high-speed switching plane.

The integrated bypass path delivers latency-sensitive services, such as transport or mobile traffic.

Features

- Eighth-generation Dune scalable fabric access processor (FAP) product line.
- Flexible network interface:
  - Ethernet: 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE, and 400GbE interfaces.
  - FlexE network interface: Large number of FlexE clients. Flexible line rate.
  - Interlaken (ILKN): 24 lanes, up to 25.78125 Gb/s per lane, and up to two interfaces.
- Traffic manager:
  - On-chip buffer with off-chip deep-buffering option.
  - Hierarchical memory management.
  - Programmable, hierarchical scheduling.
  - Compliant with scheduling and shaping standards, including Metro Ethernet Forum (MEF) and Broadband Forum standards.
- Flexible and software-programmable Elastic Pipe packet processor:
  - Bridging, routing, Multiprotocol Label Switching (MPLS), Virtual Private LAN Service (VPLS), Layer 2 virtual private networks (L2VPNs), Layer 3 virtual private networks (L3VPNs), and Operations, Administration, and Maintenance (OAM).
  - MPLS and IPv6 segment routing.
  - Data center tunneling encapsulations including Virtual Extensible LAN (VXLAN), Network Virtualization using Generic Routing Encapsulation (NVGRE), and Generic Network Virtualization Encapsulation (GENEVE).
  - Built-in support for data center, carrier, and metro.
  - Ethernet and packet-transport applications.
  - Large on-chip tables with off-chip expandability.
- Fabric interface:
  - SerDes interface to the StrataDNX fabric element (BCM88790).
  - Fabric-less (mesh, without the use of the BCM88790 device) supporting up to two devices.
- Bypass mode:
  - Delivery of latency-sensitive services, such as transport or mobile traffic.
  - Unified data plane for TDM and Ethernet.
- Precision Time Protocol (PTP), IEEE 1588, and Synchronous Ethernet (SyncE).
- Time-sensitive network (TSN) support.
- In-band management.

Figure 1: Functional Block Diagram



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Chapter 1: Introduction

1.1 Features

The Broadcom BCM88830 is an optimized switching solution for 5G mobile backhaul, routing, transport, and data center interconnect (DCI) applications, enabling switching platforms with a mix of Ethernet, Interlaken (ILKN), and FlexE ports.

The following features are available with the BCM88830:

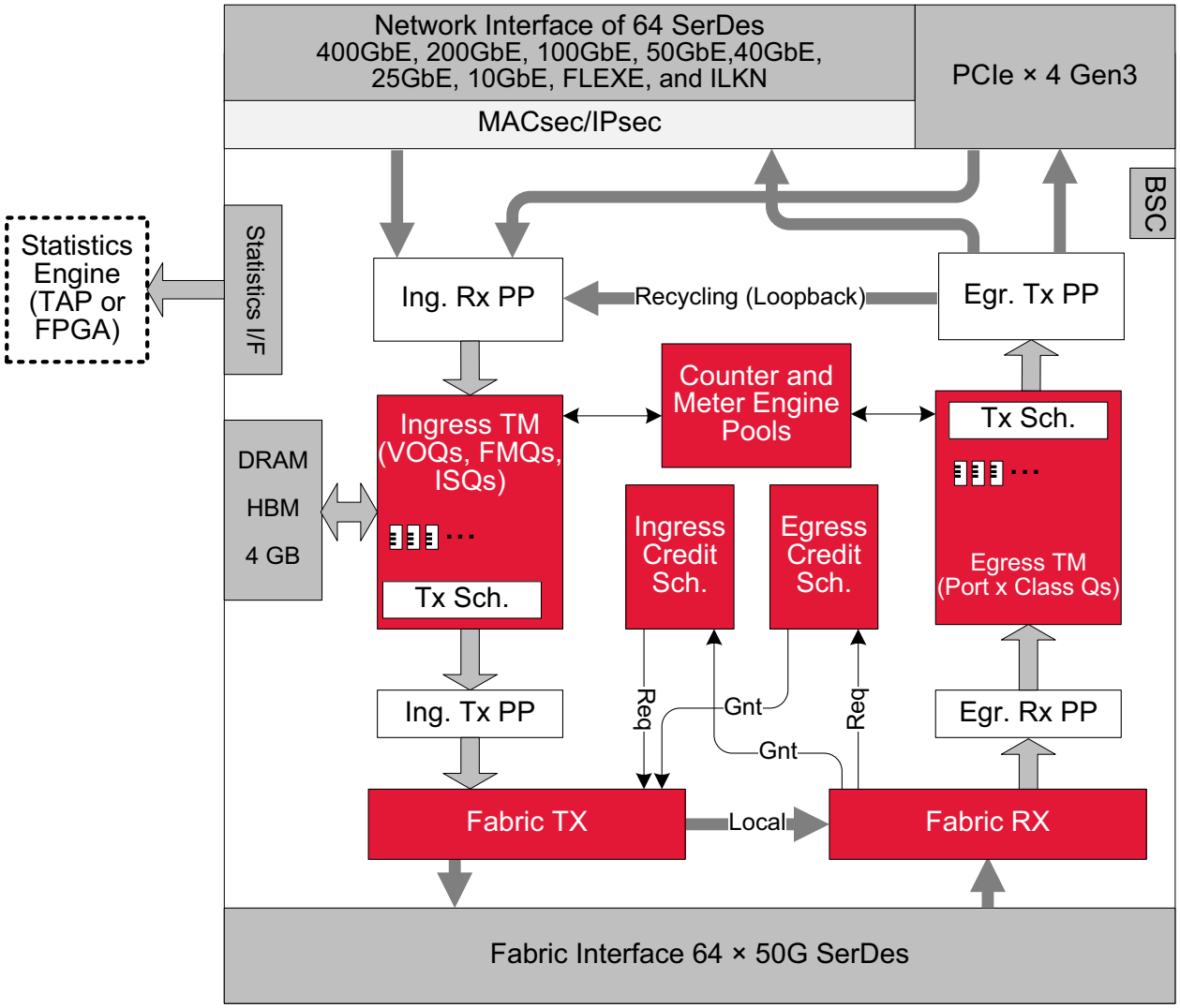
- High performance:
  - 3.2 Tb/s full-duplex, integrated traffic manager, packet processor, and Layer 1 switching device.
  - 1050-Mp/s processing rate.
- StrataDNX fabric interface:
  - 64 SerDes for up to 53.125-Gb/s serial links (PAM-4 with symbol rate of 26.5625 Gbaud).
  - Mesh configurations of up to two devices.
  - Dynamically variable-sized cells for highly efficient segmentation.
  - Multiple line coding options with Reed-Solomon Forward Error Correction (RS-FEC), which optimizes performance according to system characteristics.
  - Dynamic routing and load balancing over all fabric links.
  - 1 + 1, *N* – *x*, and *N* + *x* redundancy schemes.
  - Automatic fault detection and recovery with no software intervention.
- Flexible network interface:
  - Up to 1.6 Tb/s of total network interface (NIF) traffic and 85 Gb/s for FlexE management and control purposes.
  - 64 SerDes with rates up to 53.125 Gb/s.
  - Packet lengths supported in the range 64B to 9600B.
  - Ethernet ports supporting the following port configurations:
    - 64 × 10GbE/25GbE over one lane.
    - 32 × 50GbE over one lane.
    - 32 × 50GbE over two lanes
    - 16 × 40GbE/100GbE over four lanes.
    - 16 × 100GbE over two lanes.
    - 8 × 200GbE over four lanes.
    - 4 × 400GbE over eight lanes.
  - ILKN support for up to 24 lanes, up to 25.78125 Gb/s per lane, and up to two interfaces.
  - FlexE:
    - Full support of the Optical Internetworking Forum (OIF) FlexE standard versions 1.x and 2.x.
    - Up to 1.6 Tb/s of total FlexE traffic.
    - Bonding of up to 16 PHYs in a group.
    - Up to 320 FlexE clients, with client bandwidth granularity of 1 Gb/s.
    - Sub-rating of Ethernet PHYs.
    - Accurate time synchronization.
    - Layer 1 switching of FlexE clients.
    - Switching at Layer 2 through Layer 4 of FlexE and Ethernet traffic.

- Traffic manager:
  - 128K programmable wire-rate queues.
  - Deep packet buffering, in-package HBM Gen2 for a total of 4 GB.
  - Congestion management:
    - Hierarchical weighted random early detection (WRED) and tail-drop policies.
    - Congestion notification – Congestion notification message (CNM) generation and CNM reception (proxy).
    - Flow control generation – Fully programmable.
    - Flow control reception-any level – Interface, port, class, flow, traffic type.
    - Priority flow control (PFC) – Eight levels.
    - Congestion tracking statistics.
    - Three ingress meter operations per packet.
    - Two egress meter operations per packet.
  - Hierarchical scheduling and shaping:
    - Fully programmable to any depth.
    - Support for priority propagation.
  - MEF and Broadband Forum TR-059-compliant scheduling and shaping
- Packet processor:
  - Bridging, routing, MPLS, VPLS, L2VPNs, L3VPNs, and OAM.
  - MPLS and IPv6 segment routing.
  - Data center tunneling encapsulations including VXLAN, NV-GRE, and GENEVE.
  - Built-in support for data center, carrier and metro Ethernet, and transport applications.
  - Large modular on-chip databases, application-oriented.
  - OAM accelerator engine.
  - PEM (flexible pipe).
- Counters, meters, and statistics:
  - On-chip counter pool up to 384K counters.
  - On-chip meter pool up to 256K meters.
  - Statistics interface for expandable, off-chip statistics gathering:
    - The SerDes used for the statistics interface is shared with network interface (NIF) SerDes.
    - Efficient packet-based protocol based on Ethernet simplifies connectivity to KBP BCM16K, TAP BCM5235, or FPGAs.
    - Seamless connection to KBP BCM16K or TAP BCM5235 devices.
- Multicast – Pointer-based ingress and egress multicast replication.
- IEEE 1588 support with improved time-stamping accuracy of nanosecond scale.
- In-band management.
- PCIe × four-lane Gen3 host interface with DMA.
- Hardware linkscan engine.
- LED processor.

1.2 Device Overview

The following figure is a high-level functional block diagram of the BCM88830.

Figure 2: BCM88830 Block Diagram



As shown in Figure 2, BCM88830 Block Diagram, the BCM88830 device includes the following functional blocks.

Traffic Manager

- Ingress traffic manager (TM):
  - Manages a pool of queues in on-chip SRAM and in High Bandwidth Memory (HBM) DRAM.
  - Replicates packets for multicast, snooping, and mirroring.
- Ingress and egress end-to-end credit scheduler – Schedules packets out of the ingress TM.
- Egress traffic manager:
  - Manages a pool of egress queues in on-chip memory.
  - Schedules traffic toward packet interfaces – Network, PCIe, internal hosts, and recycling (loopback).
  - Replicates multicast packets.
- Fabric transmit and fabric receive:
  - Segments packet to cells.
  - Transmit – Load-balances cells across fabric SerDes.
  - Receive – Reassembles cells into packets.
- Counter engines:
  - General-purpose counters.
  - Ingress and egress counting.
  - Configurable counting modes and criteria.
- Meter engines:
  - General-purpose metering using a pool of meters for traffic metering.
  - Ingress and egress metering.
  - Metering according to the packet processor command.

Packet Processing

- Ingress receive packet processor:
  - Functions as the main packet processing stage.
  - Identifies incoming interface link layer, tunnel, PWE, and AC.
  - Determines where to forward the packet based on packet forwarding header (L2, L3, MPLS, and so on).
  - Appends a packet processor (PP) header.
- Ingress transmit packet processor:
  - Edits the packet (or packet copy) before transmitting to egress PP.
- Egress receive packet processor:
  - Filters packets according to various criteria.
- Egress transmit packet processor:
  - Edits packets according to the PP header (from ingress).

Interfaces

- Network interface:
  - Includes 64 dedicated SerDes up to 53.125 Gb/s (PAM-4).
  - Supports various port types, including 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE, 400GbE, FlexE, and ILKN.
- Fabric interface:
  - Includes up to 64 SerDes.
  - Supports up to 53.125 Gb/s (PAM-4) per link.
  - Detects and corrects errors using Reed-Solomon Forward Error Correction (RS-FEC).
- Statistics interface:
  - Shares NIF SerDes.
  - Uses Ethernet ports, up to 400GbE per statistics interface.
  - Generates statistics records over packets.
- PCIe × 4 lane Gen3 host interface:
  - Accesses configuration and status registers.
  - Transfers packets to and from host memory by using DMA.
- BSC (NXP I^2C-compatible) 2-line interface:
  - Performs basic device debug and register access (PCIe only).
  - Programs PCIe QSPI flash.
  - Loads code for heating when an industrial device is powered-up at a low ambient temperature (not supported by the current SDK).

Chapter 2: System Configurations

2.1 Broadcom StrataDNX Components

The StrataDNX architecture includes two types of components: Fabric Elements (FEs) and Fabric Access Processors (FAPs):

- FEs do the following:
  - Are used to build a Clos fabric.
  - Provide self-routing, cell-based switching.
  - Support both single-stage and multistage fabric configurations.
- FAPs do the following:
  - Provide integrated fabric access and traffic management functions.
  - Provide an integrated packet processor.
  - May be used as a stand-alone TM (ingress, egress, or both) or with a fabric.

2.1.1 Interoperation with StrataDNX Fabric Element Devices

The BCM88830 can interoperate in a system with the following FE devices:

- BCM88790
- BCM88770

2.1.2 Interoperation with StrataDNX Fabric Access Processor Devices

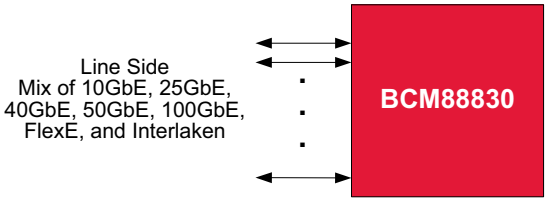
The BCM88830 can interoperate in a system with the following FAP devices:

- BCM88830
- BCM88850
- BCM88800
- BCM88690
- BCM88680
- BCM88670

2.2 Stand-Alone Configurations

The BCM88830 may be used as a stand-alone switch device with ingress/egress intelligent TM. The integrated TM enables intelligent oversubscription with granular, per-flow (or per-customer-and-traffic-class) scheduling and shaping in the upstream direction, downstream direction, or both.

Figure 3: BCM88830 Switch with Integrated Traffic Manager Example



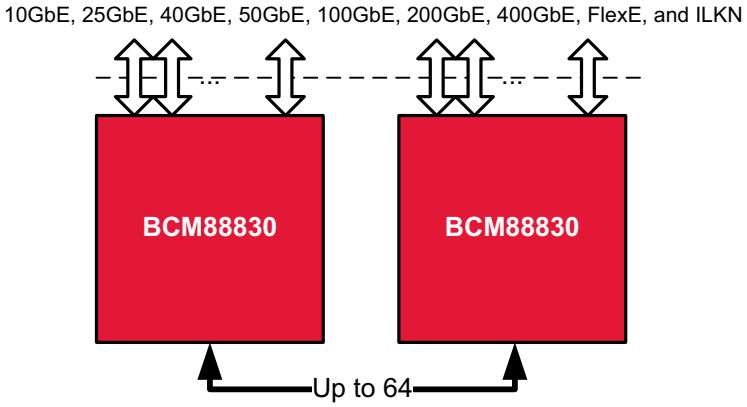
As shown in Figure 3, the BCM88830 offers a flexible set of user interfaces, supporting a mix of 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE, and 400GbE Ethernet ports, as well as FlexE interfaces from 50G to 1.6T using PHYs of 50G, 100G, 200G, or 400G, and Interlaken interfaces.

In the upstream direction from the network interfaces into the system, the integrated TM intelligently manages the oversubscription. In the downstream direction, the integrated TM may schedule and shape traffic, possibly per-customer and per-application.

2.3 Back-to-Back and Mesh Fabric Configurations

The BCM88830 devices may be interconnected in a back-to-back (mesh) configuration without the use of StrataDNX Fabric Elements. Figure 4 shows two BCM88830 devices connected back-to-back through up to 64 fabric links, creating a 3.2-Tb/s fabric-less switching system.

Figure 4: Two BCM88830 Devices in a Back-to-Back (Mesh) Configuration



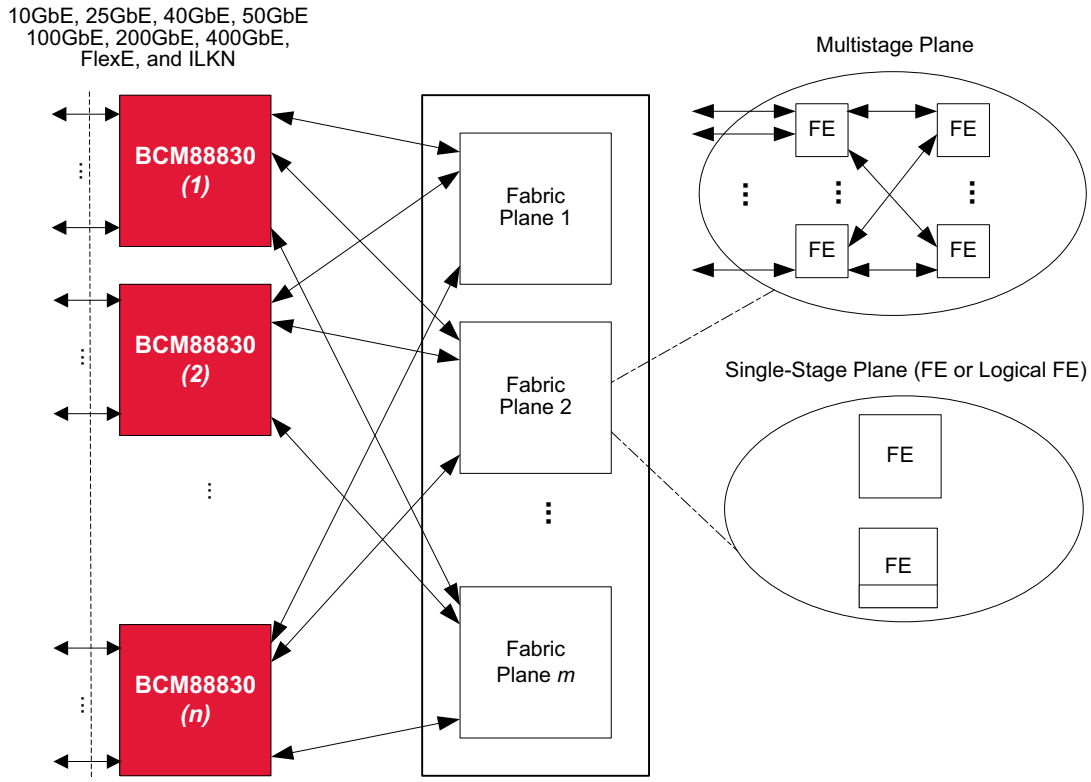
Other mesh configuration options are as follows:

- Three devices using 32 links between each other, creating a 4-Tb/s fabric-less switching system.
- Four devices using 21 links between each other, providing net bandwidth of about 1 Tb/s between each two devices.

2.4 StrataDNX CLOS Fabric Configurations

A StrataDNX fabric with Fabric Element devices (for example, the BCM88790) interconnects the FAP devices for medium-to-large nonblocking configurations. With the BCM88830, the StrataDNX fabric scales from 1.6 Tb/s to 1638 Tb/s.

Figure 5: FAPs Interconnected by StrataDNX Fabric



In Figure 5, *n* FAP devices are interconnected through a Clos fabric composed of Fabric Elements. The number of interconnected FAP devices can range from 1 to 1024. A StrataDNX fabric based on the BCM88790 or BCM88770 accommodates a mix of BCM88830, BCM88850, BCM88800, and BCM88690 FAP devices, all of which are interconnected and interoperate simultaneously.

Chapter 3: System Interfaces

3.1 Network Interface

The BCM88830 network interface (NIF) includes eight Ethernet port macros (PMs) based on 50G SerDes (PM50), one Interlaken core, and FlexE framer.

Ethernet PMs

The BCM88830 Ethernet PM capabilities are as follows:

- Eight Ethernet PMs supporting SerDes rates up to 53.125 Gb/s (PM50).
- Each PM50 includes four Blackhawk (BH2x2) SerDes cores, each supporting two lanes, up to 53.125 Gb/s.
- Each PM50 supports the following configurations:
  - 1 × 400GbE port over eight lanes (PAM-4)
  - 2 × 200GbE ports over four lanes (PAM-4)
  - 4 × 100GbE ports over two lanes (PAM-4)
  - 2 × 100GbE ports over four lanes
  - 8 × 50GbE ports over one lane (PAM-4)
  - 4 × 50GbE ports over two lanes
  - 2 × 40GbE ports over four lanes
  - 8 × 25GbE ports over one lane
  - 8 × 10GbE ports over one lane
- Receive buffering:
  - Per-port buffer
  - Temporary buffering before injection into the ingress packet processor pipeline.
  - Used for burst absorption in case the total packet rate is higher than the device core processing capability.
  - Interface (link level) flow-control generation.
- Transmit buffering:
  - Temporary buffering before transmission through the Ethernet port.
  - Enable interface (link level) flow-control reception fast reaction time.

FlexE Core

The BCM88830 supports a 1600G FlexE core with the following capabilities:

- Up to 1600G FlexE traffic.
- Up to 16 FlexE groups.
- Up to 320 clients. Client bandwidth can be from 1G to 1600G.

Interlaken Core

The following are the BCM88830 Interlaken core capabilities:

- The Interlaken core can be configured as two interfaces that can support up to 12 lanes each, or a single interface that can support up to 24 lanes.
- ILKN lane rate is up to 25.78125 Gb/s (NRZ).
- ILKN FEC is not supported in the BCM88830.

3.1.1 Network Interface Configurations

The following table describes the mapping of PMs to SerDes and provides the naming convention of the interfaces.

Table 1: BCM88830 NIF SerDes Mapping

PM Number	SerDes Number	Ethernet	FlexE	ILKN (NRZ Only)	STAT
PM50_0	00 to 07	+	+	+	—
PM50_1	08 to 15	+	+	+	—
PM50_2	16 to 23	+	+	+	—
PM50_3	24 to 31	+	+	—	+
PM50_4	32 to 39	+	+	—	—
PM50_5	40 to 47	+	+	—	—
PM50_6	48 to 55	+	+	—	—
PM50_7	56 to 63	+	+	—	—

3.1.2 Provisioning of the Network Interface

The BCM88830 flexible NIF can be provisioned with aggregated connectivity that does not exceed the 1.6T switching capacity.

This bandwidth provisioning restriction applies to any combination of the interfaces (Ethernet, FlexE, and Interlaken).

When connecting NIF lanes to the system management (CPU, FPGA, and so on), these ports can pass additional traffic at up to 85 Gb/s.

3.1.3 Ethernet Ports

Ethernet ports are implemented by the Ethernet port macro (PM). The PMs include the MAC layer and physical coding sublayer (PCS) of Ethernet ports. The BCM88830 includes PM50 based on Blackhawk SerDes cores, known as BH2x2, that support SerDes rates up to 53.125 Gb/s. Each BH2x2 has two SerDes and two PLLs. In total, there are eight SerDes per PM50.

The following table shows the port modes supported by PM50.

NOTE:

- RS272 FEC is a Broadcom-proprietary protocol to achieve lower latency.
- For 100G and 50G ports using RS-272 FEC mode, the FEC engine serves four SerDes lanes. If using RS-272, no other FEC mode can be used in the same FEC engine.
- BASE-R FEC indicates IEEE 802.3, Clause 74-compliant FEC.

Table 2: PM50 Supported Port Modes

Port Speed	No. of Lanes	Port Mode	SerDes Rate (Gb/s)	VCO Rate (GHz)	SerDes Mode	FEC	Related Standard
400GbE	8	400GAUI-8 C2C	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3 Annex 120D
		400GAUI-8 C2M	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3 Annex 120E
		400GBASE-KR8	53.125	26.5625	PAM-4	RS-544, RS-272	This is 400GAUI-8 with KR interface as defined in IEEE 802.3cd CL137
		400GBASE-CR8	53.125	26.5625	PAM-4	RS-544, RS-272	This is 400GAUI-8 with CR interface as defined in IEEE 802.3cd CL136
200GbE	4	200GAUI-4 C2C	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3 Annex 120D
		200GAUI-4 C2M	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3 Annex 120E
		200GBASE-KR4	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3cd CL137
		200GBASE-CR4	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3cd CL136
100GbE	2	100GAUI-2 C2C	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3cd Annex 135F
		100GAUI-2 C2M	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3cd Annex 135G
		100GBASE-KR2	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3cd CL137
		100GBASE-CR2	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3cd CL136
		CAUI-2 C2C	51.5625	25.78125	PAM-4	RS-528	IEEE 802.3 (CAUI-4) port, bit-muxed to two lanes with C2C interface as defined in IEEE 802.3cd Annex 135F
		CAUI-2 C2M	51.5625	25.78125	PAM-4	RS-528	IEEE 802.3 (CAUI-4) port, bit-muxed to two lanes with C2M interface as defined in IEEE 802.3cd Annex 135G

Table 2: PM50 Supported Port Modes (Continued)

Port Speed	No. of Lanes	Port Mode	SerDes Rate (Gb/s)	VCO Rate (GHz)	SerDes Mode	FEC	Related Standard
100GbE	4	CAUI-4 C2C	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 Annex 83D
		CAUI-4 C2M	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 Annex 83E
		100GBASE-KR4	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 CL93
		100GBASE-CR4	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 CL92
		100GAUI-4 C2C	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135D
		100GAUI-4 C2M	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135E
50GbE	1	50GAUI-1 C2C	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3cd Annex 135F
		50GAUI-1 C2M	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3cd Annex 135G
		50GBASE-KR	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3cd CL137
		50GBASE-CR	53.125	26.5625	PAM-4	RS-544, RS-272	IEEE 802.3cd CL136
50GbE	2	LAUI-2 C2C	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3cd Annex 135B
		LAUI-2 C2M	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3cd Annex 135C
		50GBASE-KR2	25.78125	25.78125	NRZ	RS-528, no FEC	50GbE with KR interface as defined in IEEE 802.3 CL93
		50GBASE-CR2	25.78125	25.78125	NRZ	RS-528, no FEC	50GbE with CR interface as defined in IEEE 802.3 CL92
		50GAUI-2 C2C	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135D
		50GAUI-2 C2M	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135E
40GbE	4	XLAUI	10.3125	25.78125	NRZ	BASE-R, no FEC	IEEE 802.3 Annex 83A
		40GBASE-KR4	10.3125	25.78125	NRZ	BASE-R, no FEC	IEEE 802.3 CL84
		40GBASE-CR4	10.3125	25.78125	NRZ	BASE-R, no FEC	IEEE 802.3 CL85
		XLPPI	10.3125	25.78125	NRZ	BASE-R, no FEC	IEEE 802.3 Annex 86A
25GbE	1	25GAUI C2C	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 Annex 109A
		25GAUI C2M	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 Annex 109B
		25GBASE-KR/25GBASE-KR-S	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 CL111
		25GBASE-CR/ 25GBASE-CR-S	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 CL110

Table 2: PM50 Supported Port Modes (Continued)

Port Speed	No. of Lanes	Port Mode	SerDes Rate (Gb/s)	VCO Rate (GHz)	SerDes Mode	FEC	Related Standard
10GbE	1	10GBASE-KR	10.3125	25.78125	NRZ	BASE-R, no FEC	IEEE 802.3 CL72
		XFI	10.3125	25.78125	NRZ	BASE-R, no FEC	XFI+ (FC-PI-3)
		SFI	10.3125	25.78125	NRZ	BASE-R, no FEC	SFF-8431
		Direct attached cable (DAC)	10.3125	25.78125	NRZ	BASE-R, no FEC	—

3.1.3.1 Mixed Port Types on PM50

The PM50 supports the PCS and MAC layers and can manage different types of Ethernet (ETH) ports.

For the physical medium dependent sublayer (PMD), the BCM88830 PM50 contains four BH2x2 cores, where each BH2x2 core has two Blackhawk TX/RX SerDes and their PLLs.

Support for port types on the same PM50 or on the same BH2x2 within a PM50 is as follows:

- A mix of any ETH or FlexE ports in the same PM50 is allowed.
- A mix of any two ETH or FlexE ports in the same BH2x2 is allowed.
- For a PM50 that supports ILKN, a mix of ILKN, ETH and FlexE in the same PM50 is allowed.
- A mix of ILKN and ETH or ILKN and FlexE in the same BH2x2 is not supported.
- A mix of statistics interface ports and NIF Ethernet/FlexE ports on PM50-3 is not supported.

3.1.3.2 Lane Mapping (Lane Swap) in BCM88830 PM50

The following table shows the default SerDes-to-lane assignment.

Table 3: Default SerDes-to-Lane Assignment in PM50

Logic Lane	Default PM50 SerDes (<BH2x2>.<SerDes>)
0	0 (0.0)
1	1 (0.1)
2	2 (1.0)
3	3 (1.1)
4	4 (2.0)
5	5 (2.1)
6	6 (3.0)
7	7 (3.1)

3.1.3.2.1 ETH and FlexE Lane Mapping

To ease board design, the PM50 permits SerDes-to-lane mapping (lane swap) to enable non-default configurations.

The design allows TX and RX lane swapping with the limitation that TX SerDes and RX SerDes must be in the same BH2x2 core.

The following table shows an example of a lane swap case.

Table 4: Lane Swap Example

Port Definition	Logic Lane	PM50 TX SerDes (<BH2x2>.<SerDes>)	PM50 RX SerDes (<BH2x2>.<SerDes>)
Port 1: 100G (4 × 25.78)	0	7 (3.1)	6 (3.0)
	1	3 (1.1)	2 (1.0)
	2	4 (2.0)	4 (2.0)
	3	0 (0.0)	0 (0.0)
Port 2: 200G (4 × 53.125)	0	5 (2.1)	5 (2.1)
	1	6 (3.0)	7 (3.1)
	2	1 (0.1)	1 (0.1)
	3	2 (1.0)	3 (1.1)

3.1.3.2.2 Interlaken Lane Mapping

As with lane mapping for ETH and FlexE ports, TX and RX lane swapping is allowed when ILKN ports are involved, but the TX SerDes and RX SerDes must be in the same BH2x2 core.

The following additional lane-mapping rules apply to ILKN ports:

- When a BH2x2 module uses SerDes for ILKN, the other SerDes in the BH2x2 can be used only for ILKN (it cannot be used for ETH or FlexE).
- When a TX SerDes is used for ILKN, the same RX SerDes should be part of the same ILKN interface.

3.1.3.3 400GbE Port

The BCM88830 device supports standard 400GbE according to IEEE 802.3.

The 400GbE port supports the following interfaces:

- 400GAUI-8 (chip-to-chip IEEE 802.3 Annex 120D and chip-to-module IEEE 802.3 Annex 120E)
- 400GBASE-KR8 (400GAUI-8 with a KR interface as defined in IEEE 802.3cd Clause 137)
- 400GBASE-CR8 (400GAUI-8 with a CR interface as defined in IEEE 802.3cd Clause 136)

When using the 400GbE port, Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3 Clause 119, RS(544,514).

3.1.3.4 200GbE Port

The BCM88830 device supports standard 200GbE according to IEEE 802.3 and IEEE 802.3cd.

The 200GbE port supports the following interfaces:

- 200GAUI-4 (chip-to-chip IEEE 802.3 Annex 120D and chip-to-module IEEE 802.3 Annex 120E)
- 200GBASE-KR4 (IEEE 802.3cd Clause 137)
- 200GBASE-CR4 (IEEE 802.3cd Clause 136)

When using the 200GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3 Clause 119, RS(544,514).

3.1.3.5 100GbE Port

3.1.3.5.1 100GbE over Two Lanes

The BCM88830 device supports standard 100GbE according to IEEE 802.3cd.

The 100GbE port supports the following interfaces:

- 100GAUI-2 (chip-to-chip IEEE 802.3cd Annex 135F and chip-to-module IEEE 802.3cd Annex 135G)
- 100GBASE-KR2 (IEEE 802.3cd Clause 137)
- 100GBASE-CR2 (IEEE 802.3cd Clause 136)
- CAUI-2, which is the IEEE 802.3 (CAUI-4) port bit-muxed to two lanes (chip-to-chip and chip-to-module).

When using the 100GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3 Clause 91, both RS(528,514) and RS(544,514).

3.1.3.5.2 100GbE over Four Lanes

The BCM88830 device supports standard 100GbE according to IEEE 802.3.

The 100GbE port supports the following interfaces:

- CAUI-4 (chip-to-chip IEEE 802.3 Annex 83D and chip-to-module IEEE 802.3 Annex 83E)
- 100GBASE-KR4 (IEEE 802.3 Clause 93)
- 100GBASE-CR4 (IEEE 802.3 Clause 92)
- 100GAUI-4 (chip-to-chip IEEE 802.3cd Annex 135D and chip-to-module IEEE 802.3cd Annex 135E)

When using the 100GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3 Clause 91, both RS(528,514) and RS(544,514).

3.1.3.6 50GbE Port

3.1.3.6.1 50GbE over One Lane

The BCM88830 supports 50GbE according to IEEE 802.3cd.

The 50GbE port supports the following interfaces:

- 50GAUI-1 (chip-to-chip IEEE 802.3cd Annex 135F and chip-to-module IEEE 802.3cd Annex 135G)
- 50GBASE-KR (IEEE 802.3cd Clause 137)
- 50GBASE-CR (IEEE 802.3cd Clause 136)

When using the 50GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3cd Clause 134 RS(544,514).

3.1.3.6.2 50GbE over Two Lanes

The BCM88830 supports 50GbE according to IEEE 802.3cd.

The 50GbE port supports the following interfaces:

- LAUI-2 (chip-to-chip IEEE 802.3cd Annex 135B and chip-to-module 802.3cd Annex 135C)
- 50GBASE-KR2 (Ethernet consortium 50GbE with a KR interface as defined in IEEE 802.3 Clause 93)
- 50GBASE-CR2 (Ethernet consortium 50GbE with a CR interface as defined in IEEE 802.3 Clause 92)
- 50GAUI-2 (chip-to-chip IEEE 802.3cd Annex 135D and chip-to-module IEEE 802.3cd Annex 135E)

When using the 50GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3cd Clause 134, RS(544,514), or Clause 91, RS(528,514).

3.1.3.7 40GbE Port

3.1.3.7.1 40GbE over Four Lanes

The BCM88830 supports standard 40GbE according to IEEE 802.3.

The 40GbE ports support the following interfaces:

- XLAUI (IEEE 802.3 Annex 83A)
- 40GBASE-KR4 (IEEE 802.3 Clause 84)
- 40GBASE-CR4 (IEEE 802.3 Clause 85)
- XLPPI (IEEE 802.3 Annex 86A)

When using the 40GbE port in four-lane mode, an optional FEC is supported. The FEC is compliant to IEEE 802.3 Clause 74.

3.1.3.8 25GbE Port

The BCM88830 supports 25GbE according to IEEE 802.3.

The 25GbE ports support the following interfaces:
- 25GAUI (chip-to-chip IEEE 802.3 Annex 109A and chip-to-module IEEE 802.3 Annex 109B)
- 25GBASE-KR/25GBASE-KR-S (IEEE 802.3 Clause 111)
- 25GBASE-CR/25GBASE-CR-S (IEEE 802.3 Clause 110)

When using the 25GbE port, an optional FEC is supported. The FEC can be either IEEE 802.3 Clause 108, RS(528, 514), or IEEE 802.3 Clause 74 FEC.

3.1.3.9 10GbE Port

The BCM88830 supports 10GbE according to IEEE 802.3.

The 10GbE ports support the following interfaces:
- XFI or SFI for direct connect to optical module.[1]
- 10GBASE-KR (IEEE 802.3 Clause 72).
- Direct attached cable (DAC).

When using the 10GbE port with the KR interface, an optional FEC is supported. The FEC is compliant to IEEE 802.3 Clause 74.

3.1.4 FlexE

The BCM88830 includes a FlexE core with the following features:
- Full support of the OIF FlexE standard versions 1.1, 2.0, and 2.1.
- Up to 1600 Gb/s of total FlexE traffic.
- Up to 16 FlexE groups.
- 50G, 100G, 200G, and 400G PHY rates and 53.125G, 26.5625G, and 25.78125G SerDes rates.
- Bonding of up to 16 PHYs in a group.
- Up to 320 FlexE clients, with client bandwidth granularity of 5 Gb/s, 1.25 Gb/s, or 1 Gb/s.
- Dynamic configuration of adding and removing FlexE groups and clients.
- Insertion and extraction of FlexE overhead.
- IEEE1588 over FlexE overhead.
- OAM insertion, extraction, and monitoring.
- 1+1 and 1:1 protection.
- Bonding of Ethernet PHYs.
- Sub-rating of Ethernet PHYs.
- Accurate time synchronization.
- Layer 1 switching between FlexE clients to FlexE clients.
- Layer 1 switching between FlexE clients to Ethernet ports.
- Layer 1 switching between clients on different BCM88830 devices (using a DNX fabric).
- Switching at Layer 2 through Layer 4 of FlexE and Ethernet traffic.

1. Supported: SR (limiting), LR (limiting), ER (limiting).
   Not supported: ZR (limiting), ZR (linear), LRM (linear), DWDM (linear)

3.1.5 Interlaken

The BCM88830 has one Interlaken (ILKN) core.

The BCM88830 ILKN core supports SerDes rates of up to 25.78125G. For the defined ILKN rates and specifications, see Section 3.1.5.1, Interlaken SerDes Supported Rates and Electrical Standards.

The ILKN core can be configured to operate as either a single interface (ILKN_0, up to 24 lanes) or as two interfaces (ILKN_0 and ILKN_1, each up to 12 lanes). The ILKN core shares SerDes with PM50-0, PM50-1, and PM50-2.

For information about PM assignment to ILKN cores, see Table 1, BCM88830 NIF SerDes Mapping. When making assignments, use the following guidelines:

- If the RX (or TX) of a specific physical SerDes is used for ILKN, the TX (or RX) of the same SerDes should go to the same ILKN interface.
- For a logical ILKN lane, RX SerDes and TX SerDes should be on the same BH2x2.

3.1.5.1 Interlaken SerDes Supported Rates and Electrical Standards

The ILKN interface is targeted to comply with the electrical specifications of the standards as listed in the following table.

Table 5: ILKN Supported Rates and Electrical Specifications Standards

SerDes Rate (Gb/s)	SerDes Mode	Standard Electrical Specifications
25.78125	NRZ	25GBASE-KR-S IEEE 802.3 Clause 111
		CAUI-4 C2C: IEEE 802.3 Annex 83D
		CAUI-4 C2M: IEEE 802.3 Annex 83E
25.0	NRZ	25GBASE-KR-S IEEE 802.3 Clause 111[a]
		CAUI-4 C2C: IEEE 802.3 Annex 83D[a]
12.5	NRZ	10G XFI: XFI+ (FC-PI-3)[a]
10.3125	NRZ	10GBASE-KR IEEE 802.3 Clause 72
		10G XFI: XFI+ (FC-PI-3)

a. Scaled to the appropriate rate.

3.1.5.2 Interlaken Receive Burst Rules

Packets are transmitted across the Interlaken interface in bursts. The BCM88830 requires that burst sizes and burst intervals (Interlaken BurstShort) conform to certain rules.

The BCM88830 Interlaken receive supports both burst interleaving and full packet mode. If the peer device is configured to burst interleaving, assign a separate ingress reassembly context for each active channel.

Receive (into the BCM88830) burst interleaving rules are as follows:

- Supported BurstMax size is 256B.
- Start-of-packet (SOP) bursts should be 192B or larger.
- Bursts that are not end-of-packet (EOP) bursts may be either 128B, 192B, or 256B.
- EOP bursts may be any size (up to the configured BurstMax).
- BurstShort (the minimum interval between burst control words) should be at least 64B.

3.1.5.3 Interlaken Transmit Burst Rules

When the StrataDNX TM is operational (stand-alone or central switch mode), the BCM88830 ILKN TX supports only full-packet mode (burst-interleaving occurs only when TDM packets preempt data packets).

When transmitting across an Interlaken interface, the BCM88830 supports configurations consistent with the following:

- BurstShort (minimum interval between burst control words):
  - Configuration is from 64B to 256B in increments of 32B.
- BurstMax options:
  - BurstMax = 256B, normal scheduling:
    - Non-EOP bursts are 256B.
    - EOP burst can be from 1B to 256B.
  - BurstMax = 256B, enhanced scheduling:
    - Configurable BurstMin of 64B or 128B.
    - Non-EOP bursts are 256B.
    - Penultimate burst when BurstMin is 128B: 128B or 256B.
    - Penultimate burst when BurstMin is 64B: 192B or 256B.
    - EOP bursts are from 64B to 256B.

3.1.5.4 Interlaken In-Band Flow Control

Each Interlaken interface supports in-band flow control according to the Interlaken protocol definition.

The flow-control (FC) information is carried over the control words sent across the interface. Each control word includes a 16-bit flow-control field and a reset calendar bit. Each flow-control bit indicates the flow-control status (ON/OFF) of a specific Interlaken calendar channel. The BCM88830 supports a configurable calendar length between 16 to 256 channels (16, 32, 64, 128, and 256).

The BCM88830 supports two options for link level flow control (LLFC) mapping:

- Map the LLFC to flow control calendar channel #0.
- Map the LLFC to the first flow-control calendar channel in every control word (that is, entries 0, 16, 32, and so on). This option is useful for faster reaction times for LLFC, at the expense of flow-control channels.

The BCM88830 is flexible in flow-control processing, and each calendar entry can be mapped to one of the following flow-control reaction points:

- Link level (mapped to Interlaken NIF port)
- Channel level (mapped to OTM port)
- Egress queue pair level

Flow-control generation (flow-control transmission) – The BCM88830 can assign each calendar entry with flow control information or indications that may represent the following:

- Status of Interlaken port receive buffer (useful for link level).
- Status of the global resources (in other words, DRAM buffers).
- Status of a virtual-statistics queue – May be programmed to generate flow control per Interlaken channel but enables more fine-grain flow-control indications; for example, per port and traffic class, per flow, and so on.

3.2 Time Sensitive Networking

The device supports the IEEE Time-Sensitive Networking (TSN) standards. The TSN standards specify methods to provide the appropriate QoS for time-sensitive applications in converged networks containing both time-sensitive and non-time-sensitive traffic.

TSN methods are supported only for Ethernet ports. The TSN standards use the concept of *stream* for traffic flows of time-sensitive applications.

The device supports the following TSN standards:

- 802.1AS-Rev – Timing and synchronization
- 802.1Qav – Forwarding and queuing enhancements for time sensitive streams (FQTSS)
- 802.1Qcr – Asynchronous traffic shaping (ATS)
- 802.1Qbu – Frame preemption
- 802.3br – Interspersing express traffic (IES)
- 802.1Qbv – Enhancements for scheduled traffic
- 802.1Qci – Per-stream filtering and policing (PSFP)
- 802.1Qch – Cyclic queuing and forwarding (CQF)

For more information, refer to the *BCM88830 Traffic Manager Architecture* design guide (88830-DG1xx).

3.3 MACsec and IPsec

The BCM88830 supports full wire-speed integrated MACsec and IPsec on all network ports. MACsec and IPsec are supported for all port rates available in the BCM88830, including 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE, and 400GbE. MACsec and IPsec are also supported for FlexE clients at any rate from 1GbE to 400GbE.

The BCM88830 MACsec capabilities are as follows:

- Crypto algorithms: AES-128-GCM and AES-256-GCM
- IEEE 802.1AE MACsec implementation, including the following standards:
  - IEEE Std 802.1AEbn-2011 – 256-bit key
  - IEEE Std 802.1AEbw-2013 – XPN counter mode
- Secure channels (SCs): 1K
- MACsec secure associations (SAs): 1K TX + 2K RX
- MACsec supported tunneling structures (termination and encapsulation) include the following:
  - Ethernet MAC + up to two VLAN tags (IEEE 802.1AE-2006, IEEE 802.1AEcg-2007)
  - IPv4/IPv6 over Ethernet
  - TCP/UDP over IPv4/IPv6 over Ethernet
  - VXLAN over IPv4/IPv6 over Ethernet
  - MPLS, up to 14-label encryption and up to 4-label decryption

The BCM88830 IPsec capabilities are as follows:

- Crypto algorithms: AES-128-GCM and AES-256-GCM only
  - No support for AES-CBC, DES, 3DES encryption
  - No support for SHA-1, SHA-256, SHA512 authentication HMAC
- Tunnel mode IPsec (ESP)
- SAs: 1K TX + 1K RX
- 1280 entries in the SC TCAM map table to allow seamless IPsec secure association switchover
- IPsec-supported tunneling structures (termination and encapsulation) include the following:
  - IPsec over IPv4/IPv6 transport
  - IPsec-GRE over IPv4-GRE and IPv6-GRE transport
  - IPsec over MPLS transport, up to 12-label encryption and up to 4-label decryption

3.4 Synchronous Ethernet

The BCM88830 supports Synchronous Ethernet (SyncE) applications. The support includes two functions: controlling the transmit clock of network ports, and recovering a clock from a network port.

3.4.1 Transmit Clock

The transmit clock of each SerDes is locked to an external reference clock driving the NIF_[3:0]_REFCLK_P/N input pins.

By connecting the system transmit clock to the NIF_[3:0]_REFCLK_P/N inputs, you can control the transmit clock of the SerDes.

3.4.2 Recovered Clock

The BCM88830 provides up to two recovered clocks that may be used as reference clocks for an external synchronization unit. The source for the recovered clocks can be any of the NIF SerDes configured as an Ethernet port. The BCM88830 drives two recovered clocks (SYNCE[1:0]_CLK_OUT) and a valid indication per clock (SYNCE[1:0]_CLK_OUT_VALID).

NOTE: Clock recovery is supported for a NIF interface configured as an Ethernet or FlexE port. It is not supported for fabric or Interlaken ports.

The valid indication is asserted when the recovered clock is synchronized to the selected SerDes RX signal and can be used for system synchronization. The valid indication is based on a PCS lock and a linkup indication.

Each of the recovered clocks works as either a normal clock or a squelched clock. In normal clock mode, the CLK_OUT is the recovered clock of the selected SerDes. In squelched mode, the CLK_OUT halts if the RX of the selected link is not synced.

For multilane ports (for example, 40GbE or 100GbE), the recovered clock is derived from the first SerDes of the relevant port, and the valid signal is according to the link up status of the entire port.

The recovered clock frequency is 25 MHz.

A fractional divider is used for generating an average clock of 25 MHz.

The following example describes how the average output frequency of 25 MHz is generated for a 100GbE port (4 × 25.78125 Gb/s).

The 25.78125 GHz is divided by 40, and the fractional divider, over 32 clock cycles, uses 7 clock cycles of a 25 divider [(25.78125 ÷ 40) ÷ 25] and 25 clock cycles of a 26 divider [(25.78125 ÷ 40) ÷ 26], as shown in the following equation.

$$\frac{25.78125\ \text{GHz}}{40} \div \frac{(7 \times 25) + (25 \times 26)}{32} = 25\ \text{MHz}$$

Similarly:

- A fractional divider of 26.5625 GHz uses 14 clock cycles of a 26 divider and 18 clock cycles of a 27 divider.
- A fractional divider of 20.625 GHz uses 12 clock cycles of a 20 divider and 20 clock cycles of a 21 divider.

NOTE: An external jitter attenuator device is required to clean the recovered clock before using it as a reference for the rest of the system.

3.5 IEEE 1588

The BCM88830 is a highly integrated device with many hardware hooks for designs that require network time synchronization with improved timestamping accuracy on a nanosecond scale. The following features make the device ideally suited for time synchronization applications that comply with IEEE 1588.

- Supported modes:
  - E2E and P2P transparent clock (TC).
  - Boundary clock (BC).
  - TC + OC timeReceiver, BC + OC timeReceiver.
- One-step clock features:
  - On-the-fly egress packet modification, including UDP checksum update and CRC update.
  - All modifications to the correction field are handled in hardware.
  - Very short residence time.
  - All packets timestamped on ingress.
  - Uses switch-packet processing engines to identify IEEE 1588 packets.
- Two-step features:
  - Egress timestamps are stored in per-port FIFO, along with IEEE 1588 sequence number.
  - The CPU indicates which packets should generate a timestamp on egress.
  - All packets are timestamped on ingress.
  - Uses switch packet processing engines to identify IEEE 1588 packets and trap to CPU.
- Synchronizable timestamp counter:
  - Can be phase-locked to external source.
  - BroadSync® (timecode + event clock) interface.
  - Broadcom PHY sync interface.
  - Timestamped GPIOs.
- Frequency synthesizer:
  - Additional clock divider: 10 MHz + 1 p/s.
  - Low jitter.

NOTE: PTP and IEEE 1588 functionality is supported over network (NIF) Ethernet and FlexE ports only. Timestamping is not supported over fabric and Interlaken interfaces.

3.5.1 BroadSync External Interfaces

The BroadSync block provides the following external interfaces for providing timing information to off-chip devices or for retrieving timing information from external devices:

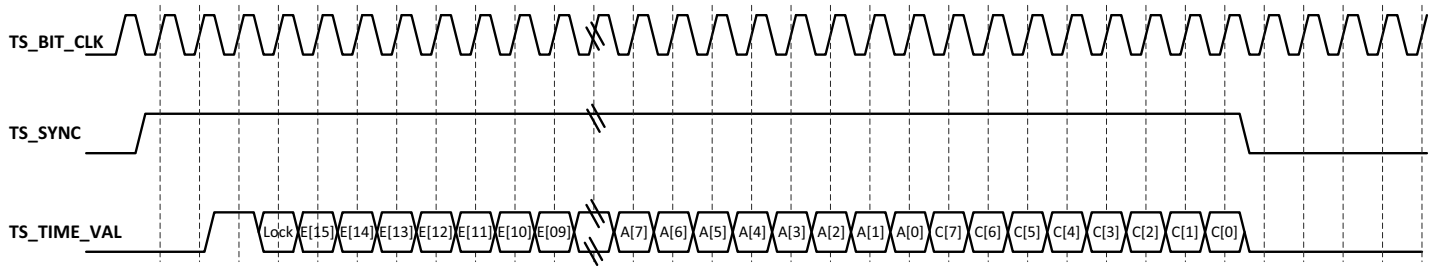
- Reference clock (input)
- External Sync 1 (input or output)
- External Sync 2 (input or output)
- Three-pin BroadSync interface (input or output):
  - TS_BIT_CLK
  - TS_SYNC
  - TS_TIME_VAL

The reference clock input is used for the clocking of all of the logic in the BroadSync block. The BroadSync block operates on a separate clock domain than the rest of the switch logic. Drive the reference clock input from a low-jitter source to ensure that all time-related functions are accurate.

Use the External Sync 1 and 2 signals as either inputs or outputs. When the signals are used as inputs, a rising edge on the signal can sample the current value of the internal timer, which can then be retrieved by the CPU. When these signals are used as outputs, the signal can be programmed to toggle based on a configurable interval.

The BroadSync interface is configured through the CMIC_BS_CONFIG register and is composed of three signals: the clock, the heartbeat, and the time code. The BroadSync interface can be configured to operate as either a timeTransmitter (output) or timeReceiver (input). The interface clocks out or takes in serial data as shown in the following figure.

Figure 6: BroadSync Interface I/O



When the BroadSync interface is operating in timeReceiver mode, an external device clocks a time code into the BCM88830. External hardware provides the TS_BIT_CLK, TS_SYNC, and TS_TIME_VAL signals. During each heartbeat period, the external hardware shifts in a time code value, which consists of the following:

- Start bit
- Lock bit
- 16-bit epoch
- 32-bit seconds
- 2-bit zero
- 30-bit nanoseconds
- 8-bit accuracy
- CRC8 (covers all bits from LOCK to ACCURACY[0])

The time value shifted in corresponds to the time of the most recent rising edge of the heartbeat signal. All of the bits clocked in from the time code are stored in the CMIC_BS_INPUT_TIME[0:2] registers. Additionally, the received CRC8 is compared against the computed CRC8, and the result of the comparison is present in the CHECKSUM_ERROR field in the CMIC_BS_INPUT_TIME_2 register.

The internal time value is calibrated to the external signals through the following process:

1. The rising edge of TS_SYNC samples the device's internal free-running clock value.
2. The sampled free-running clock value is compared to the time value subsequently shifted in using the TS_TIME_VAL signal.
3. These pairs of values (shifted-in time and sampled free-running time) are provided to the CPU on an occasional basis.
4. The differences and rates of change of the differences of the two time bases derive a drift value.
5. The computed drift value corrects the internal time counter.

When the BroadSync interface is operating in timeTransmitter mode, the interface drives a time code to external devices. How frequently a new time code is clocked out depends on how often the heartbeat signal goes high. Configure the heartbeat signal toggling frequency through the CMIC_BS_HEARTBEAT_CTRL register. When the heartbeat goes high, the contents of the CMIC_BS_OUTPUT_TIME memory are clocked out. The BCM88830 automatically computes and appends the correct CRC8 value immediately after the 8-bit accuracy field is clocked out. The TS_BIT_CLK that clocked out the time code is synthesized from the BroadSync Clock domain.

The BCM88830 can optionally synthesize the TS_BIT_CLK from a highly accurate internal PLL. The PLL generates an extremely low-jitter clock that is ITU-T G.824 and ITU-T G.823 compliant.

3.6 Fabric Interface

The fabric block integrates 64 SerDes links. The SerDes core is an octal (x8) lane 53.125-Gb/s PAM-4 or 25.78125-Gb/s NRZ and is suitable for optical and backplane applications. The SerDes core supports data rates from 23.0 Gb/s to 25.78125 Gb/s in NRZ (backward-compatible with the BCM88770) and a data rate of up to 53.125 Gb/s in PAM-4 mode. Each lane can be configured independently to run in PAM-4 or NRZ modes. When mixing rates in same core, the supported rates per lane can be one of the following: 50 Gb/s or 25 Gb/s.

NOTE: Unlike the previous 16-nm devices, the eight-lane fabric core of the BCM88830 includes only one PLL per core.

SerDes supports a built-in PRBS functionality. PRBS is also supported on the fabric MAC layer per lane.

The following table lists the supported SerDes rates as well as the associated electrical specification standards.

Table 6: Fabric Supported Rates and the Electrical Specifications Standards

SerDes Rate (Gb/s)	SerDes Mode	Standard Electrical Specifications
53.125	PAM-4	50GBASE-CR: IEEE 802.3cd Clause 136
		50GBASE-KR: IEEE 802.3cd Clause 137
		50GAUI-1 C2C: IEEE 802.3cd Annex 135F
		50GAUI-1 C2M: IEEE 802.3cd Annex 135G
50	PAM-4	50GBASE-KR: IEEE 802.3cd Clause 137[a]
25.78125	NRZ	100GBASE-CR4: IEEE 802.3 Clause 92
		100GBASE-KR4: IEEE 802.3 Clause 93
		CAUI-4 C2C: IEEE 802.3 Annex 83D
		CAUI-4 C2M: IEEE 802.3 Annex 83E
25	NRZ	100GBASE-KR4: IEEE 802.3 Clause 93[a]
23	NRZ	100GBASE-KR4: IEEE 802.3 Clause 93[a]

a. Scaled to the appropriate rate.

3.6.1 PCS Layer Line Coding

Each fabric link supports one of the following line coding options:

- 64b/66b encoding
- 25G Reed-Solomon FEC
- Low Latency 25G Reed-Solomon FEC
- 50G Reed-Solomon FEC
- Low Latency 50G Reed-Solomon FEC

3.6.1.1 64b/66b Encoding

The 64b/66b line coding is based on the standard 10GbE 64b/66b coding (IEEE 802.3 Clause 49). KR-FEC is not supported.

The effective bandwidth of 64b/66b is ~97% (64b/66b) of the SerDes rate.

3.6.1.2 25G Reed-Solomon FEC (RS-FEC)

The RS-FEC is based on the Reed-Solomon error correction code and can be configured on a per-link basis.

For 25-Gb/s links, the BCM88830 supports RS (206, 196, t=5) coding using 10-bit symbols. This means that each 2060-bit frame consists of 1960 bits of data and 100 bits RS Syndrome, which the decoder uses to correct errors.

The selected code can correct any five symbols in the frame. This RS code corrects any single-error burst of 41 bits per RS frame, and up to 50 bits of error burst if it spans no more than five symbols.

Out of the 1960 data bits of the RS-FEC frame, the BCM88830 uses only 1950 bits for real data and 10 bits as overhead. The effective bandwidth of a link running RS-FEC is ~93.2% of the link rate (64/65 × 1950/2060).

The 25G RS-FEC decoder on the receive side adds a delay equivalent to ~1.5 RS-FEC frame time (the computation logic takes ~0.5 FEC frame time). For example, RS-FEC adds a latency of ~130 ns on 23-Gb/s links (~116 ns on 25.78125-Gb/s links).

The RS-FEC supports the option to indicate uncorrectable RS-FEC frames. When enabled, the RX MAC drops all cells that are part of an uncorrectable RS-FEC frame. Enabling this indication adds one additional RS-FEC frame time delay (total of ~2.5 RS-FEC frame time). For example, RS-FEC with error indication adds a latency of ~220 ns on 23-Gb/s links (~196 ns on 25.78125-Gb/s links).

3.6.1.3 Low Latency 25G Reed-Solomon FEC (LL 25G RS-FEC)

The BCM88830 supports a lower-latency version of the RS-FEC (for 25-Gb/s links only). The LL 25G RS-FEC is based on the same 25G RS(206, 196, t=5) coding using 10-bit symbols; however, only half the data is transmitted. The LL 25G RS-FEC code is able to correct any five symbols in the frame, which is the same as 25G RS-FEC.

The LL 25G RS-FEC transmitted frame is 1080 bits (975 data bits, 5 overhead bits, and 100 RS Syndrome bits). The effective bandwidth of a link running LL 25G RS-FEC is ~88.9% of the link rate (64/65 × 975/1080).

The LL 25G RS-FEC has a delay equivalent to ~2 LL 25G RS-FEC frame time (computation logic takes ~1 LL 25G RS-FEC frame time) and ~3 LL 25G RS-FEC frame time when the uncorrectable error indication is enabled. For example, LL 25G RS-FEC adds a latency of ~84 ns on 23-Gb/s links without uncorrectable error indication (~76 ns on 25.78125-Gb/s links) and ~131 ns on 23-Gb/s links when uncorrectable error indication is enabled (~118 ns on 25.78125-Gb/s links).

3.6.1.4 50G Reed-Solomon FEC (RS-FEC)

For 50-Gb/s links, the BCM88830 supports RS (545, 515, t=15) coding using 10-bit symbols. This means that each 5450-bit frame consists of 5150 bits of data and 300 bits RS Syndrome, which the decoder uses to correct errors.

This code is able to correct any 15 symbols in the frame. This RS code can correct any single error burst of 141 bits per RS frame, and up to 150 bits of error burst if it spans no more than 15 symbols.

Out of the 5150 data bits of the RS-FEC frame, the BCM88830 uses only 5056 bits for real data. The effective bandwidth of a link running RS-FEC is ~92.7% of the link rate (5056/5450).

The 50-Gb/s RS-FEC decoder on the receive side adds a delay equivalent to ~1.8 RS-FEC frame time (the computation logic takes ~0.8 FEC frame time). For example, RS-FEC adds a latency of ~185 ns on 53.125-Gb/s links.

3.6.1.5 Low Latency 50G Reed-Solomon FEC (LL 50G RS-FEC)

The BCM88830 supports a lower-latency version of the 50G RS-FEC. The LL 50G RS-FEC is based on the same 50G RS(545, 515, t=15) coding using 10-bit symbols; however, only half the data is transmitted. The LL 50G RS-FEC code is able to correct any 15 symbols in the frame, which is the same as 50G RS-FEC.

The LL 50G RS-FEC transmitted frame is 3040 bits (2688 data bits). The effective bandwidth of a link running LL 50G RS-FEC is ~88.4% of the link rate. The LL 50G RS-FEC has a delay equivalent to ~2 LL 50G RS-FEC frame time (computation logic takes ~1 LL 50G RS-FEC frame time) and ~3 LL 50G RS-FEC frame time when the uncorrectable error indication is enabled.

3.6.1.6 Line Coding Overheads and FEC Latency

Table 7 and Table 8 show technical specifications for the line coding options.

Table 7: Line Coding Overheads

Code	Block Length (Bits)	Data Length (Bits)	Utilization	SerDes Rate (Gb/s)	Encoded SerDes Rate (Gb/s)
64b/66b	66	64	96.97%	23	22.3
25G RS-FEC	2060	1920	93.20%	23	21.43
Low Latency 25G RS FEC	1080	975	88.9%	23	20.45
64b/66b	66	64	96.97%	25.78125	25
25G RS-FEC	2060	1920	93.20%	25.78125	24
Low Latency 25G RS FEC	1080	975	88.9%	25.78125	22.92
50G RS-FEC	5450	5150	92.7%	50	46.35
50G RS-FEC	5450	5150	92.7%	53.125	49.24
Low Latency 50G RS FEC	3040	2688	88.4%	50	44.21
Low Latency 50G RS FEC	3040	2688	88.4%	53.125	46.97

Table 8: FEC Latency

Code	Frame Size (Bits)	SerDes Rate (Gb/s)	Frame Transmit (ns)	Total Without Error Marking (ns)	Total With Error Marking (ns)
25G RS-FEC	2060	23	90	130	220
Low Latency 25G RS FEC	1080	23	47	84	131
25G RS-FEC	2060	25.78125	80	116	196
Low Latency 25G RS FEC	1080	25.78125	42	76	118
50G RS-FEC	5450	50	109	198	307
50G RS-FEC	5450	53.125	102.6	184.6	287.2

3.6.2 Fabric SerDes Connectivity

3.6.2.1 Fabric SerDes Cable Length and Link Delay

When a link-input FIFO is building up, link-level flow control (LLFC) is asserted to prevent input FIFO overflow. When the LLFC is deasserted, the input FIFO should have enough data to prevent the FIFO from getting empty, resulting in potential performance loss. The LLFC assertion and deassertion threshold must be able to handle the LLFC delivery time as well as data in-flight, which depends on various parameters. The significant parameters are the PCS line encoding, the cell size, and the cable length. The LLFC settings depend on the size of the input-link FIFO:

- In single-pipe mode, the input-link FIFO size is 512 entries of 128 bytes per link (using the memory from the other pipes).
- In two-pipe mode in the BCM88830, the input-link FIFO size can be set to 256 entries of 128 bytes.

The following table describes the cable length limitations when the BCM88830 requires generating LLFC indication, which is calculated according to the BCM88830 input link FIFO size. The LLFC cable length limitations of a link partner device must be calculated separately and may be more or less than the data presented in this table

NOTE:

- Minimize the cable length in the system.
- Propagation delay above the maximum value requires special approval. (The propagation delay is from device ball to device ball and is the sum of all the elements in the link path.)
- Minimize the propagation delay variance in the system.
- A variance (skew) between links in the system that is greater than 50% of the maximum-allowed propagation delay, requires special approval.

Table 9: Maximum Link Propagation Delay and Skew

Number of Fabric Pipes	Maximum Link Rate (Gb/s)	Uncorrectable Error Marking	Peer (Link Partner) Device	Maximum Link Propagation Delay (ns)	Maximum Allowed Skew Between Links (ns)	Fiber-Optic Cable Length (Meters)
Single	53.125	Any	Any	500	250	100
Single	50	Any	Any	500	250	100
Single	25.78125	Any	Any	500	250	100
Two	53.125	No	88790 (FE)	350	175	70
Two	53.125	No	88830 (Mesh)	300	150	60
Two	53.125	Yes	88790 (FE)	240	120	48
Two	53.125	Yes	88830 (Mesh)	195	97	39
Two	50	No	88790 (FE)	380	190	76
Two	50	No	88830 (Mesh)	335	167	67
Two	50	Yes	88790 (FE)	270	135	54
Two	50	Yes	88830 (Mesh)	220	110	44
Two	25.78125	Any	Any	500	250	100

3.6.2.2 Fabric SerDes Balancing

The BCM88830 fabric interface, which supports 64 SerDes, has two fabric engines. Each fabric engine serves half of the 64 fabric SerDes.

The following table shows the association between the fabric engines and the SerDes.

Table 10: Fabric Engine and SerDes Association

Fabric Engine	Associated SerDes
Fabric Engine 0	0 to 31
Fabric Engine 1	32 to 63

If the board or the system does not use all of the fabric lanes for fabric connectivity, evenly spread the used lanes between the two fabric engines.

Balancing the lanes among the two fabric engines is not a requirement, but this implementation is recommended as long as there is no additional cost or complexity involved in the board and system design.

3.7 Statistics Interface

The statistics interface is an event-driven interface through which statistics are pushed out. Statistics records are continuously reported at a maximum rate of one record per clock in ingress and egress. The BCM88830 supports one of the following global configurable options:

- Queue-Size – The statistics interface reports the queue size of ingress enqueue actions and ingress dequeue actions. This mode can be used to build an image of queue sizes, infer congestion, and enable congestion management by an ingress PP.
- Billing – The statistics interface reports ingress received packets and egress transmitted packets. Packets are tagged with information that maps into counters at the external statistic processing device.
- Ingress-Enqueue/Dequeue – In this mode, the statistics interface reports per each ingress packet enqueued and dequeued. Packets are tagged with information that maps into counters at the external statistic processing device.

The statistics interface has two modes:

- Split mode – This mode uses two statistics interfaces, and each interface is a 200GbE port (or 100GbE port). The BCM88830 splits the egress and ingress statistics reports between the two ports. This is a dedicated mode to connect directly to the Broadcom KBP or TAP. In this mode, each logical counter requires an allocation of two counters in the KBP or TAP.
- Single mode – This mode uses only one statistics interface of up to 400GbE. This interface serves the ingress and egress directions. This mode can also handle different record sizes for the ingress and the egress.

The external statistics processor can be Broadcom KBP or TAP devices, or a custom FPGA. When connecting to the Broadcom KBP or TAP as an external statistics processor, configure the statistics interface to split mode.

The statistics interface uses Ethernet ports from the NIF, PM50-3. A mix of statistics interface ports and NIF Ethernet/FlexE ports on PM50-3 is not supported.

NOTE: Only the TX direction of the Ethernet port is used for the statistics interface. The RX direction is not used for data (statistics records) transfer, and it can be left unconnected. However, connecting the RX direction enables the use of link-training and allows more debug capabilities over the interface.

An Ethernet-like MAC is used to send statistics packets and is made up of the following:

- Standard Ethernet 8-byte preamble.
- 32b FCS, which is the same as standard Ethernet.
- Average interpacket gap (IPG) of 12B.

3.8 HBM Packet Buffers

The BCM88830 integrates an HBM (4H) Gen2 module for a total of 4 GB of deep buffering. The HBM technology integration enables low-power and high-performance memory access.

3.9 CPU Interface

The Broadcom iProc block provides an interface between the host CPU and the internal registers and tables within the switch device, enabling complete management of the switch.

The iProc block is made up of the following components:

- PCIe x4 lane Gen3 interface at up to 8 Gb/s:
  - Compatible with x1 or x2 lane PCIe.
  - Compatible with PCIe Gen1 at 2.5 Gb/s or Gen2 at 5 Gb/s.
- BSC (I^2C-compatible) 2-line interface.
  - For basic debug and register access (PCIe only).
  - PCIe QSPI flash programming.
  - Loading code for heating when an industrial device is powered-up at a low ambient temperature (not supported by the current SDK).
- Microcontroller subsystem:
  - Includes four Arm Cortex-R5 microcontrollers.
  - Runs at 875 MHz (independent of core clock).
  - 16-KB I-Cache, 16-KB D-Cache for each microcontroller core.
  - 128-KB I-Tightly coupled memory, 128-KB D-tightly coupled memory for each microcontroller core.
  - 4-MB internal system memory.
- MIIM interface:
  - MDIO compatible interface.
- LED interface.
- SBUS DMA: Enables reading and writing BCM88830 tables directly from and to host memory using DMA.
- FIFO DMA.
- Packet TX/RX DMA.
- Remote CPU over network or fabric interface.
- Miscellaneous (endian order, reset controls).

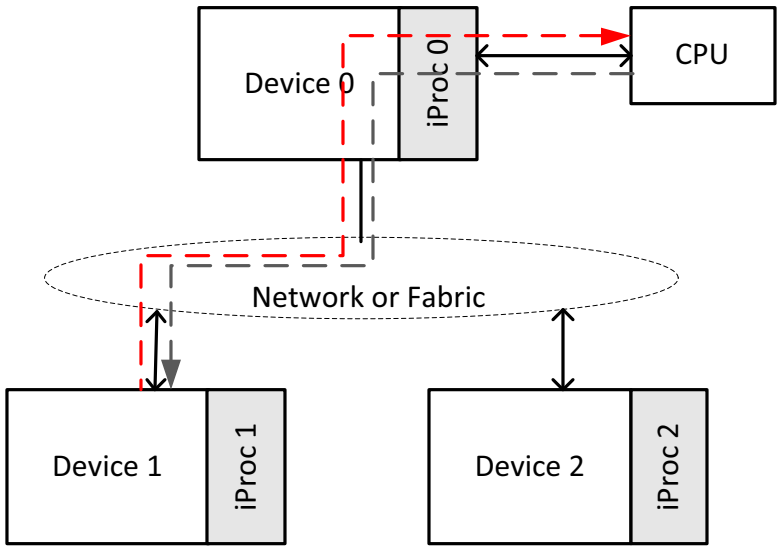
3.9.1 Remote CPU Support

The BCM88830 can be programmed from a remote CPU after initialization. Upon power-up, the device must be initialized using the PCIe interface. After the device has been initialized, the following functions are supported:

- iProc register access
- Generating remote CPU (RCPU) packets when interrupts are triggered
- SCHAN register access
- SCHAN table access

The BCM88830 can operate in a system that is managed by a remote CPU. The CMIC communicates with the remote CPU through Ethernet packets with a special EtherType. These packets are referred to as remote CPU packets. The following figure represents a system managed by a remote CPU.

Figure 7: System Managed by Remote CPU



The CPU generates an S-channel operation in Device 1 as follows:

1. The CPU generates an Ethernet packet with MACDA addressed to iProc1 with a special EtherType value reserved for remote CPU packets. The packet is an SCHAN_REQUEST.
2. iProc0 injects this packet into the ingress pipeline of Device 0. The packet is forwarded based on the MAC destination address (MACDA).
3. The packet is received at Device 1 and is forwarded to iProc1.
4. iProc1 interprets the packet and performs the S-channel operation.
5. iProc1 creates a new SCHAN_REPLY packet based on the result of the S-channel operation. This is also an Ethernet packet with MACDA addressed to the CPU with a special EtherType. This packet is injected into the ingress pipeline of Device 1.
6. Device 1 forwards the SCHAN_REPLY packet based on the MACDA, and the packet is sent to Device 0.
7. Device 0 receives the packet and forwards it to iProc0.
8. iProc 0 sends the packet to the CPU.

3.9.2 Remote Packet Operations

Remote packets are those that are sent or received by the iProc without a local CPU (whether internal or external) being involved. The iProc receives a remote packet from the switch egress pipe. The iProc matches this packet and performs some operations based on the packet data. The iProc may then send a packet back to the sender of the original packet.

The remote CPU performs certain SCHAN operations without the local CPU's intervention. This is especially useful in stacks where the primary CPU in the stack may want to perform L2 insert or delete operations. The means for having the CMIC match incoming packets and perform an SCHAN operation is provided. The CMIC may then send a reply packet back to the requesting remote CPU with the SCHAN operation's status and result data.

Although remote CPUs can send arbitrary SCHAN control packets to the device using this mechanism, it does not remove the requirement for a local CPU to configure the switch (either internal or external). The remote CPU SCHAN packets contain control information to match a reply to a request, but higher layer software must be provided to deal with lost packets, whether they are request or reply packets. Some SCHAN operations are potentially destructive in that they cannot easily be replayed if a reply is lost. There is no mechanism provided in this device to deal with such situations.

3.9.3 PCIe Interface

The PCIe interface of the BCM88830 switch conforms to PCIe 3.1 specifications. The BCM88830 supports four lanes of Gen3 PCIe (8G in each direction). No external glue logic is required to support this interface. The protocols and electrical requirements of the PCIe specifications are strictly implemented.

3.9.4 MIIM

The iProc supports the IEEE 802.3 standard MII Management (MIIM) interface. This is a two-wire serial bus controlled by the iProc that allows register access to external PHYs in the system. The two signals for MIIM are MDC (clock) and MDIO (bidirectional data).

The CPU programs the external PHY registers using this interface. The MIIM interface can be configured to support Clause 22 or Clause 45.

The BCM88830 supports 12 MIIM interfaces. Out of the 12 interfaces, four are used for internal modules, and eight can be used by the system for external PHY access.

3.9.5 UART

The BCM88830 has four UART interfaces. UART interfaces are used for debugging software running on the microcontrollers. The UART interfaces can be used for Time-of-Day (ToD) synchronization.

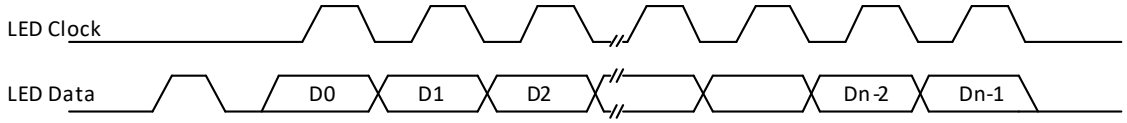
3.9.6 LED Interface

The device provides five serial LED output interfaces. The microcontroller has control of all five interfaces, allowing the user to select which interfaces are used to provide serial LED bitstreams. For example, a user can write code for the microcontroller that collects status for 64 × 50GbE ports, forms a single stream of status bits, and then shifts this out using any one of the LED interfaces.

The output frequency and refresh rate are user-configurable. These parameters are common across all five of the LED status interface outputs.

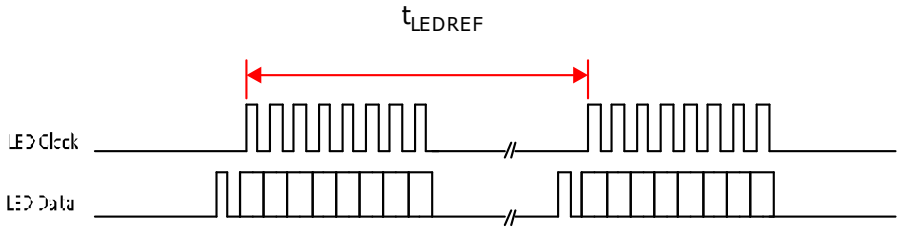
A two-wire (clock and data) LED interface controls system LEDs. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED data bits. The LED data signal is pulsed high at the start of each LED refresh cycle (see Figure 8).

Figure 8: Single LED Refresh Cycle



The LED refresh cycle is repeated periodically to refresh the LEDs (see Figure 9).

Figure 9: LED Refresh Timing



Chapter 4: Pin Signal Description

4.1 Pin List and Pin Map

The BCM88830 pin list and pin map are provided in spreadsheet format on the Broadcom Engineering Support Portal (ESP) collateral distribution site. The spreadsheet serves as the official document containing the device's signal mapping. Refer to the *BCM88830 PinList* file.

4.2 Pin I/O Type Description

The following table lists the conventions that describe the I/O nature of the pins.

Table 11: Signal I/O Type Description

I/O	Description
B	Bidirectional signal
B_{OD}	Open drain bidirectional signal
B_{PD}	Bidirectional signal, with internal pull-down[a]
B_{PU}	Bidirectional signal, with internal pull-up[a]
I	Input signal
I_{PD}	Input signal, with internal pull-down[a]
I_{PU}	Input signal, with internal pull-up[a]
NC	No Connect
O	Output signal
O_{OD}	Open drain output signal
O_{PD}	Output, with internal pull-down[a]
O_{PU}	Output, with internal pull-up[a]

a. Pull-up and pull-down values are minimum = 35 kΩ, maximum = 65 kΩ.

4.3 Pin Description – Grouped by Function

The following table provides an overview of the pins on the BCM88830.

Table 12: Pin List by Function

Signal/Bus Name	Qty.	Type	Tech	Description
Start-Up and Configuration				
CLOCK25	1	I_{PU}	CMOS 1.8V	25-MHz clock. Used for reset, initialization, and monitoring functions.
SYS_RST_N	1	I_{PU}	CMOS 1.8V	Device reset input. Active low. Use external pull down to force 0 when control logic is not initiated.
PCIE_RST_N	1	I_{PU}	CMOS 1.8V	PCIe reset. Active low. Follow the sequence described in Section 5.5, Power-Up, Power-Down, and Reset Sequence. Use external pull down to force 0 while control logic is not initiated.
DISCONNECT	1	I_{PD}	CMOS 1.8V	Disconnect control input. When 1, the device indicates to the fabric link partners to stop sending data to it. This pin can be used for graceful shutdown by external logic that implements early detection of power-down or card removal. ■ 0 – Normal operation. ■ 1 – Graceful shutdown.
INT_N	1	O_{PU}	CMOS 1.8V	CPU interrupt output. Pseudo open drain, active low. Must be pulled up externally to 1.8V.
Power-Up Configuration Word				Power-up configuration (PUC) word. For PUC bus information, see Section 5.5, Power-Up, Power-Down, and Reset Sequence and Section 5.6, Power-Up Configuration Word.
PUC_PARALLEL_SEL	1	I_{PD}	CMOS 1.8V	Select the load mode of the PUC word. ■ 0 – Use serial mode. ■ 1 – Use parallel mode.
PUC_SERIAL_CLK	1	I_{PD}	CMOS 1.8V	When serial mode is selected, used as clock. If the default configuration is used, CLK can be set to 0. When parallel mode is selected, force 0.
PUC_SERIAL_DATA	1	I_{PD}	CMOS 1.8V	When serial mode is selected, use as data. When parallel mode is selected, leave open.
PUC_[31:0]	32	I_{PD}	CMOS 1.8V	When parallel mode is selected, use as data bus. When serial is selected, leave open.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
Recommended Operating Voltage				
ROV_[7:0]	8	O_{PD}	CMOS 1.8V	Recommended operating voltage. These pins define the required VDDC voltage levels with which the specific device should work. Working with a VDDC level that is different from the value required by the ROV may cause the device to fail normal operation or exceed power limits. For ROV information, see Section 5.2, Recommended Operating Conditions.
Reference Clocks				For connectivity information, see Section 5.9, Reference Clocks.
PCIE_REFCLK_P/N	2	I	Differential CML	PCIe reference clock inputs. 100 MHz. This clock is mandatory in all applications and requires external AC coupling. External 100Ω termination is required between P and N pins.
C_PLL_REFCLK_P/N	2	I	Differential CML	Core PLL reference clock inputs. 50 MHz. This clock is mandatory in all applications and requires external AC coupling.
U_PLL_REFCLK_P/N	2	I	Differential CML	Microcontroller (in iProc) PLL reference clock inputs. 50 MHz. This clock is mandatory in all applications and requires external AC coupling.
TS_PLL_REFCLK_P/N	2	I	Differential CML	TSPLL (time stamp PLL) and BSPLL (BroadSync PLL) reference clock. 50 MHz. This clock requires external AC coupling. Usage options: ■ When not in use, pull to GND. R ≤ 1 kΩ. ■ When using BroadSync, can be sourced from a simple free-running local oscillator. ■ When using BroadPTP™, must be sourced from TDPLL, which is sourced from OCXO.
DRAM_PHY_REFCLK_P/N	2	I	Differential CML	DRAM PHY reference clock inputs. 50 MHz. This clock is mandatory in all applications and requires external AC coupling.
FAB_PLL_REFCLK_P/N	2	I	Differential CML	Fabric PLL reference clock inputs. 156.25 MHz Used for fabric logic section (not for SerDes core). This clock is mandatory in all applications and requires external AC coupling.
NIF_SEC_PLL_REFCLK_P/N	2	I	Differential CML	NIF SEC PLL reference clock inputs. 156.25 MHz. Used for NIF logic section. This clock is mandatory in all applications and requires external AC coupling.
NIF_TSC_PLL_REFCLK_P/N	2	I	Differential CML	NIF TSC PLL reference clock inputs. 156.25 MHz Used for NIF logic section. This clock is mandatory in all applications and requires external AC coupling.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
FAB_[1:0]_REFCLK_P/N	2 × 2	I	Differential CML	FAB SerDes reference clock inputs. 156.25 MHz. This clock is required for applications that use the fabric SerDes. It requires external AC coupling. In a typical application, FAB_[1:0]_REFCLK reference clocks should share the same source. For unused FAB[1:0]_REFCLK, pull inputs to GND, R ≤ 1 kΩ.
NIF_[3:0]_REFCLK_P/N	4 × 2	I	Differential CML	NIF SerDes reference clock inputs. **312.5 MHz**. This clock is mandatory in all applications and requires external AC coupling. In a typical application, NIF_[3:0]_REFCLK reference clocks should share the same source.
FRAMER_PLL_REFCLK_P/N	2	I	Differential CML	FRAMER PLL reference clock inputs. 155.52 MHz. FRAMER_PLL_REFCLK and SAR_PLL_REFCLK should come from the same source. This clock is mandatory in all applications and requires external AC coupling.
SAR_PLL_REFCLK_P/N	2	I	Differential CML	SAR PLL reference clock inputs. 155.52 MHz. FRAMER_PLL_REFCLK and SAR_PLL_REFCLK should come from the same source. This clock is mandatory in all applications and requires external AC coupling.
Test Clocks (for Internal Testing)				
FAB50_OCT_03_REFCLK_P/N FAB50_OCT_05_REFCLK_P/N	2 × 2	I	Differential CML	Factory test only. Pull to GND, R ≤ 1 kΩ.
NIF50_OCT_00_C_PLL0_REFCLK_P/N NIF50_OCT_03_C_PLL0_REFCLK_P/N	2 × 2	I	Differential CML	Factory test only. Pull to GND, R ≤ 1 kΩ.
PLL Lock Indications				
C_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Core PLL lock indication. High indicates PLL is locked.
U_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Microcontroller PLL lock indication. High indicates PLL is locked.
FAB_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Factory test only. Leave open.
NIF_SEC_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Factory test only. Leave open.
NIF_TSC_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Factory test only. Leave open.
TS_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Factory test only. Leave open.
BS_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Factory test only. Leave open.
FRAMER_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Factory test only. Leave open.
SAR_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Factory test only. Leave open.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
PLL Test Outputs (for Internal Testing)				
BS_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
C_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
FAB_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
NIF_SEC_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
NIF_TSC_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
TS_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
U_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
PCIE_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
DRAM_PHY_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
DRAM_PHY_CLK_OBS_[1:0]_P/N	2 × 2	O	Differential HCSL	Factory test only. Leave open.
FAB50_OCT_00_TESTOUT_P/N FAB50_OCT_03_TESTOUT_P/N FAB50_OCT_05_TESTOUT_P/N FAB50_OCT_06_TESTOUT_P/N	4 × 2	O	Differential CML	Factory test only Leave open.
NIF50_OCT_00_C_PLL0_TESTOUT_P/N NIF50_OCT_01_B_PLL0_TESTOUT_P/N NIF50_OCT_02_B_PLL0_TESTOUT_P/N NIF50_OCT_03_C_PLL0_TESTOUT_P/N NIF50_OCT_04_B_PLL0_TESTOUT_P/N NIF50_OCT_06_B_PLL0_TESTOUT_P/N	6 × 2	O	Differential CML	Factory test only. Leave open.
CLK_OBS_P/N	2	O	Differential HCSL	Factory test only. Leave open.
FRAMER_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
SAR_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
Host Interface Utilities				
QSPI				An interface to an external serial flash memory device that holds the PCIe SerDes firmware and configuration. The output pins for this interface are driven even when the device is in reset.
QSPI_CS_N	1	O_{PD}	CMOS 1.8V	Chip select (active low) from device to flash.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
QSPI_HOLD_N	1	O_{PD}	CMOS 1.8V	Hold (active low) from device to flash. Can be used to pause the serial communication with the initiator device without resetting the serial sequence.
QSPI_MISO	1	I_{PD}	CMOS 1.8V	Serial data from flash (SO) to device (MI).
QSPI_MOSI	1	O_{PD}	CMOS 1.8V	Serial data from device (MO) to flash (SI).
QSPI_SCK	1	O_{PD}	CMOS 1.8V	Serial clock from device to flash.
QSPI_WP_N	1	O_{PD}	CMOS 1.8V	The write protect (WP_N) allows normal read/write operations when held high. When WP_N is brought low, all write operations are blocked.
BSC/I2C Interface				The BSC/I^2C interface (responder only) is used for PCIe debugging and QSPI image programing.
I2C_SCL	1	IOD	CMOS 1.8V	I^2C clock. Open drain. Must be pulled up externally to 1.8V.
I2C_SDA	1	B_{OD}	CMOS 1.8V	I^2C data in/out. Open drain. Must be pulled up externally to 1.8V.
MIIM Interface				The MIIM interface enables controlling external PHY (initiator mode only). Supports Clause 22/45 protocol formats with CMOS 1.8V signaling.
MDC_[11:0]	12	O_{PU}	CMOS 1.8V	Clock output of MIIM interface chains. When not in use, leave open. MDC_[3:0] are for factory test only. Leave open.
MDIO_[11:0]	12	B_{PU}	CMOS 1.8V	Data in and data out of MIIM interface chains. When not in use, leave open. MDIO_[3:0] are for factory test only. Leave open.
UART UART[1:0]: BroadPTP Time of day (ToD). UART[3:2]: Embedded CPU debug.				
UART[3:0]_SIN	4	I_{PD}	CMOS 1.8V	UART data receive (RX). When not in use, leave open.
UART[3:0]_SOUT	4	O_{PU}	CMOS 1.8V	UART data transmit (TX). When not in use, leave open.
UART0_CTS_N UART2_CTS_N UART3_CTS_N	3	I_{PU}	CMOS 1.8V	Factory test only. Leave open.
UART0_RTS_N UART2_RTS_N UART3_RTS_N	3	O_{PU}	CMOS 1.8V	Factory test only. Leave open.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
LED Controller				
LED[4:0]_CLK	5	O_{PD}	CMOS 1.8V	LED clock of the five LED buses. Used to latch the LED output data. When not in use, leave open.
LED[4:0]_DATA	5	O_{PD}	CMOS 1.8V	LED data of the five LED buses. Serially indicates port status. When not in use, leave open.
Synchronous Ethernet (SyncE)				With an additional external circuit, these signals can be used for system-level clock synchronization for SyncE applications. See Section 3.4.2, Recovered Clock.
SYNCE[1:0]_CLK_OUT	2	O_{PD}	CMOS 1.8V	SyncE recovered clock.
SYNCE[1:0]_CLK_OUT_VALID	2	O_{PD}	CMOS 1.8V	SyncE valid indication. If used as input by external logic, add pull down to force *not valid* when the device is not fully configured.
IEEE 1588 and BroadSync I/Os				For BroadSync implementation, refer to *Broadcom BroadSync Solution: Description and Implementation* (1588-AN2xx).
TS_GPIO_[5:0]	6	B_{PD}	CMOS 1.8V	User-programmable general-purpose I/Os. Each pin can be individually configured to act as input or output. Usage options: ■ When not in use, leave open. ■ When using BroadSync, TS_GPIO_1 can be used as 1PPS for testing. ■ When using BroadPTP, TS_GPIO_[5:0] can be used as 1PPS input or 1PPS output.
TS[1:0]_1PPS	2	B_{PD}	CMOS 1.8V	Usage options: ■ When not in use, leave open. ■ When using BroadSync or BroadPTP, 1PPS signal.
TS[1:0]_BIT_CLK	2	B_{PD}	CMOS 1.8V	Usage options: ■ When not in use, leave open. ■ When using BroadSync: – TS0_BIT_CLK is used as BroadSync bit clock, usually 10 MHz. This signal can be configured as input for a BroadSync timeReceiver or output for a BroadSync timeTransmitter. – TS1_BIT_CLK is not used. ■ When using BroadPTP, both TS[1:0]_BIT_CLK are optional 10-MHz output.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
TS[1:0]_SYNC	2	B_{PD}	CMOS 1.8V	Usage options: ■ When not in use, leave open. ■ When using BroadSync: – TS0_SYNC is used as BroadSync heartbeat pulse, 4 kHz. Marks the start of the transmission of the synchronize time value. This signal can be configured as input for BroadSync timeReceiver or output for BroadSync timeTransmitter. – TS1_SYNC is not used. ■ When using BroadPTP, both TS[1:0]_SYNC are optional 4-kHz input or output.
TS[1:0]_TIME_VAL	2	B_{PD}	CMOS 1.8V	Usage options: ■ When not in use, leave open. ■ When using BroadSync: – TS0_TIME_VAL is used as BroadSync synchronized time value and serially shifts the time value 1 bit per rising edge of the TS0_BIT_CLK. This signal can be configured as input for BroadSync timeReceiver or output for BroadSync timeTransmitter. – TS1_TIME_VAL is not used. ■ When using BroadPTP, both TS[1:0]_TIME_VAL are not used.
FRAMER and SAR Signals (for Factory Testing)				
FRAMER_GPI_[9:0]	10	I_{PD}	CMOS 1.8V	Factory test only. FRAMER_GPI_9: Pull to GND, R ≤ 1 kΩ. FRAMER_GPI_[8:0]: Leave open.
FRAMER_GPO_[31:0]	32	O_{PD}	CMOS 1.8V	Factory test only. Leave open.
FRAMER_8K	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
FRAMER_PPS_IN	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
FRAMER_PPS_OUT	1	O_{PD}	CMOS 1.8V	Factory test only. Leave open.
FRAMER_TOD_IN	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
FRAMER_TOD_OUT	1	O_{PD}	CMOS 1.8V	Factory test only. Leave open.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
SerDes				
PCIe				PCIe interface supporting Gen1, Gen2, and Gen3. According to connectivity (x1, x2, or x4), use lanes [0], [1:0], or [3:0].
PCIE_RX_[3:0]_P/N	2 × 4	I	Differential	PCIe differential RX pairs. The lanes should be AC coupled. RX is internally terminated. When not in use, leave open.
PCIE_TX_[3:0]_P/N	2 × 4	O	Differential	PCIe differential TX pairs. The lanes should be AC coupled. When not in use, leave open.
Fabric				
FAB50_RX_[63:00]_P/N	2 × 64	I	Differential	Fabric SerDes (50G) differential RX pairs. The SerDes receiver includes internal serial AC coupling and termination. If external AC coupling is required, see Chapter 5, Electrical Specifications.
FAB50_TX_[63:00]_P/N	2 × 64	O	Differential	Fabric SerDes (50G) differential TX pairs. The link should be AC coupled and have a termination on the link partner receiver. Verify that the link partner includes this circuitry.
Network Interface (NIF)				
NIF50_RX_[63:00]_P/N	2 × 64	I	Differential	NIF SerDes (50G) differential RX pairs. The SerDes receiver includes internal serial AC coupling and termination. SerDes lane mapping in the BCM88830 is different from other DNX devices. For more information, see Section 3.1.3.2, Lane Mapping (Lane Swap) in BCM88830 PM50. If external AC coupling is required, see Chapter 5, Electrical Specifications.
NIF50_TX_[63:00]_P/N	2 × 64	O	Differential	NIF SerDes (50G) differential TX pairs. The link should be AC coupled and have a termination on the link partner receiver. Verify that the link partner includes this circuitry.
HBM				
HBM_THERM_ALARM	1	O_{PD}	CMOS 1.8V	An indication that a CATTRIP signal from the HBM die was asserted. Indicates that the HBM die temperature has reached a certain level where catastrophic damage may occur unless power is reduced. The CATTRIP output is sticky in that to clear a CATTRIP, power-off of the device is required to return the CATTRIP output to 0. When HBM_THERM_ALARM is asserted, power down the following HBM power supplies: ■ HBM_VDD1P2 ■ HBM_VPP2P5

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
HBM_DA_##	39	I/O	Not defined	HBM direct access port for vendor-specific test implementations. Factory test only. Leave open.
VTMON_AIO (for Internal Testing)				
C_VTMON_AIO	1	B	Analog	Factory test only. Leave open.
FAB[1:0]_VTMON_AIO	2	B	Analog	Factory test only. Leave open.
NIF[1:0]_VTMON_AIO	2	B	Analog	Factory test only. Leave open.
Calibration Resistors (RESCAL)				
FAB[1:0]_RESCAL	2	I/O	Analog	Resistor calibration terminal for SerDes. Connect each pin through an external resistor of 4.53 kΩ (1%) to SRD_AGND. Optimize the resistor placement and signals routing to reduce the signals' resistance as much as possible (<2Ω). ■ FAB0_RESCAL: Calibrate SerDes 0 to 31 ■ FAB1_RESCAL: Calibrate SerDes 32 to 63
NIF[1:0]_RESCAL	2	I/O	Analog	Resistor calibration terminal for SerDes. Connect each pin through an external resistor of 4.53 kΩ (1%) to SRD_AGND. Optimize the resistor placement and signals routing to reduce the signals' resistance as much as possible (<2Ω). ■ NIF0_RESCAL: Calibrate SerDes 0 to 31 ■ NIF1_RESCAL: Calibrate SerDes 32 to 63
Thermal Diode Sensors (for Internal Testing)				
C_THERM_DIODE_P/N	2	B	Analog	Factory test only. Leave open.
JTAG				
CORE_TAP_CTRL_N	1	I_{PD}	CMOS 1.8V	JTAG test enable. ■ Set to 0 during normal device operation. ■ Set to 1 to enable JTAG functionality. An option is to connect with JTAG_TRST_N.
JTAG_TCK	1	I_{PD}	CMOS 1.8V	JTAG, clock input.
JTAG_TDI	1	I_{PU}	CMOS 1.8V	JTAG, input data.
JTAG_TDO	1	O	CMOS 1.8V	JTAG, output data.
JTAG_TMS	1	I_{PU}	CMOS 1.8V	JTAG, TMS test mode input.
JTAG_TRST_N	1	I_{PD}	CMOS 1.8V	JTAG TAP controller reset. Pull down to GND. (R ≤ 10 kΩ.)
JTAG_TR_TCK	1	I	CMOS 1.8V	Factory test only. Pull down to GND. (R ≤ 1 kΩ.)

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
SPI (for Internal Testing)				
SPI_MISO	1	O_{PU}	CMOS 1.8V	Factory test only. Leave open.
SPI_MOSI	1	I_{PU}	CMOS 1.8V	Factory test only. Leave open.
SPI_SCK	1	I_{PU}	CMOS 1.8V	Factory test only. Leave open.
SPI_SSN	1	I_{PU}	CMOS 1.8V	Factory test only. Leave open.
BRCM Test I/Os (for Internal Testing)				
ATPG_MODE_N	1	I_{PU}	CMOS 1.8V	Pull to VDDO. R ≤ 1 kΩ.
EDMON	1	O	Analog	Factory test only. Connect to VSS directly (without a pull-down resistor).
TRI_N	1	I_{PU}	CMOS 1.8V	Pull to VDDO. R ≤1 kΩ.
TEST_[4:0]	5	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
FTEST_[63:0]	64	B	CMOS 1.8V	Factory test only. Required connectivity: ■ FTEST_[1:0]: Connect to GND. R ≤ 1 kΩ. ■ FTEST_[20:4]: Connect to GND. R ≤ 1 kΩ. ■ FTEST_[63:62]: Connect to GND. R ≤ 1 kΩ. ■ Other FTEST pins: Leave open.
NIF_IDDQ	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
FABRIC_IDDQ	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
PCIE_IDDQ	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
JTAG_SEL_[2:0]	3	I_{PD}	CMOS 1.8V	Factory test only. Set to 000. R ≤ 1 kΩ.
VQPS_TEST	1	B	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
Power				
Analog 1.8V and GND				
C_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V. Supplies the following blocks: ■ C_PLL ■ FRAMER_PLL ■ NIF_SEC_PLL ■ CORE_VTMON (die center)
U_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V. Supplies the following blocks: ■ U_PLL ■ TS_PLL ■ BS_PLL
DRAM_PHY_PLL_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
FAB_PLL_AVDD1P8	2	PWR	1.8V	PLL analog supply 1.8V Supplies the following blocks: ■ FAB_PLL ■ FAB0_VTMON
FAB1_VTMON_AVDD1P8	1	PWR	1.8V	Analog supply 1.8V.
NIF0_VTMON_AVDD1P8	1	PWR	1.8V	Analog supply 1.8V.
NIF1_VTMON_AVDD1P8	1	PWR	1.8V	Analog supply 1.8V.
SAR_PLL_AVDD1P8	1	PWR	1.8V	PLL analog supply 1.8V. Supplies the following blocks: ■ SAR_PLL ■ NIF_TSC_PLL
DRAM_PHY_PLL_AGND	11	GND	GND	PLL analog ground. Shares the same common GND plane as the VSS pins.
C_AGND	24	GND	GND	PLL analog ground. Shares the same common GND plane as the VSS pins.
U_AGND	12	GND	GND	PLL analog ground. Shares the same common GND plane as the VSS pins.
SAR_PLL_AGND	1	GND	GND	PLL analog ground. Shares the same common GND plane as the VSS pins.
SerDes Supplies and GND				
PCIE_PVDD0P75	1	PWR	0.75V	PCIe PLL power 0.75V.
FAB50_OCT_[7:0]_PVDD0P75	8	PWR	0.75V	SerDes octet PLL power 0.75V.
NIF50_OCT_[7:0]_A_PLL0_PVDD0P75 NIF50_OCT_[7:0]_B_PLL0_PVDD0P75 NIF50_OCT_[7:0]_C_PLL0_PVDD0P75 NIF50_OCT_[7:0]_D_PLL0_PVDD0P75	32	PWR	0.75V	SerDes octet PLL power 0.75V.
NIF50_OCT_[7:0]_A_PLL1_PVDD0P75 NIF50_OCT_[7:0]_B_PLL1_PVDD0P75 NIF50_OCT_[7:0]_C_PLL1_PVDD0P75 NIF50_OCT_[7:0]_D_PLL1_PVDD0P75	32	PWR	0.75V	SerDes octet PLL power 0.75V.
PCIE_RTVDD0P75	3	PWR	0.75V	PCIe SerDes receiver and transmitter power 0.75V.
FAB_RTVDD0P75	72	PWR	0.75V	FAB SerDes receiver and transmitter power 0.75V.
NIF_RTVDD0P75	72	PWR	0.75V	NIF SerDes receiver and transmitter power 0.75V.
FAB_TVDD1P2	20	PWR	1.2V	FAB SerDes transmitter power 1.2V.
NIF_TVDD1P2	20	PWR	1.2V	NIF SerDes transmitter power 1.2V.
SRD_AGND	1276	GND	GND	Analog ground (return path) for Blackhawk and PCIe SerDes and their supplies (PVDD, RTVDD, and TVDD1P2). Shares the same common GND plane as with VSS pins.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
HBM Supplies				
HBM_VDD1P2	58	PWR	1.2V	Supply for HBM VDDC, VDDQ, and for the DRAM controller (HBM side) VDDQ.
HBM_VPP2P5	8	PWR	2.5V	HBM VPP supply.
Main Die VDDC and VDDO Supplies				
VDDC	205	PWR	VDDC	Core power supply. Must be adjusted according to ROV. Working with a VDDC level different from the value required by the ROV may cause the device to fail normal operation or exceed power limits. **NOTE:** ROV levels might be updated closer to the final product definitions.
VDDO	13	PWR	1.8V	I/O 1.8V power supply.
VSS	284	GND	GND	Connect to GND.
Power Supply Sense Indications (Connected to the Power Supplies)				
VDDC_SENSE VSS_SENSE	1 + 1	O	Analog	Used by the system as a feedback to the voltage supply monitor.
HBM_VDD1P2_SENSE HBM_VSS_SENSE	1 + 1	O	Analog	Used by the system as a feedback to the voltage supply monitor.
FAB_RTVDD0P75_SENSE FAB_RTGND_SENSE	1 + 1	O	Analog	Used by the system as a feedback to the voltage supply monitor.
NIF_RTVDD0P75_SENSE NIF_RTGND_SENSE	1 + 1	O	Analog	Used by the system as a feedback to the voltage supply monitor.
Power Supply Observation Indications (Connected to Test Points)				
HBM_VPP_SENSE	1	O	Analog	Voltage observation pin. Connect to test point.
FAB_PVDD0P75_SENSE FAB_PGND_SENSE	1 + 1	O	Analog	Voltage observation pin. Connect to test point.
NIF_PVDD0P75_SENSE NIF_PGND_SENSE	1 + 1	O	Analog	Voltage observation pin. Connect to test point.
Assembly Support Pins				
NB	4	—	—	No ball (package corner).
NC_OCHK	1	—	—	Orientation check. Factory test only. Leave open.

Chapter 5: Electrical Specifications

5.1 Power Supply Absolute Maximum Ratings

The specifications shown in the following table indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect the long-term reliability of the device.

Table 13: Absolute Maximum Ratings

Rail	Pins on Rail	Minimum	Maximum	Unit
Core supply, ROV controlled	VDDC	–0.25	+0.95	V
CMOS I/O 1.8V	VDDO	–0.25	+2.05	V
Analog 1.8V	C_AVDD1P8 DRAM_PHY_PLL_AVDD1P8 FAB_PLL_AVDD1P8 SAR_PLL_AVDD1P8 U_AVDD1P8 FAB1_VTMON_AVDD1P8 NIF0_VTMON_AVDD1P8 NIF1_VTMON_AVDD1P8	–0.25	+2.05	V
SerDes core PLL 0.75V	PCIE_PVDD0P75 NIF50_OCT_[7:0]_#_PLL[1:0]_PVDD0P75[a] FAB50_OCT_[7:0]_PVDD0P75	–0.25	+0.85	V
SerDes RX and TX 0.75V	PCIE_RTVDD0P75 FAB_RTVDD0P75 NIF_RTVDD0P75	–0.25	+0.85	V
SerDes TX 1.2V	FAB_TVDD1P2 NIF_TVDD1P2	–0.25	+1.35	V
HBM 1.2V	HBM_VDD1P2	–0.3	+1.5	V
HBM 2.5V	HBM_VPP2P5	–0.3	+3.0	V

a. # represents A, B, C, or D.

5.2 Recommended Operating Conditions

5.2.1 Recommended Operating Voltage

The BCM88830 is equipped with a preprogrammed recommended operating voltage (ROV) stamp indicating the nominal voltage at which the core (VDDC) of each specific BCM88830 device must be operated. Working with a VDDC level that is different from the value required by the ROV may cause the device to fail normal operation or exceed power limits.

Power-up the BCM88830 with VDDC = 0.8V. Next, read the ROV stamp from the ROV_[7:0] pins. Then, trim the VDDC power supply to the ROV stamp voltage. Perform VDDC trimming before the BCM88830 is initialized. ROV does not change from power-up to power-up.

NOTE: If more than one device is present on the card, make sure each device has its own VDDC power supply. This VDDC power rail cannot be shared with any other supply rail.

Table 14: VDDC Voltage Level According to ROV Stamp

ROV_[7:0]	VDDC Voltage Level (V)
01110101	0.88125
01110110	0.87500
01111000	0.86250
01111010	0.85000
01111100	0.83750
01111110	0.82500
10000000	0.81250
10000010	0.80000
10000100	0.78750
10000110	0.77500
10001000	0.76250
10001010	0.75000
10001100	0.73750
10001110	0.72500
10010000	0.71250
10010010	0.70000
10010100	0.68750
10010110	0.67500

5.2.2 Recommended Operating Voltage Range for DC Supplies

The following table shows the operating voltage range of the DC supplies.

Table 15: Supply Voltage Range

Supply	Symbol	Minimum (V)	Maximum (V)
Core supply, ROV[a] controlled	VDDC	ROV × 0.99	ROV × 1.01
CMOS I/O 1.8V	VDDO	1.71	1.89
Analog 1.8V	C_AVDD1P8 DRAM_PHY_PLL_AVDD1P8 FAB_PLL_AVDD1P8 SAR_PLL_AVDD1P8 U_AVDD1P8 FAB1_VTMON_AVDD1P8 NIF0_VTMON_AVDD1P8 NIF1_VTMON_AVDD1P8	1.71	1.89
SerDes Core PLL 0.75V	PCIE_PVDD0P75 NIF50_OCT_[7:0]_#_PLL[1:0]_PVDD0P75[b] FAB50_OCT_[7:0]_PVDD0P75	0.75	0.785
SerDes RX and TX 0.75V	PCIE_RTVDD0P75 FAB_RTVDD0P75 NIF_RTVDD0P75	0.75	0.785
SerDes TX 1.2V	FAB_TVDD1P2 NIF_TVDD1P2	1.17	1.23
HBM 1.2V	HBM_VDD1P2	1.19[c]	1.21[c]
HBM 2.5V	HBM_VPP2P5	2.43	2.57

a. Recommended operating voltage (ROV).

b. # represents A, B, C, or D.

c. The requirement is to keep a voltage variation of up to ±2% on DC + AC. Keeping a voltage variation of ±1% (±12 mV) for DC and ±1% (±12 mV) for AC is preferred.

NOTE: Usually, the rail name indicates the *typical* value. However, for SerDes core PLL 0.75V and SerDes RX and TX 0.75V, the *minimum* value is 0.75V.

5.3 Device Power Consumption

The BCM88830 device maximum power consumption is as follows:

- 210W for an application with FlexE interfaces.
- 170W for an application with Ethernet only interfaces.

These maximum power numbers are for the worst-case scenario for traffic, voltage, temperature, and process as defined by Broadcom.

Broadcom does not provide a separate value for thermal power. Use the maximum power as the thermal power as well.

Table 16 shows the current drawn by the different supply rails.

NOTE: The following notes apply to Table 16:

- The table describes the estimated worst-case current of each supply during steady state and under worst-case sub-module configuration conditions.
- The table does not define the worst-case power of the full device (in other words, the sum of all maximum currents results in a number higher than the expected device power).
- The table does not take into account in-rush currents caused by the board and PDN, or by power supply response.

Table 16: Supply Rails and Their Drawn Current

Voltage Rail	Voltage	Related Ball	Number of Instances	Max. Current per Instance (mA)	Max. Current From Power Supply (mA)
Core supply, ROV controlled	ROV	VDDC	1	320,000	320,000
CMOS I/O 1.8V	1.8	VDDO	1	1500	1500
Analog 1.8V	1.8	SAR_PLL_AVDD1P8	1	48	250
		U_AVDD1P8	1	72	
		C_AVDD1P8	1	72.4	
		DRAM_PHY_PLL_AVDD1P8	1	24	
		FAB_PLL_AVDD1P8	1	24.4	
		FAB1_VTMON_AVDD1P8	1	0.4	
		NIF0_VTMON_AVDD1P8	1	0.4	
		NIF1_VTMON_AVDD1P8	1	0.4	
SerDes PLL	0.75	PCIE_PVDD0P75	1	30	6200
		FAB50_OCT_xx_PVDD0P75	8	85	
		NIF50_OCT_xx_x_PLLx_PVDD0P75	64	85	
SerDes RTVDD	0.75	FAB_RTVDD0P75	64	250	32,500
		NIF_RTVDD0P75	64	250	
		PCIE_RTVDD0P75	1	150	
SerDes 1.2V	1.2	FAB_TVDD1P2	64	20	2600
		NIF_TVDD1P2	64	20	
HBM	1.2	HBM_VDD1P2	1	15000	15000
	2.5	HBM_VPP2P5	1	150	150

NOTE: Usually, the rail name indicates the *typical* value. However, for SerDes core PLL 0.75V and SerDes RX and TX 0.75V, the range is minimum = 0.75V and maximum = 0.785V.

5.4 Power Supply Filtering

The following table lists the magnitude of supply noise allowed on the different supply rails.

Table 17: Supply Noise Specifications (AC)

Rail	Pins on Rail	Condition	Max.	Unit
Core supply, ROV controlled	VDDC	PCB target impedance:[a] ■ 0 to 10 kHz: PDN < 0.1 mΩ ■ 10 kHz to 5 MHz: PDN < 0.2 mΩ	30	mVpp
CMOS I/O 1.8V	VDDO	100 kHz to 20 MHz	30	mVpp
Analog 1.8V	C_AVDD1P8 DRAM_PHY_PLL_AVDD1P8 FAB_PLL_AVDD1P8 SAR_PLL_AVDD1P8 U_AVDD1P8 FAB1_VTMON_AVDD1P8 NIF0_VTMON_AVDD1P8 NIF1_VTMON_AVDD1P8	50 kHz to 20 MHz	10	mVpp
SerDes core PLL 0.75V	PCIE_PVDD0P75 NIF50_OCT_[7:0]_#_PLL[1:0]_PVDD0P75[b] FAB50_OCT_[7:0]_PVDD0P75	10 kHz to 20 MHz	3	mVpp
SerDes RX and TX 0.75V	PCIE_RTVDD0P75 FAB_RTVDD0P75 NIF_RTVDD0P75	10 kHz to 16 MHz: PDN < 0.625 mΩ	10	mVpp
SerDes TX 1.2V	FAB_TVDD1P2 NIF_TVDD1P2	10 kHz to 20 MHz	10	mVpp
HBM 1.2V	HBM_VDD1P2	100 kHz to 20 MHz: PDN < 3 mΩ	24[c]	mVpp
HBM 2.5V	HBM_VPP2P5	100 kHz to 20 MHz	25	mVpp

a. The target impedance is for the PCB and capacitors and their physical properties.
VRM and VRM inductors should be replaced with an equivalent *simple* resistance model provided by the VRM vendor.

b. # represents A, B, C, or D.

c. The requirement is to keep a voltage variation of up to ±2% on DC + AC. Keeping ±1% (±12 mV) for DC, and ±1% (±12 mV) for AC is preferred.

5.5 Power-Up, Power-Down, and Reset Sequence

NOTE: Compliance with the power-up, power-down, and fail-safe requirements is mandatory for proper operation and long-term reliability.

The tables and figures in this section describe the required logic sequences for power rail power-up and power-down.

If you partition a rail to different power supplies, each group of power supplies should meet the required sequence.

Table 18: Power Rail Names in Power-Up and Power-Down Tables and Figures

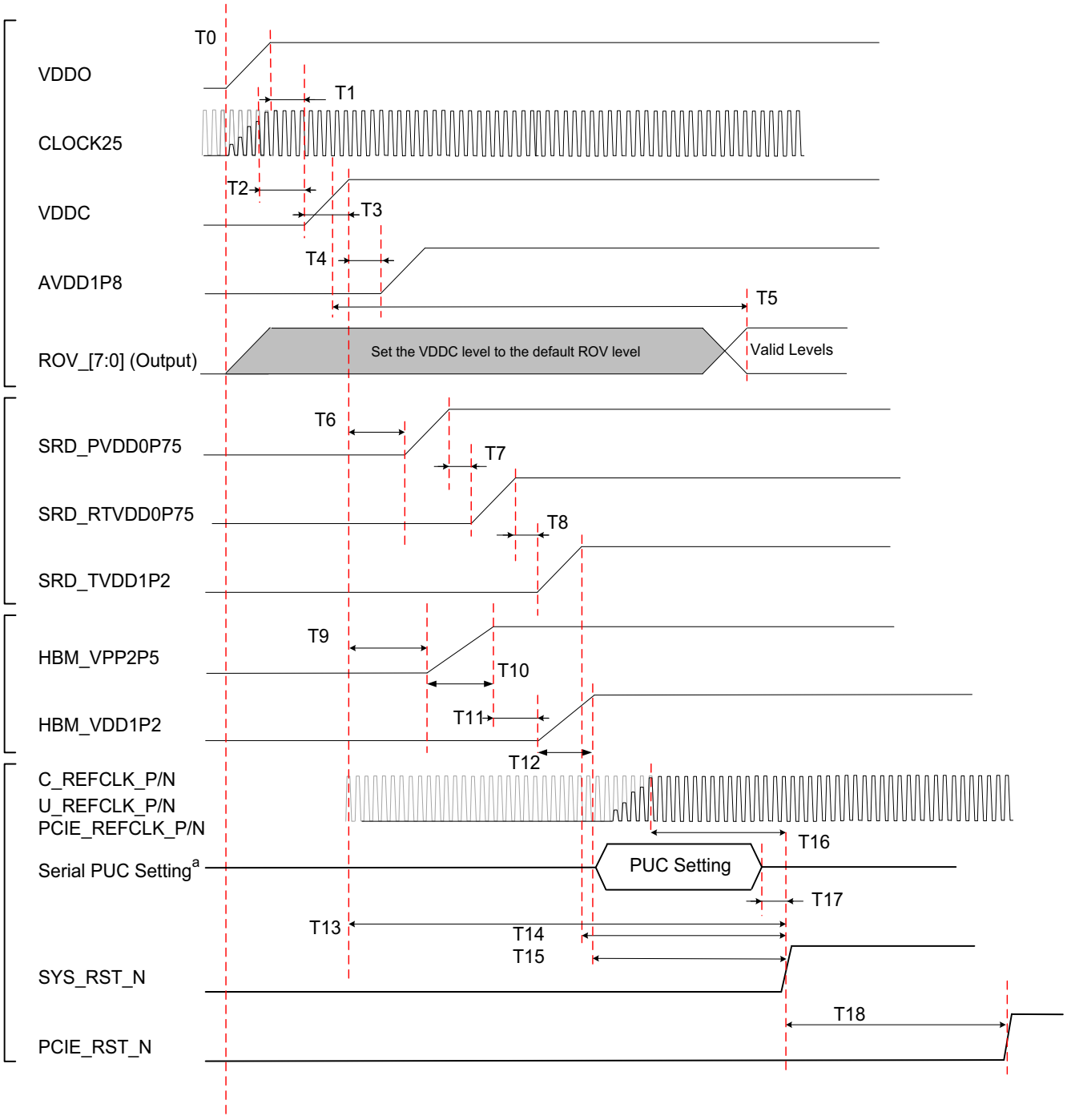
Power Rail Name	Description	Pins on Rail
VDDO	CMOS I/O 1.8V	VDDO
VDDC	Core Supply, ROV controlled	VDDC
AVDD1P8	Analog 1.8V	C_AVDD1P8 DRAM_PHY_PLL_AVDD1P8 FAB_PLL_AVDD1P8 SAR_PLL_AVDD1P8 U_AVDD1P8 FAB1_VTMON_AVDD1P8 NIF0_VTMON_AVDD1P8 NIF1_VTMON_AVDD1P8
SRD_PVDD0P75	SerDes Core PLL 0.75V	PCIE_PVDD0P75 NIF50_OCT_[7:0]_#_PLL[1:0]_PVDD0P75[a] FAB50_OCT_[7:0]_PVDD0P75
SRD_RTVDD0P75	SerDes RX and TX 0.75V	PCIE_RTVDD0P75 FAB_RTVDD0P75 NIF_RTVDD0P75
SRD_TVDD1P2	SerDes TX 1.2V	FAB_TVDD1P2 NIF_TVDD1P2
HBM_VDD1P2	HBM 1.2V	HBM_VDD1P2
HBM_VPP2P5	HBM 2.5V	HBM_VPP2P5

a. # represents A, B, C, or D.

5.5.1 Power-Up Sequence

The following figure illustrates the power-up sequence.

Figure 10: Power-Up Sequence



a. For parallel PUC settings, see Figure 13, Parallel PUC Setting.

NOTE: REFCLK can be active before the device is powered up. Differential clocks require AC coupling, and the amplitude must be within the specifications listed in Table 34, Reference Clock Specifications.

Table 19: Power-Up Sequence Timing

T Number	Description	Min.	Max.	Unit
T0	Initial condition: ■ All voltage rails are below 100 mV ■ TEST[4:0], JTAG_TCE are 0 ■ SYS_RST_N, PCIE_RST_N are 0	—	—	—
T1	(VDDO > 95%) to (VDDC start)	0	—	ms
T2	(CLOCK25 valid) to (VDDC start)	0	—	ms
T3	(VDDC start) to (VDDC > 95%)	—	5	ms
T4	(VDDC > 95%) to (AVDD1P8 start)	0	—	ms
T5	(VDDC > 55%) to ROV valid	—	55	ms
T6	(VDDC > 95%) to (SRD_PVDD0P75 start)	0	—	ms
T7	(SRD_PVDD0P75 > 95%) to (SRD_RTVDD0P75 start)	0	5	ms
T8[a]	(SRD_RTVDD0P75 > 95%) to (SRD_TVDD1P2 start)	0	5	ms
T9	(VDDC > 95%) to (HBM_VPP2P5 start)	0	3	ms
T10	(HBM_VPP2P5 start) to (HBM_VPP2P5 > 95%)	0.01	5	ms
T11	(HBM_VPP2P5 > 95%) to (HBM_VDD1P2 > start)	0.01	5	ms
T12	(HBM_VDD1P2 start) to (HBM_VDD1P2 > 95%)	0.01	30	ms
T13	(VDDC > 95%) to SYS_RST_N deassertion (rising from 0 to 1)	30	—	ms
T14	(SRD_TVDD1P2 > 95%) to SYS_RST_N deassertion (rising from 0 to 1)	10	—	ms
T15	(HBM_VDD1P2 > 95%) to SYS_RST_N deassertion (rising from 0 to 1)	10	—	ms
T16	C_REFCLK and U_REFCLK valid to SYS_RST_N deassertion	10	—	ms
T17	PUC setting completed SYS_RST_N deassertion (see Section 5.6, Power-Up Configuration Word)	160	—	ns
T18	SYS_RST_N =1 to PCIE_RST_N deassertion (rising from 0 to 1)	100	—	ms

a. SRD_TVDD1P2 should *not* exceed SRD_RTVDD0P75 by more than 0.6V (SRD_TVDD1P2 – SRD_RTVDD0P75 < 0.6V).

5.5.2 Power-Down Sequence

The following figure illustrates the power-down sequence.

Figure 11: Power-Down Sequence

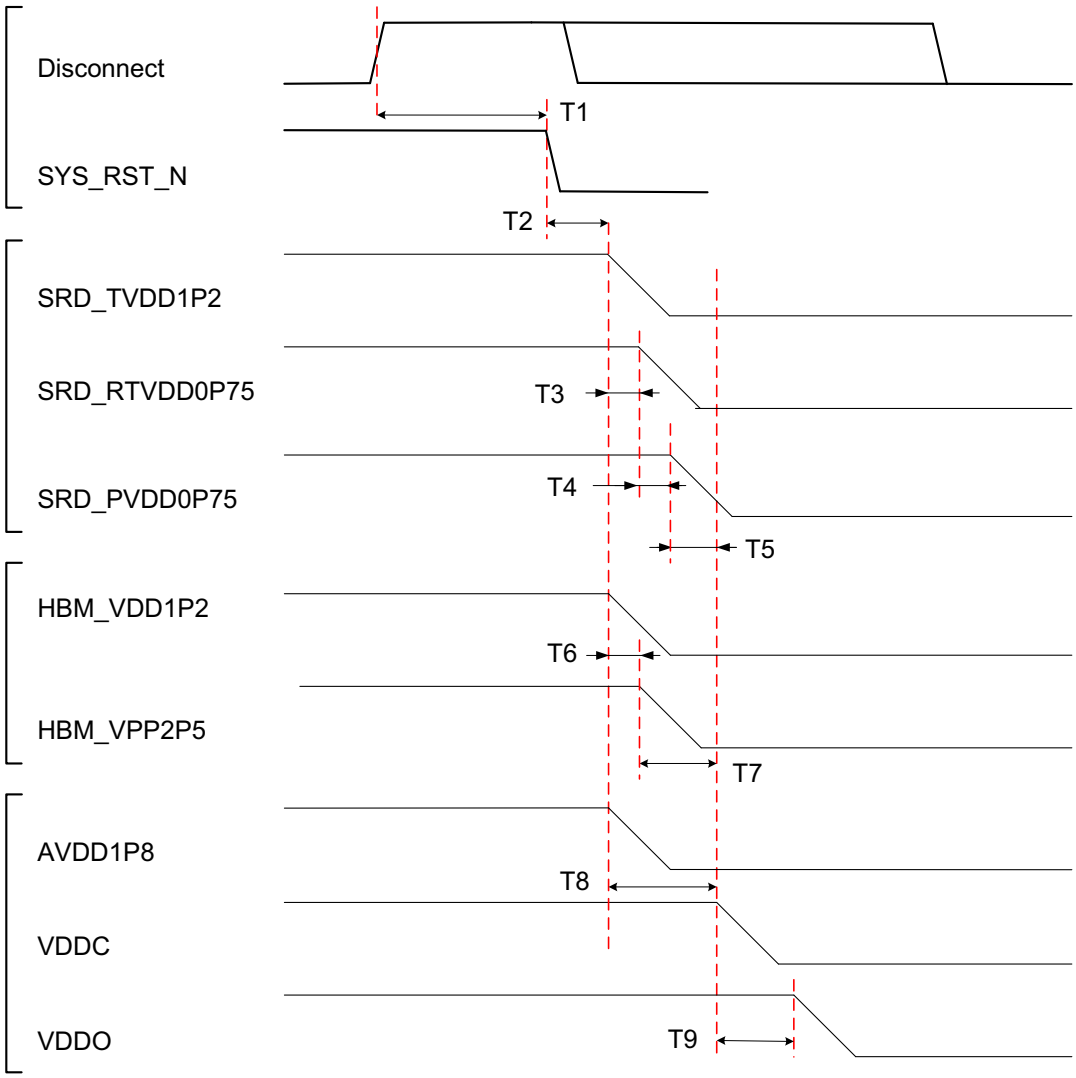


Table 20: Power-Down Sequence Timing

T Number	Description	Min.	Max.	Unit
T1	DISCONNECT pin or SW disconnect before reset. This is optional to maintain traffic data integrity during reset and graceful shutdown.	—	—	—
	For single stage system	15	—	µs
	For multi stage system	10	—	ms
T2[a,b]	SYS_RST_N asserted to first power-off start. This is optional to minimize the number of packets with errors during reset.	5	—	µs
T3[c]	SRD_TVDD1P2 drop start to SRD_RTVDD0P75 drop start.	0	—	ms
T4	SRD_RTVDD0P75 drop start to SRD_PVDD0P75 drop start.	0	—	ms
T5	SRD_PVDD0P75 drop start to VDDC drop start	0	—	ms
T6	HBM_VDD1P2 to HBM_VPP2P5 drop start. (HBM_VPP2P5 supply must be equal to or higher than HBM_VDD1P2 at all times, including during the entire power-down sequence.)	0	—	ms
T7	HBM_VPP2P5 drop start to VDDC drop start.	0	—	ms
T8	AVDD1P8 drop start to VDDC drop start.	0	—	ms
T9	VDDC drop start to VDDO drop start.	0	—	ms

a. Timing is not required between xVDD1P8, SRD_TVDD1P2, and HBM_VDD1P2.

b. Power rails can start the drop without delay.

c. SRD_TVDD1P2 should *not* exceed SRD_RTVDD0P75 by more than 0.6V (SRD_TVDD1P2 – SRD_RTVDD0P75 < 0.6V).

5.5.3 Fail-Safe Considerations

No fail-safe considerations are required. The CMOS I/Os of the BCM88830 are powered by 1.8V VDDO. Input signals can be driven before VDDO (1.8V) is supplied.

5.5.4 Warm Reset

It is possible to reset the device during normal device operation and not just during power-up. To place the device in reset, assert SYS_RST_N and PCIE_RST_N to low. Keep SYS_RST_N low for at least 10 µs before setting it high (releasing the device from the reset condition). The PCIE_RST_N should go high at least 100 ms after the SYS_RST_N.

When taking the device from the reset condition, all the requirements for logic signals that are part of the power-up and reset sequence should be met (see Section 5.5, Power-Up, Power-Down, and Reset Sequence).

5.5.5 HBM-Only Power-Down and Power-Up

If, due to thermal conditions, the HBMs must be powered-down, follow the T6 requirement described in Section 5.5.2, Power-Down Sequence.

When powering-up the HBMs, follow the T10, T11, and T12 requirements described Section 5.5.1, Power-Up Sequence.

5.6 Power-Up Configuration Word

This section describes the power-up configuration (PUC). The following table describes the PUC_[31:0] functionality.

NOTE:

- If the design uses the default value (0x2000_1469), it is possible to set POR_PARALLEL_SEL=0 and keep PUC_SERIAL_CLK as 0 (the ECI_POWERUP_CONFIG register shows 0x22001469).
- When using a parallel PUC setting, use pull-up or pull-down resistors where R < 5 kΩ.

Table 21: Power-Up Configuration Bit Description

PUC	Function	Description
PUC_[9:0]	CORE_PLL_N_DIV[9:0]	For core rate = 1050 MHz, set to 105 (PUC_[9:0] = 0x069, VCO = 5250 MHz)
PUC_[17:10]	CORE_PLL_M_DIV[7:0]	Set to 5 (PUC_[17:0] = 0x01469)
PUC_[19:18]	Factory test	Set to 00
PUC_[21:20]	I2C_SA[1:0]	I^2C responder address. Valid configurations are 2'b00, 2'b01, 2'b10, and 2'b11
PUC_[25:22]	Factory test	Set to 0000
PUC_[27:26]	PCIE_FORCE_GEN[1:0]	Set to 00
PUC_[28]	Factory test	Set to 0
PUC_[29]	Factory test	Set to 1
PUC_[31:30]	PCIE_FORCE_LANE[1:0]	Set to 00

The three options for PUC settings are as follows:

- Use the default setting: When the required PUC word is used as the BCM88830 internal default value, set POR_PARALLEL_SEL=0 and keep the PUC_SERIAL_CLK as 0.
- Use a serial setting: Set POR_PARALLEL_SEL=0 and use PUC_ SERIAL _CLK and PUC_ SERIAL _DATA to load the 32 PUC bits. (For details, see Figure 12 and Table 22.)
- Use a parallel setting: Set POR_PARALLEL_SEL=1 and use the PUC_[31:0] bus to set the 32 PUC bits. (For details, see Figure 13 and Table 23.)

Figure 12: Serial PUC Setting

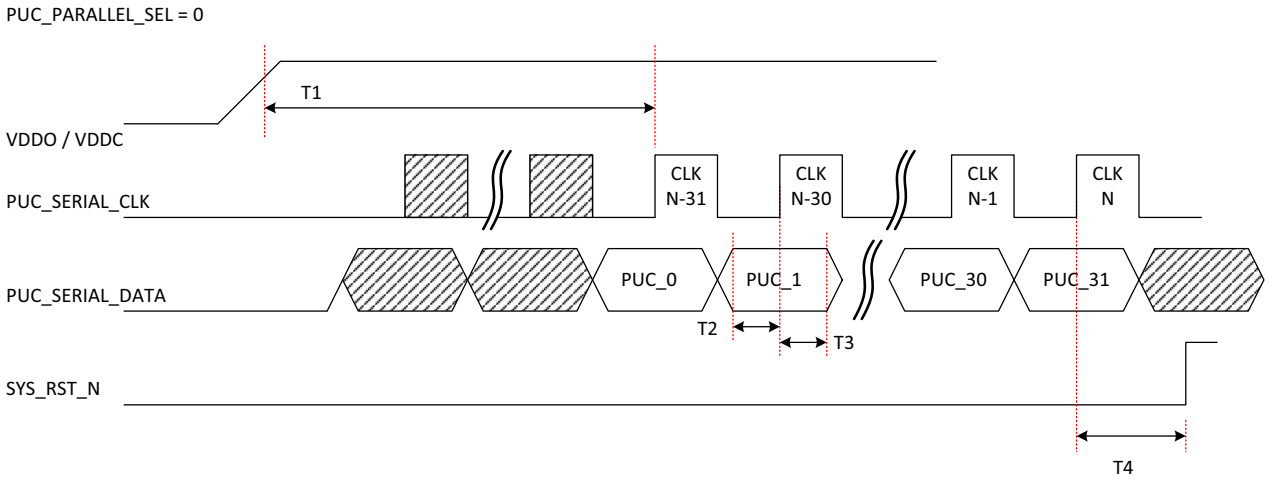


Table 22: Serial PUC Setting Timing

T Reference	Description	Minimum	Unit
T1	VDDO and VDDC (last to reach 95%) to first PUC_SERIAL CLK	30	ms
T2	PUC_SERIAL_DATA to PUC_SERIAL_CLK setup	10	ns
T3	PUC_SERIAL_DATA from PUC_SERIAL_CLK hold	10	ns
T4	Last PUC_SERIAL_CLK to SYS_RST_N rise	160	ns

Figure 13: Parallel PUC Setting

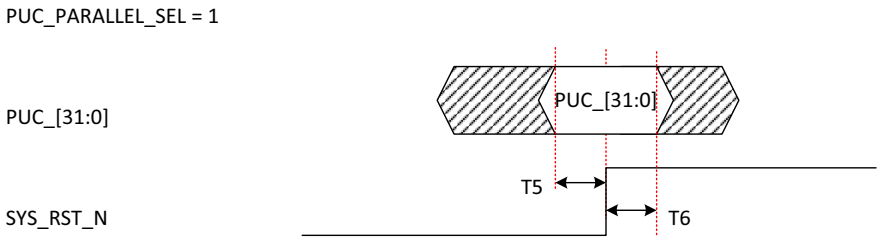


Table 23: Parallel PUC Setting Timing

T Reference	Description	Minimum	Unit
T5	Parallel PUC_[31:0] to SYS_RST_N setup	200	ns
T6	Parallel PUC_[31:0] from SYS_RST_N hold	200	ns

5.7 DC Electrical Specifications

5.7.1 1.8V Digital I/Os

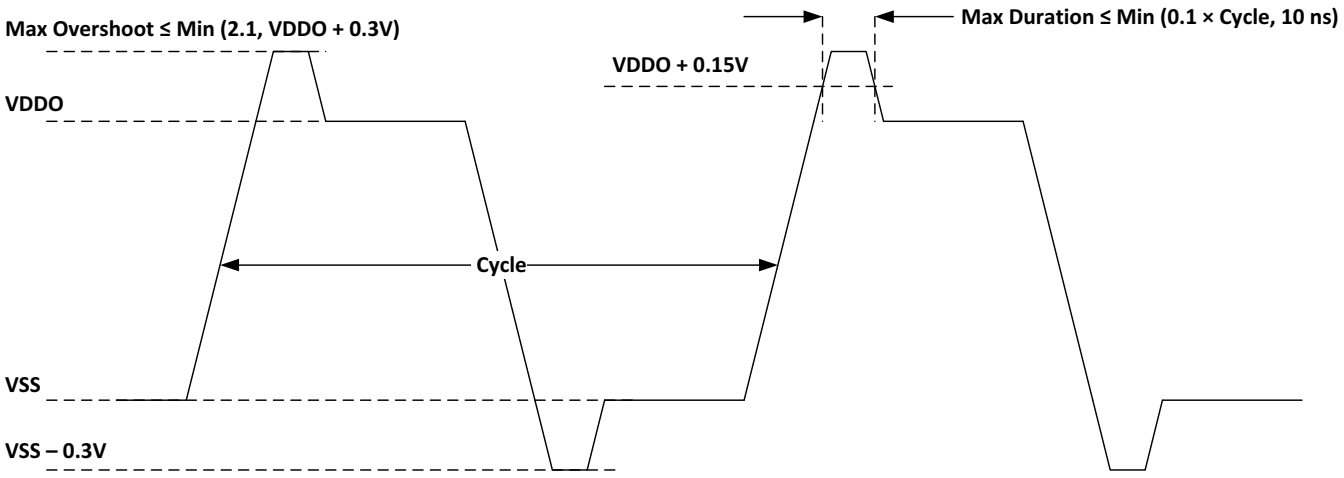
The following table lists the DC specifications for the CMOS1.8V I/Os.

Table 24: DC Specification for CMOS 1.8V I/O

Parameters	Symbol	Conditions	Min.	Max.	Unit
Input low-level voltage	V_{IL}	—	See Figure 14	VDDO × 0.35	V
Input high-level voltage	V_{IH}	—	VDDO × 0.65	See Figure 14	V
Output low-level voltage	V_{OL}	I_{OUT} = 6 mA	—	0.45	V
Output high-level voltage	V_{OH}	I_{OUT} = –6 mA	VDDO – 0.45	—	V

The following figure shows CMOS 1.8V overshoot definitions.

Figure 14: CMOS 1.8V Input Overshoot Definitions



The high overshoot should be lower than 2.1V and lower than VDDO + 0.3V (whichever is lower). The low overshoot can be down to GND – 0.3V. The duration, measured on a level of half the peak, should be less than 10% of the duty cycle and less than 10 ns.

5.7.2 BSC/I^{2}C

The following table lists the DC specifications of the BSC I/Os.

Table 25: DC Specification for CMOS 1.8V BSC/I^{2}C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input low level voltage	V_{IL}	—	—	—	0.3 × VDD	V
Input high level voltage	V_{IH}	—	0.7 × VDD	—	2.0	V
Output low level current	V_{OL}	V_{OL} = 0.4V	8	—	—	mA

5.8 AC Electrical Specifications

5.8.1 BSC/I^{2}C Interface Timing

The BSC (I^{2}C-compatible) interface supports standard I^{2}C mode and can operate at up to 100 kHz.

The BSC interface of the BCM88830 can operate in responder mode only.

The BCM88830 samples BSC_SDA during a write operation and drives BSC_SDA during a read operation.

Figure 15: BSC Timing Diagram

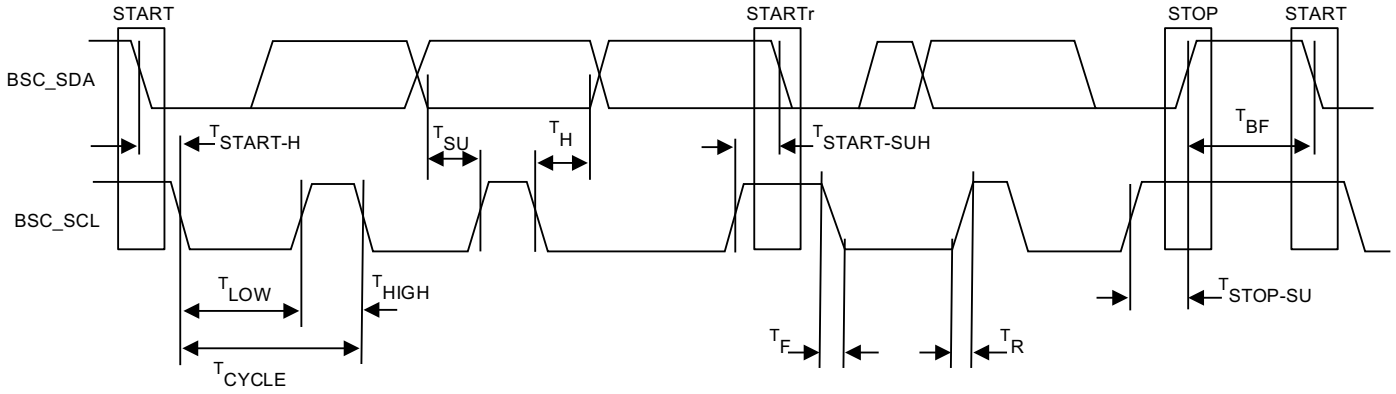


Table 26: BSC Responder Standard-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
BSC_SCL clock frequency	f_{CLK}	—	—	100	kHz
BSC_SCL cycle time	T_{CYCLE}	10	—	—	µs
BSC_SCL low time	T_{LOW}	4.7	—	—	µs
BSC_SCL high time	T_{HIGH}	4.0	—	—	µs
Data hold time	T_H	0.0	—	—	µs
Data setup time	T_{SU}	250	—	—	ns
Rise time data[a]	T_R	—	—	1000	ns
Fall time data	T_F	—	—	300	ns
Hold time, start, or repeated start	$T_{START–H}$	4.0	—	—	µs
Setup time, repeated start	$T_{START–SU}$	4.7	—	—	µs
Setup time, stop	$T_{STOP–SU}$	4.0	—	—	µs
Bus free time (between stop and start)	T_{BF}	4.7	—	—	µs

a. BSC_SCL is an open-drain input, and BSC_SDA is an open-drain input/output. The rise time is dependent on the strength of the external pull-up resistor, which must be chosen to meet the rise time requirement.

5.8.2 Management (MDC and MDIO) Interface Timing

The following figure and table describe the MDIO AC characteristics.

Figure 16: MIIM Interface Timing Diagram

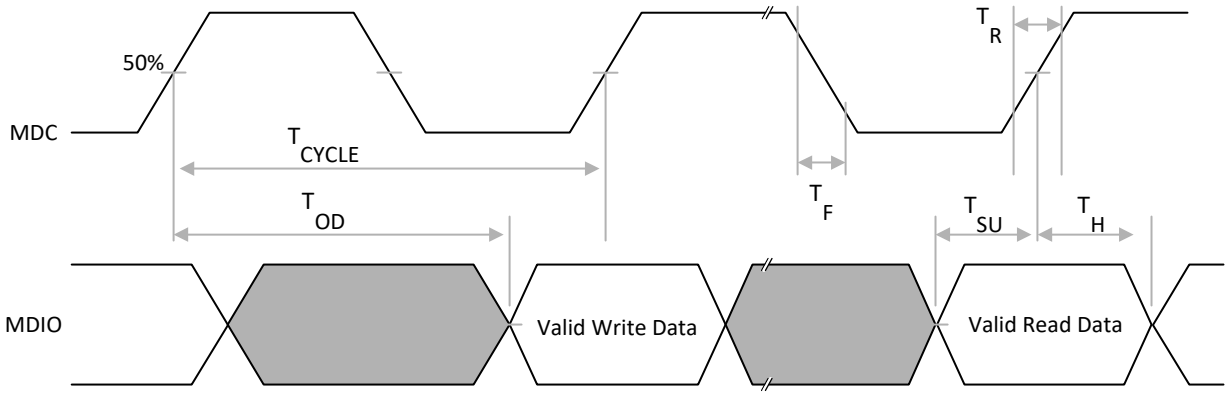


Table 27: MDC and MDIO Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
MDC clock frequency	f_{CLK}	—	2.5	12.5	MHz
MDC cycle time	T_{CYCLE}	80	400	—	ns
MDC duty cycle	—	40	—	60	%
MDIO setup time	T_{SU}	20	—	—	ns
MDIO hold time	T_H	0	—	—	ns
MDIO output delay	T_{OD}	10	—	35	ns

NOTE:

- Output load conditions = 25 pF.
- The external device conforms to the IEEE specifications.
- The MDC rate and the MDIO output delay are configurable.

5.8.3 LED Timing

LED[4:0]_CLK and LED[4:0]_DATA are outputs. LED[4:0]_CLK output clock period is 200 ns (5.0 MHz).

Figure 17: LED Timing Diagram

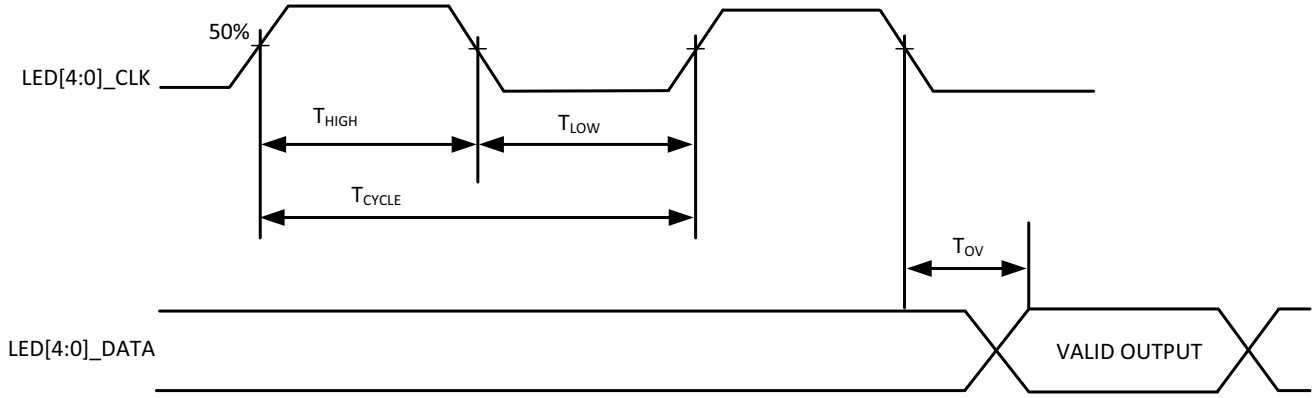


Table 28: LED Timing[a]

Parameter	Symbol	Min.	Typ.	Max.	Unit
LED frequency	F_{TCK}	—	20	—	MHz
LED period	T_{CYCLE}	50	—	—	ns
LED clock HIGH	T_{HIGH}	20	25	30	ns
LED clock LOW	T_{LOW}	20	25	30	ns
LED data output valid	T_{OV}	–5	—	5	ns

a. Timing figures are specified at the 50% crossing thresholds.

5.8.4 BroadSync and Time Sync Timing

The following figure and table show the timeReceiver mode input timing.

Figure 18: BroadSync Input Timing – timeReceiver Mode

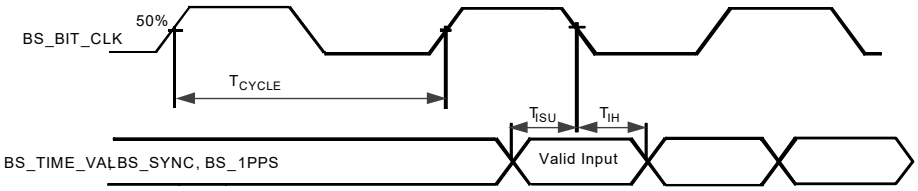


Table 29: BroadSync Input Timing – timeReceiver Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	—	100	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	ns
BS_TIME_VAL; BS_SYNC, BS_1PPS input setup time	t_{ISU}	20	—	—	ns
BS_TIME_VAL; BS_SYNC, BS_1PPS input hold time	t_{IH}	0	—	—	ns

The following figure and table show the timeTransmitter mode input timing.

Figure 19: BroadSync Output Timing – timeTransmitter Mode

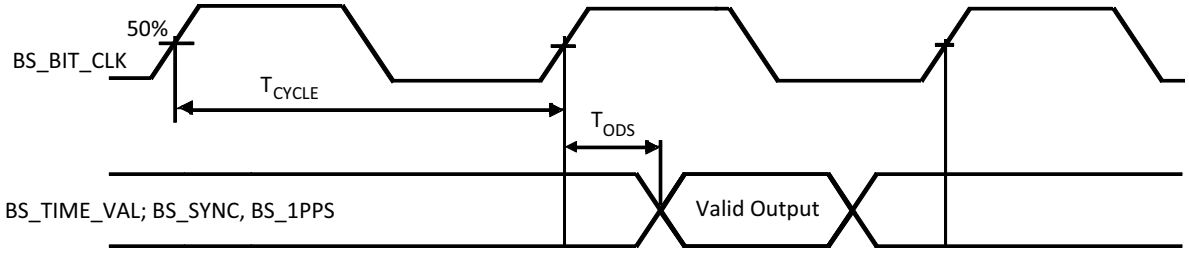


Table 30: BroadSync Output Timing – timeTransmitter Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	—	100	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	ns
BS_TIME_VAL; BS_SYNC, BS_1PPS output delay	t_{ODV}	0	—	25	ns

5.8.5 PCIe Interface

The PCIe core of the BCM88830 supports PCIe Gen1 (2.5G), Gen2 (5G), and Gen3 (8G). The following sections provide basic electrical specifications.

5.8.5.1 PCIe Receiver

The following table lists the specifications of the PCIe SerDes receiver.

Table 31: PCIe SerDes RX Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input differential swing[a]	$V_{IN-DIFF}$	85	—	1200	mVppd
Input differential termination	R_{TERM}	80	100	120	Ω

a. The receiver input should be externally AC coupled.

5.8.5.2 PCIe Transmitter

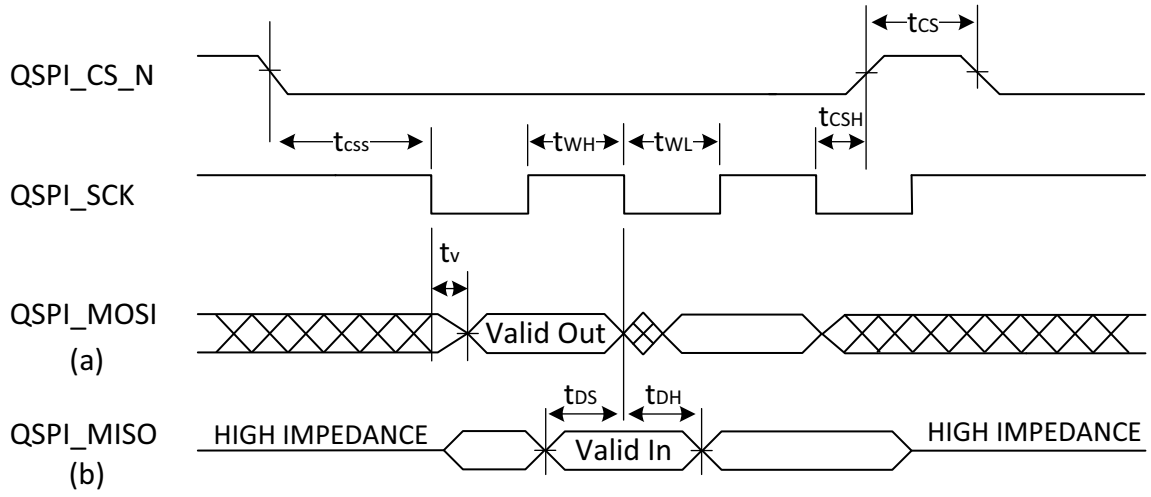
The following table lists the specifications of the PCIe SerDes transmitter.

Table 32: PCIe SerDes TX Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output differential termination	R_{TERM}	80	100	120	Ω
Output differential swing (programmable)	$V_{OUT-DIFF}$	400	—	1200	mVppd
Output common mode	V_{OUT-CM}	—	400	—	mV

5.8.6 QSPI Flash Interface

Figure 20: IP_QSPI Timing (Boot Read Mode Using BSPI Controller)



(a): Also valid for QSPI_MISO in dual/quad mode; also valid for QSPI_WP_N, QSPI_HOLD_N in quad mode.
(b): Also valid for QSPI_MOSI in dual/quad mode; also valid for QSPI_WP_N, QSPI_HOLD_N in quad mode.

Table 33: IP_QSPI Timing (Boot Read Mode Using BSPI Controller)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	62.5[a]	—	MHz
SCK clock LOW period	t_{WL}	0.5 / F_{SCK} – 0.5	—	—	ns
SCK clock HIGH period	t_{WH}	0.5 / F_{SCK} – 0.7	—	—	ns
CS lead time	t_{CSS}	1 / F_{SCK} – 2.9	—	—	ns
CS trail time	t_{CSH}	–1.6	—	—	ns
MOSI output valid	t_V	–1.6	—	3	ns
MISO input setup	t_{SU}	4	—	—	ns
MISO input hold	t_H	1.3	—	—	ns

a. The QSPI controller issues only FAST_READ commands, as opposed to READ (03h) commands. Therefore, the operating frequency of the QSPI device should be based on the Fast Read commands rather than Read (03h) command.

5.9 Reference Clocks

5.9.1 REFCLK Specifications

The following table lists the specifications of the BCM88830 reference clock. Duty cycle, T_R / T_F, and swing values are shown from minimum to maximum.

Table 34: Reference Clock Specifications

Reference Clock	Freq. (MHz)	I/O Type	Tolerance (PPM)	Duty Cycle (%)	T_R / T_F (ns)[a]	Max. T_{SLEW} (ns/Vppd)	Input Jitter	Swing Vppd[b]	Internal Termination
CLOCK25	25	CMOS (1.8V)	±100	40 to 60	0.5 to 4	—	100 ps[c]	Follow CMOS I/O definitions	No[d]
C_PLL_REFCLK	50	CML	±32	40 to 60	—	1	1 ps[e]	0.5 to 2	Yes[f]
U_PLL_REFCLK	50	CML	±32	40 to 60	—	1	1 ps[e]	0.5 to 2	Yes[f]
DRAM_PHY_REFCLK	50	CML	±100	40 to 60	—	1	1 ps[e]	0.5 to 2	Yes[f]
TS_PLL_ REFCLK	50	CML	±50	40 to 60	—	1	1 ps[e]	0.5 to 2	Yes[f]
PCIE_REFCLK	100	CML	±300	40 to 60	0.2 to 0.9	—	Follow PCIe specifications	0.6 to 1.2	No[g]
FRAMER_PLL_REFCLK	155.52	CML	±50	40 to 60	—	1	1 ps[e]	0.5 to 2	Yes[f]
SAR_PLL_REFCLK	155.52	CML	±50	40 to 60	—	1	1 ps[e]	0.5 to 2	Yes[f]
NIF_TSC_REFCLK	156.25	CML	±50	40 to 60	—	1	1 ps[e]	0.5 to 2	Yes[f]
NIF_SEC_REFCLK	156.25	CML	±50	40 to 60	—	1	1 ps[e]	0.5 to 2	Yes[f]
FAB_PLL_REFCLK	156.25	CML	±50	40 to 60	—	1	1 ps[e]	0.5 to 2	Yes[f]
NIF_[3:0]_REFCLK	312.5	CML	±50	40 to 60	0.05 to 0.4	—	0.15 ps[e]	0.8 to 1.4	Yes[f]
FAB_[1:0]_REFCLK	156.25	CML	±50	40 to 60	0.05 to 0.4	—	0.15 ps[e]	0.8 to 1.4	Yes[f]

a. 20% to 80% of minimum amplitude.

b. CML input reference clock differential swing (peak-to-peak).

c. Input jitter cycle-to-cycle, 10K samples. Not meeting the requirement may result in initialization failures or HBM monitoring failures.

d. There is no internal termination for CLOCK25. Use on-board termination for the CMOS line.

e. Integrated phase noise from 12 kHz to 20 MHz, RMS.

f. CML REFCLK with internal termination should follow the clock scheme shown in Figure 21. The example in the figure uses an LVPECL oscillator.

g. PCIE REFCLK requires an external termination and should follow the clock scheme shown in Figure 22. The example in the figure uses an LVPECL oscillator.

NOTE: REFCLK can be active before the device is powered up as long as the amplitude is within the specifications (listed in the previous table) and AC coupling exists.

5.9.2 REFCLK Source Sharing

Source sharing for reference clocks in the BCM88830 device is as follows:

- In a typical application, NIF_[3:0]_REFCLK should come from the same source.
- In a typical application, FAB_[1:0]_REFCLK should come from the same source.
- FRAMER_PLL_REFCLK and SAR_PLL_REFCLK must come from the same source.
- Reference clocks with the same rate can share the same source.

5.9.3 REFCLK Connectivity Schemes

Figure 21: Differential Clock Scheme – CML Internal Termination

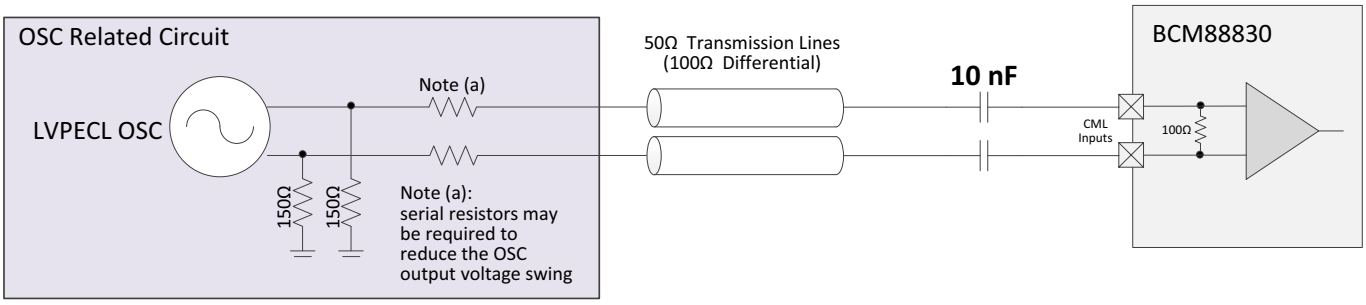
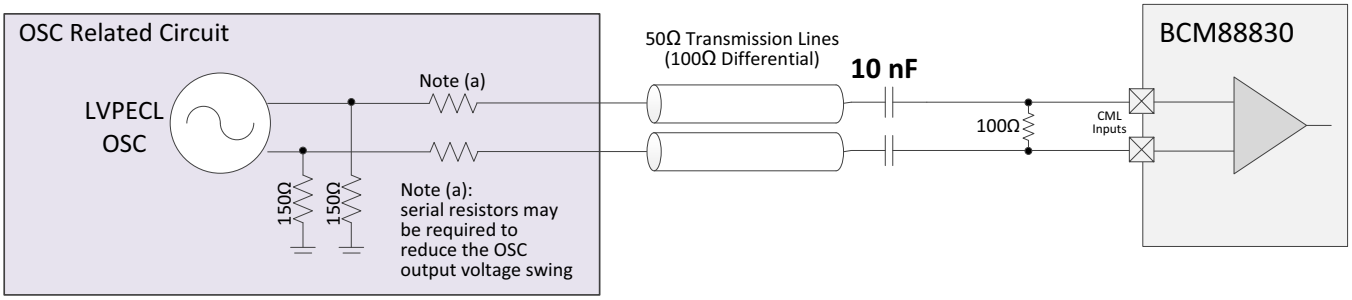


Figure 22: Differential Clock Scheme – CML External Termination



5.10 Blackhawk SerDes Operating Conditions

The Blackhawk SerDes high-speed lanes are organized in cores. Each core, named Blackhawk, includes eight SerDes. Each one of the eight SerDes is an independent lane suitable for optical and backplane applications, operating in either PAM-4 or NRZ line coding.

5.10.1 Blackhawk SerDes Features

The following sections describe the main features on the of the Blackhawk SerDes.

5.10.1.1 General Features

Blackhawk supports the following general features:

- A block of eight SerDes supporting eight serial links. The BCM88830 NIF Blackhawk contains four BH2x2 modules, where each BH2x2 is a unit of two Blackhawk TX/RX SerDes and their PLLs.
- Line rates (depending on the application) from 10.3125 Gb/s to 53.125 Gb/s per serial link (PAM-4 53.125 Gb/s, NRZ 25.78125 Gb/s).
- Integrated Arm micro subsystem: Monitors the signal and adaptively adjusts the gain, peaking-filter, and DFE coefficients to optimally equalize and restore the signal. During Clause 72/93 TX/RX link-training, this microcontroller is also responsible for returning feedback to the far-link partner to optimally tune its transmitter.

5.10.1.2 Debug Features

Blackhawk supports the following debugging features:

- PRBS 7, 9, 10, 11, 13 15, 20, 23, 31, 49, and 58 generator and checker with burst error length measurement.
- Digital loopback: Turns around the transmit data before it goes into the analog front-end (this is a digital data path loopback for the data coming from the PCS/MAC transmit side).
- AC-JTAG for both TX and RX.
- Full-range horizontal and vertical eye diagnostics.

For additional information, refer to *SerDes Configuration and Debugging Guide for StrataDNX™ 16-nm and 7-nm Devices* (DBG16S-AN1xx).

5.10.2 Blackhawk SerDes Receiver

The Blackhawk receiver features are as follows:

- Integrated AC coupling on RX inputs.
- Three-stage analog peaking filter (PF).
- Three-stage controlled variable gain amplifier (VGA).
- 14-tap DFE (six fixed and eight floating) with adaptive control slicer.
- Clock-phase interpolation in receiver timing recovery.
- Programmable RX polarity inversion.

The following table lists the electrical characteristics of the SerDes receiver.

Table 35: SerDes Receiver Characteristics

Parameter	Symbol	Min.	Max.	Unit
Absolute maximum RX input when DC coupling is used on the board (For preventing permanent damage to the device.)	V_{RX_P}[a], V_{RX_N}[a]	–50	800	mV
Absolute maximum RX input when AC coupling is used on the board (For preventing permanent damage to the device.)	$V_{IN-DIFF}$	0	1600	mV

a. Measured RX_P to GND and RX_N to GND. Values outside of this range require an external AC capacitor on the board, that is, AC coupling, 100 nF.

5.10.3 Blackhawk SerDes Transmitter

The Blackhawk transmitter features are as follows:

- Transmitter with fully programmable six-tap FIR.
- IEEE 802.3 link training.
- Programmable TX polarity inversion.
- Controlled peak-to-peak amplitude.

The following table lists the electrical characteristics of the SerDes transmitter.

Table 36: SerDes Transmitter Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Output common mode	V_{OUT-CM}	—	450	—	mV	When terminated with a 100Ω differential
Output differential swing	$V_{OUT-DIFF}$	0	—	1000	mVppd	—

Chapter 6: Thermal Specifications

6.1 Absolute and Operational Thermal Specifications

The BCM88830 is a multi-die device. The package contains the main ASIC die from Broadcom and an HBM die from the memory vendor. Take this structure into consideration when planning the thermal definitions and thermal design.

The following table shows the specifications for the absolute thermal limits.

Table 37: Absolute Thermal Limit Specifications

Parameter	Min.	Max.	Unit
Storage temperature	–40	+100	°C
Main die maximum junction temperature	—	+105[a]	°C
HBM die maximum junction temperature	—	+95[b]	°C
HBM CATTRIP assertion temperature	—	+120[c]	°C

a. Operating at a temperature above the maximum T_J may cause permanent damage to the device.
A maximum excursion temperature of T_J = 115°C for 15 days per year (less than 96 consecutive hours) is allowed.
Proper functionality and performance cannot be guaranteed when the device operates above the maximum junction temperature. When operating in the excursion zone, the maximum power is higher than the maximum power specified in Section 5.3, Device Power Consumption.

b. Over the HBM lifetime, a maximum excursion temperature of 105°C for total of 360 hours per year is allowed. A single excursion period should not be longer than 96 hours, and the time between two consecutive excursion periods is a minimum of 24 hours. During these excursion periods, the HBM performance and reliability are not affected.
When violating the excursion conditions, functional operation failures and reliability degradation are expected.
At 105°C, the HBM power consumption is higher than the value specified in Table 16, Supply Rails and Their Drawn Current. To calculate the consumption per rail, use a factor of ×1.25 for HBM_VDD1P2 and HBM_VPP2P5.

c. Operation above the CATTEMP (120°C) results in immediate and permanent damage to the device.

Table 38: SerDes Core Operating Temperatures (Junction)

Parameter	Symbol	Min. (Industrial-Grade Devices)[a]	Min. (Commercial-Grade Devices)	Max.	Unit
PCIe operating temperature	PCIE_T_N	–20	> 0	+105	°C
Blackhawk operating temperature	BLACKHAWK_T_N	–10	> 0	+105	°C

a. Lowest temperature for operation. For powering up at temperatures between –40°C and 0°C, refer to the *Hardware Design Guidelines for StrataDNX 7-nm Devices (*DNX07-DG1xx) in the Thermal Aspects chapter, Industrial-Grade Devices section.

Table 39: HBM Operating Temperature (Junction, HBM Is Powered On)

Parameter	Symbol	Min.	Max.	Unit
Standard operating temperature	HBM_T_N	0	85	°C
Extended operating temperature[a]	HBM_T_E	85	95	°C

a. The HBM extended operating temperature requires additional refresh cycles, which are inserted automatically by the controller.

NOTE: When the HBM is powered-on, it must comply with the HBM_T_N or HBM_T_E values. The HBM must be powered-down if the die temperature is below the HBM_T_N minimum or above the HBM_T_E maximum.

Table 40: HBM Exceeding Temperature (Junction, HBM Is Powered Off)

Parameter	Symbol	Min.	Max.	Unit
Exceeding temperature[a]	HBM_T_{EXCEED}	95	125	°C

a. The *exceeding* temperature is the temperature that exceeds the extended temperature. For the HBM die, an exceeding junction temperature of 95°C to 125°C for 96 hours per year is allowed as long as the following conditions are met:
1. The HBM is powered-down by the board (follow the power-down sequence as described in Section 5.5.5, HBM-Only Power-Down and Power-Up).
2. The total duration per year is less than 96 hours.
During these exceeding periods, the HBM reliability is not affected. When violating the exceeding temperature conditions, functional operation failures and reliability degradation are expected.

Table 41: Ambient Temperature Conditions

Parameter	Min.	Max.	Unit
Commercial temperature grade	0	+70	°C
Industrial temperature grade	–40	+85	°C

NOTE: For additional thermal information (including information about the temperature excursion), refer to the *Thermal Considerations for High-Power Switching Devices* application note (StrataDNX-StrataXGS-AN1xx).

6.2 Package Block Thermal Model Specifications

The BCM88830 block thermal model is available on the Broadcom Engineering Support Portal (ESP). For more information regarding block models, refer to the `Block_Thermal_Model_Brief.pdf` file, which is part of the block model package.

The block thermal model includes separate entities for the main die and the HBM die. When using the model, set the power consumption for each entity according to the specific application or according to the information provided in Section 5.3, Device Power Consumption. When using the maximum power listed in Section 5.3, consider 14W for the HBM.

Use only the block thermal model to perform thermal simulations. The block thermal model replaces all previous models, such as the 2R model, modified 2R model, and Delphi model. Accordingly, Broadcom does not provide θ_{JC} and θ_{JB} values for the device.

6.3 Temperature Monitoring

The BCM88830 main die has five internal on-die temperature sensors that can be accessed by the software API. These temperature monitors (VTMONs) can be used only while the device is operational. They have an accuracy of ± 3°C.

Table 42: Temperature Monitoring Zones and Sensor Locations

SW Number in `show pvt`	Register	Monitored Zone	Nearby PKG Ball[a]
0	ECI_PVT_MON_A	FAB0	AT35
1	ECI_PVT_MON_B	FAB1	AT26
2	ECI_PVT_MON_E	NIF0	W25
3	ECI_PVT_MON_F	NIF1	W40
4	ECI_PVT_MON_G	Die center	AJ32

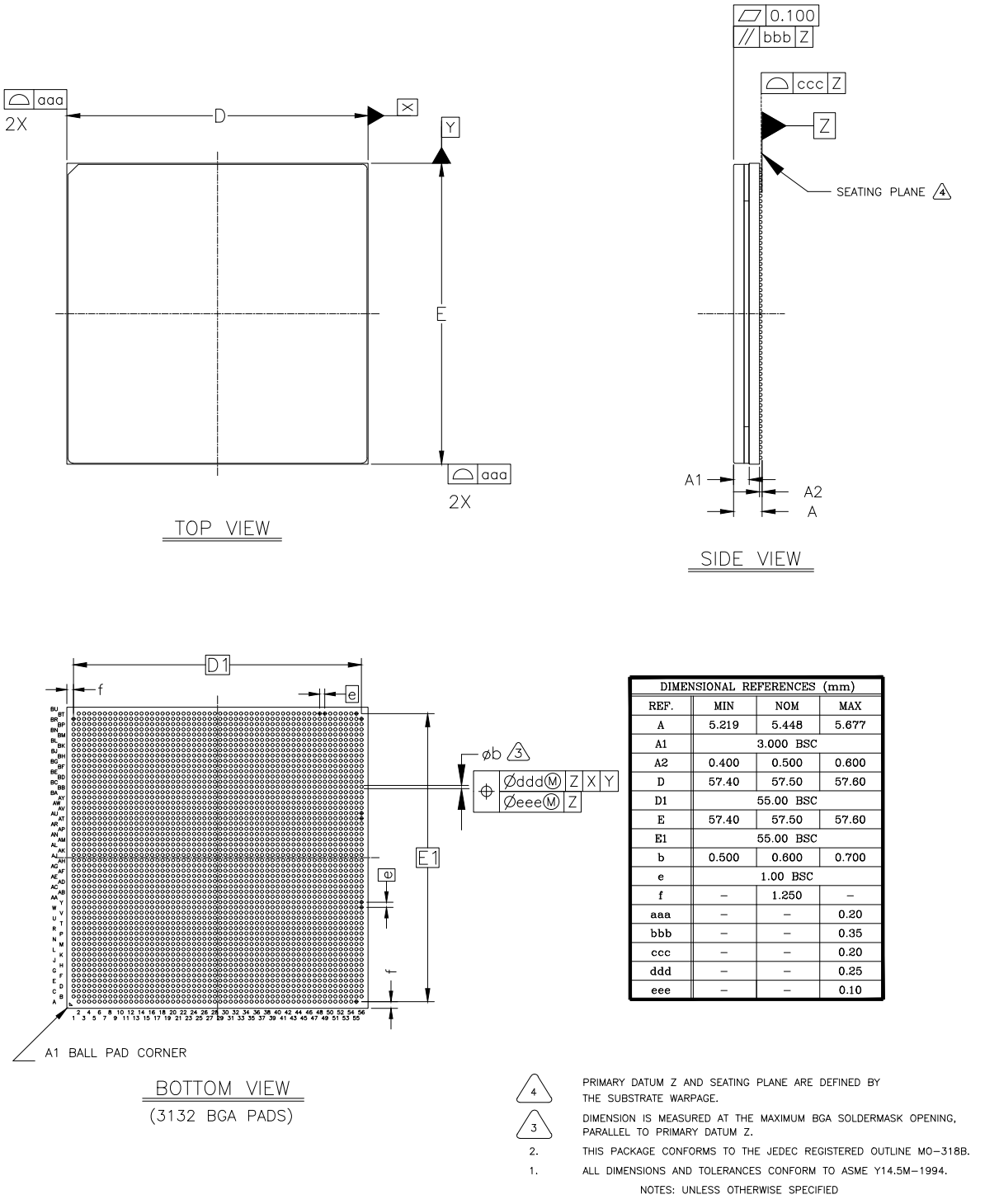
a. Ball numbers are for reference location in the package.

6.4 Heat Sink Considerations

For information about the heat sink, refer to the *Hardware Design Guidelines for StrataDNX 7-nm Devices* (DNX07-DG1xx).

Chapter 7: Packaging

Figure 23: BCM88830 Package (57.5 mm × 57.5 mm, 3132 Ball BGA)



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	5.219	5.448	5.677
A1		3.000 BSC	
A2	0.400	0.500	0.600
D	57.40	57.50	57.60
D1		55.00 BSC	
E	57.40	57.50	57.60
E1		55.00 BSC	
b	0.500	0.600	0.700
e		1.00 BSC	
f	–	1.250	–
aaa	–	–	0.20
bbb	–	–	0.35
ccc	–	–	0.20
ddd	–	–	0.25
eee	–	–	0.10

4. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SUBSTRATE WARPAGE.
3. DIMENSION IS MEASURED AT THE MAXIMUM BGA SOLDERMASK OPENING, PARALLEL TO PRIMARY DATUM Z.
2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-318B.
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

NOTE: The flatness information is for reference only.

7.1 BGA Lead-Free Packaging

Broadcom offers a lead-free (Pb-free) package. Pb-free parts have a letter G added to the top line of the part marking. Broadcom Pb-free parts comply with RoHS and Waste Electrical and Electronic Equipment (WEEE) directives. Broadcom Pb-free parts are fully RoHS 6/6 compatible and require no exemption to comply with European limitations on hazardous substances. The following table shows the solder ball composition and maximum reflow temperature of Pb-free parts.

Table 43: Solder Ball Composition and Recommended and Maximum Reflow Temperature

Part Number	Solder Ball Composition	Recommended Reflow Peak Temperature	Maximum Allowed Reflow Peak Temperature
Pb-free RoHS-compliant package	96.5% Sn, 3% Ag, 0.5% Cu	230°C to 235°C	245°C

Revision History

88830-DS105; January 9, 2024

- Updated Section 1.1, Features, with the following changes:
  - Updated the maximum management and control bandwidth (85 Gb/s).
  - Added the 32 × 50GbE over two lane port configuration.
- Updated Section 3.1, Network Interface, to add 4 × 50GbE ports over two lanes to the Ethernet PM50 configuration list.
- Updated Section 3.1.2, Provisioning of the Network Interface, to modify the speed at which the NIF ports handle management traffic.
- Updated Table 2, PM50 Supported Port Modes, to add 50GbE over two lanes.
- Updated Section 3.1.3.1, Mixed Port Types on PM50, to add that a mix of statistics interface ports and NIF Ethernet/FlexE ports on PM50-3 is not supported.
- Added Section 3.1.3.6.2, 50GbE over Two Lanes.
- Updated Section 3.1.3.8, 25GbE Port, to remove the 25G/50G Ethernet consortium reference.
- Updated Section 3.1.5, Interlaken, to modify the guidelines for logical ILKN lane assignment (RX SerDes and TX SerDes should be on the same BH2x2).
- Updated Section 3.7, Statistics Interface, to add that a mix of statistics interface ports and NIF Ethernet/FlexE ports on PM50-3 is not supported.
- Updated Table 14, VDDC Voltage Level According to ROV Stamp, to remove VDDC = 0.88750V.
- Updated Section 5.3, Device Power Consumption, with the following changes:
  - Updated the device maximum power consumption values.
  - Updated the note regarding the voltage range for SerDes core PLL 0.75V and SerDes RX and TX 0.75V.
- Updated Section 6.2, Package Block Thermal Model Specifications, to add the HBM maximum power value.

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