BROADCOM®

Data Sheet

BCM88690

9.6-Tb/s Integrated Packet Processor, Traffic Manager, and Fabric Interface Single-Chip Device

Overview

The Broadcom® BCM88690 product line is the industry's densest 400G Ethernet switching solution, enabling switching platforms of over 6000 ports of 400G Ethernet.

The BCM88690 device (also known as Jericho2) processes 4.8-Tb/s traffic at packet sizes above 284B and supports up to twelve 400GbE full-duplex ports independent of the packet processing action and configuration. The BCM88690 device has integrated deep-buffer traffic management capabilities, a flexible and programmable packet processor, and a fabric interface. The BCM88690 has integrated 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE and 400GbE network-facing interfaces, supporting various port rate combinations.

The BCM88690 integrates two 4-Hi HBM Gen2 for a total of 8-GB deep buffering. The HBM technology integration enables low power and high performance memory access.

The BCM88690 series is the seventh generation of the StrataDNX™ product line. Together with the BCM88790 (Ramon) fabric element device, it is used to build a variety of network switching solutions:

- Modular – Over 900-Tb/s core, spine, leaf, or data center interconnect (DCI) switch with single-stage fabric for data center, Enterprise, or carrier cloud application.
- Fixed – 4.8-Tb/s TOR, buffered leaf, or buffered spine.
- Multiple interconnected chassis of different capacities that use the BCM88690 and BCM88790 fabric to create a scalable core platform, delivering over 6000 ports of 400GbE.

The BCM88690 packet classification engine is flexible and PEMLA (C++ like syntax) programmable, with built-in support for data center, Enterprise, or carrier cloud application. The large on-chip classification databases can be further extended off-chip using an external KBP (or TCAM) from Broadcom.

The BCM88690 traffic manager integrates deep packet buffers with a distributed scheduling scheme that allows state-of-the-art hierarchical QoS, transmission scheduling, and flow control. The deep buffering capability of the traffic manager enables deployment of lossless protocols. The BCM88690 deep buffers ensure bandwidth allocation fairness between competing flows.

These advanced scheduling and queuing schemes natively support all the latest innovations in data center networking congestion avoidance, such as latency-based and interface utilization-based ECN.

Features

- Seventh-generation StrataDNX FAP product line
- High performance
  - 4.8-Tb/s full-duplex switching
  - 2000-Mp/s processing rate
- Fabric interface:
  - SerDes interface to the StrataDNX Fabric Element (BCM88790)
  - Fabric-less (without the fabric element) configurations of up to four devices
- Flexible network interface
  - SerDes running up to 53.125G (PAM4)
  - 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE, and 400GbE integrated MACs
- Traffic manager
  - High-speed, low-power, HBM Gen2 deep buffering
  - 32-MB on-die buffers
  - Hierarchical resource management
  - Programmable, hierarchical scheduling
  - Supports priority propagation
  - Compliant with scheduling and shaping standards, including MEF and DSL-FORUM

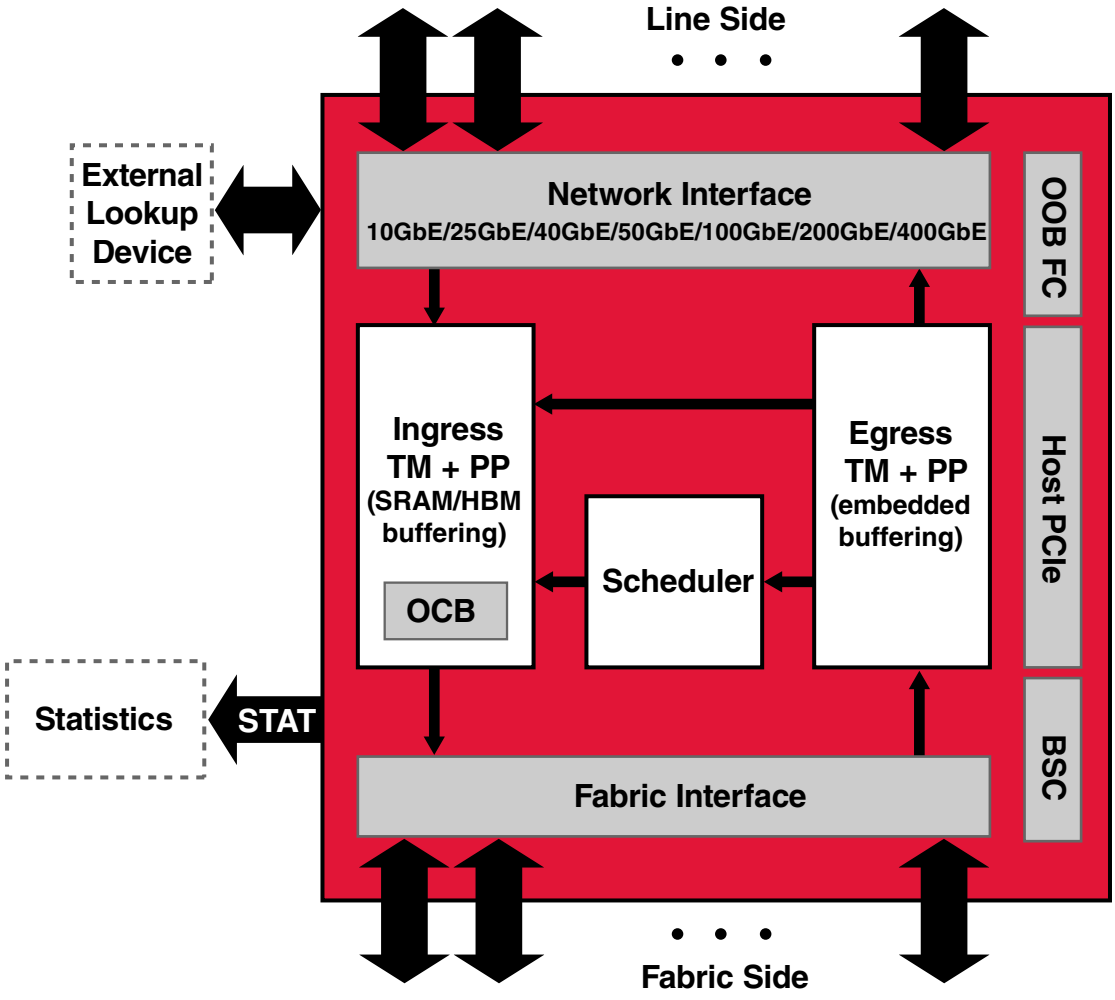
Features (Continued)

- Flexible and programmable packet processor:
  - Bridging, routing, MPLS, VPLS, L2VPNs, L3VPNs, OAM
  - Data center tunneling encapsulations including VXLAN, NV-GRE, and GENEVE
  - Built-in support for data center, carrier and metro Ethernet, and transport applications
  - Large modular on-chip databases, application-oriented with off-chip expandability
  - OAM accelerator engine
  - PEM (flexible pipe)
- Instrumentation and telemetry enhancements:
  - Flow tracker (IPfix)
  - In-band telemetry/IOAM
  - Tail stamping
  - Trajectory trace
- PCIe Gen3 host interface

Applications

- Data center TOR, leaf, spine, core, and DCI
- Carrier Ethernet core/metro/edge switches and routers
- Carrier cloud
- Software-defined networking (SDN)
- Carrier aggregation

Figure 1: Functional Block Diagram



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Chapter 1: Introduction

1.1 Features

The Broadcom® BCM88690 is an integrated packet processor, traffic manager, and fabric interface single-chip switch. The following features are available with the BCM88690:

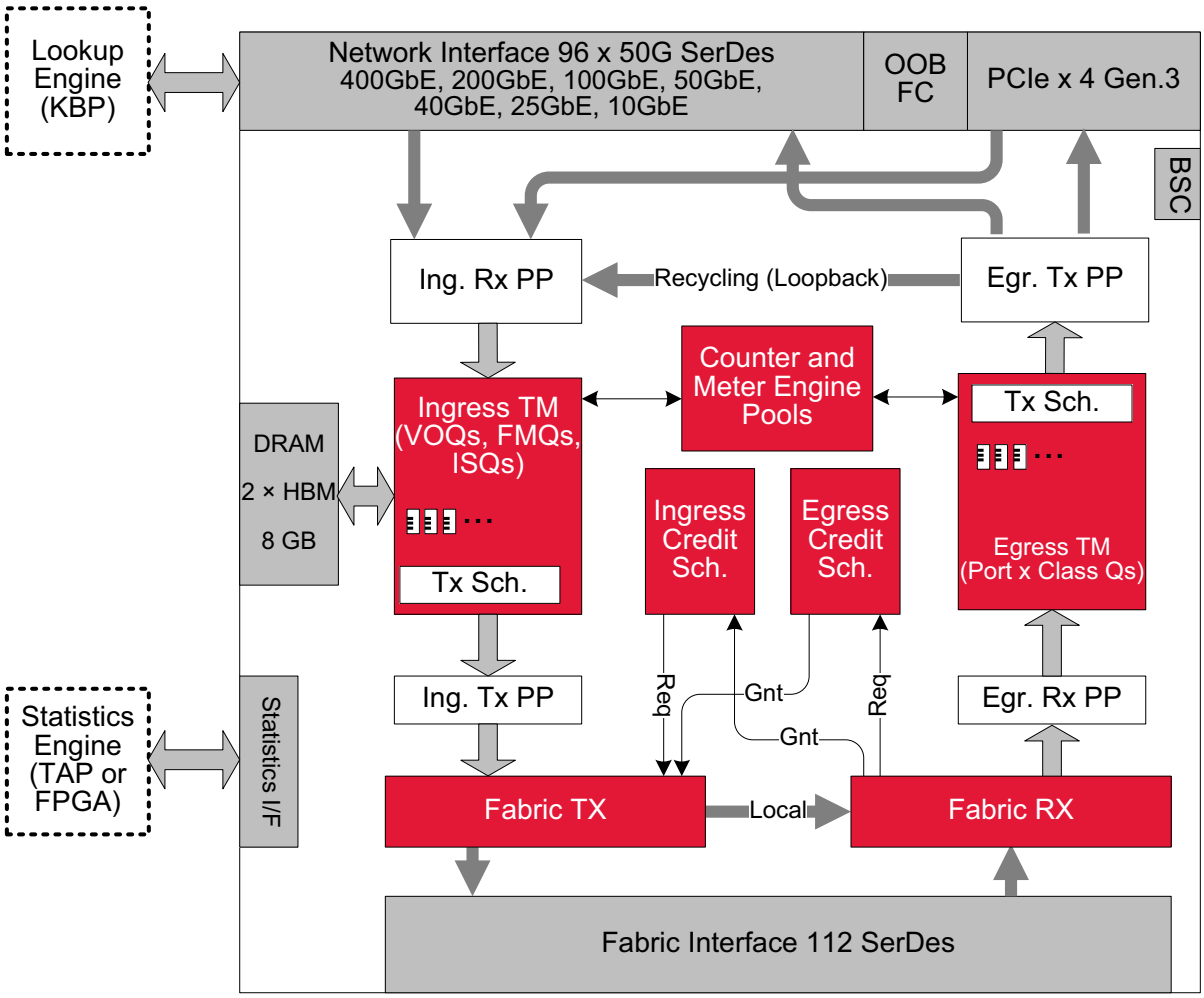
- High performance:
  - 4.8-Tb/s full-duplex, integrated fabric interface, traffic manager, and packet processor.
  - 2000-Mp/s processing rate.
- StrataDNX fabric interface:
  - 112 SerDes for up to 53.125-Gb/s serial links (PAM4 with symbol rate of 26.5625 Gbaud).
  - Mesh configurations of up to four devices.
  - Clos fabric configurations up to 2450 Tb/s (512 devices).
  - Dynamically variable-sized cells for highly efficient segmentation.
  - Multiple line coding options with Reed-Solomon Forward Error Correction (RS-FEC), which optimizes performance according to system characteristics.
  - Dynamic routing and load balancing over all fabric links.
  - 1 + 1, N – x, and N + x redundancy schemes.
  - Automatic fault detection and recovery with no software intervention.
- Flexible network interface:
  - Total of 96 SerDes, with rates up to 53.125 Gb/s.
  - Each of the two device cores has 48 dedicated SerDes that support the following port configurations:
    - 48 × 10GbE/25GbE/50GbE over one lane.
    - 24 × 40GbE/50GbE/100GbE over two lanes.
    - 12 × 40GbE/100GbE/200GbE over four lanes.
    - 6 × 400GbE over eight lanes.
- Packet lengths supported in the range 64B to 10240B.
- Traffic Manager:
  - 64K programmable wire-rate queues.
  - Deep packet buffering.
  - Two integrated HBM Gen2 cubes.
  - Each cube is 4-Hi HBM for a total of 8 GB.
  - Congestion management:
    - Hierarchical WRED and tail-drop policies.
    - Congestion notification – CNM generation and CNM reception (proxy).
    - Flow Control generation – Fully programmable, in-band and out-of-band.
    - Flow Control reception-any level – Interface, port, class, flow, traffic type-in-band and out-of-band.
    - Priority Flow Control (PFC) – Eight levels.
    - Congestion tracking statistics.
    - Up to 192K meters (96K per core).
    - Three ingress meter operations per packet.
    - Two egress meter operations per packet.

  - Hierarchical scheduling and shaping.
    - Fully programmable to any depth.
    - Support for priority propagation.
  - MEF, DSL-FORUM TR-059-compliant scheduling and shaping.
- Packet processor:
  - Bridging, routing, MPLS, VPLS, L2VPNs, L3VPNs, and OAM.
  - Data center tunneling encapsulations including VXLAN, NV-GRE, and GENEVE.
  - Built-in support for data center, carrier and metro Ethernet, and transport applications.
  - Large modular on-chip databases, application oriented with off-chip expandability.
  - OAM accelerator engine.
  - PEM (flexible pipe).
- Counters, meters, and statistics:
  - On-chip counter pool up to 384K counters (192K per core).
  - On-chip meter pool up to 96K dual-bucket meters + 16K single-bucket meters.
  - Statistics interface for expandable, off-chip statistics gathering:
    - The SerDes used for the statistics interface is shared with NIF SerDes.
    - Efficient packet-based protocol based on Ethernet simplifies connectivity to KBP BCM16K, TAP BCM5235, or FPGAs
    - Seamless connection to KBP BCM16K and TAP BCM5235 TAP devices.
- Multicast – Pointer-based ingress and/or egress multicast replication.
- In-band management.
- PCIe × four-lane Gen3 host interface with DMA.
- Hardware linkscan engine.
- LED processor.
- The BCM88690 device is fully interoperable with previous generation of Broadcom StrataDNX devices. BCM88680, BCM88670, BCM88790, and BCM88770 devices may be used in a system simultaneously.

1.2 Device Overview

The following figure is a high-level functional block diagram of the BCM88690.

Figure 2: BCM88690 Block Diagram



As shown in Figure 2, the BCM88690 includes the following functional blocks:

Traffic Manager

- Ingress traffic manager (TM):
  - Manages a pool of queues in on-chip SRAM and in HBM DRAM.
  - Replicates packets for multicast, snooping, and mirroring.
- Ingress and egress end-to-end credit scheduler – Schedules packets out of the ingress TM.
- Egress traffic manager:
  - Manages a pool of egress queues in on-chip memory.
  - Schedules traffic toward packet interfaces – Network, PCIe, internal hosts, and recycling (loopback).
  - Replicates multicast packets.
- Fabric transmit and fabric receive:
  - Segments packet to cells.
  - Transmit – Load-balances cells across fabric SerDes.
  - Receive – Reassembles cells into packets.
- Counter engines:
  - General-purpose counters.
  - Ingress and egress counting.
  - Configurable counting modes and criteria.
- Meter engines:
  - General purpose – A pool of meters for traffic metering.
  - Ingress and egress metering.
  - Applied according to the packet processor command.

Packet Processing

- Ingress receive packet processor:
  - Main packet processing stage.
  - Identifies incoming interface link layer, tunnel, PWE, and AC.
  - Determines where to forward the packet based on packet forwarding header (L2, L3, MPLS, and so on).
  - Appends a packet processor (PP) header.
  - Uses optionally expandable databases using External Lookup (ELK) interface.
- Ingress transmit packet processor:
  - Edits the packet (or packet copy) before transmitting to egress PP.
- Egress receive packet processor:
  - Filters packets according to various criteria.
- Egress transmit packet processor:
  - Edits packets according to PP header (from ingress).

Interfaces

- Network interface:
  - 96 dedicated SerDes up to 53.125 Gb/s (PAM4)
  - Port types supported include 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE, and 400GbE.
- Fabric interface:
  - Up to 112 SerDes.
  - Up to 53.125 Gb/s (PAM4) per link.
  - Reed-Solomon Forward Error Correction (RS-FEC).
- External Lookup Interface:
  - Dedicated External Lookup Interface (ELK) for each of the two cores.
  - Runs over Interlaken interface, using NIF or fabric SerDes.
- Statistics interface:
  - Sharing network interface (NIF) SerDes
  - Use Ethernet ports, up to 400GbE per statistics interface.
  - Generate statistics records over packets.
- Out-of-Band Flow Control (OOBFC):
  - Transmit and receive flow control.
  - SPI 4.2 or ILKN protocol.
- PCIe x4 lane Gen3 host interface:
  - Configuration and status register access.
  - Packet transfer to and from host memory by using DMA.
- BSC (NXP I^2C-compatible) 2-line interface:
  - Basic device debug and register access (PCIe only).
  - PCIe QSPI flash programming.

Chapter 2: System Configurations

2.1 Broadcom StrataDNX Components

The StrataDNX architecture includes two types of components: Fabric Elements (FEs) and Fabric Access Processors (FAPs):

- FEs:
  - Are used to build a Clos fabric.
  - Provide self-routing, cell-based switching.
  - Support both single-stage and multistage fabric configurations.
- FAPs:
  - Provide integrated fabric access and traffic management functions.
  - Provide an integrated packet processor.
  - May be used as a stand-alone TM (ingress, egress, or both) or with a fabric.

2.1.1 Interoperation with StrataDNX Fabric Element Devices

The BCM88690 can interoperate in a system with the following FE devices:

- BCM88790
- BCM88770

2.1.2 Interoperation with StrataDNX Fabric Access Processor Devices

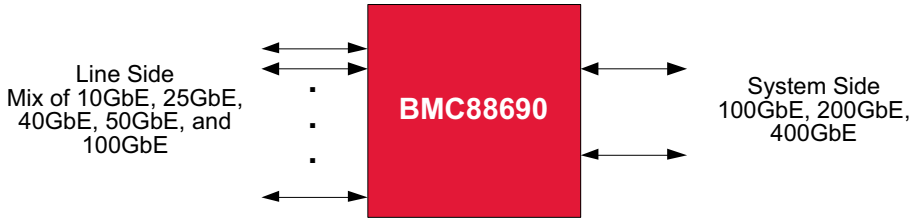
The BCM88690 can interoperate in a system with the following FAP devices:

- BCM88690
- BCM88680
- BCM88670

2.2 Stand-Alone Configurations

The BCM88690 may be used as a stand-alone switch device with ingress/egress intelligent TM. The integrated TM enables intelligent oversubscription with granular, per-flow (or per-customer-and-traffic-class) scheduling and shaping in the upstream and/or the downstream direction.

Figure 3: BCM88690 Switch with Integrated Traffic Manager Example



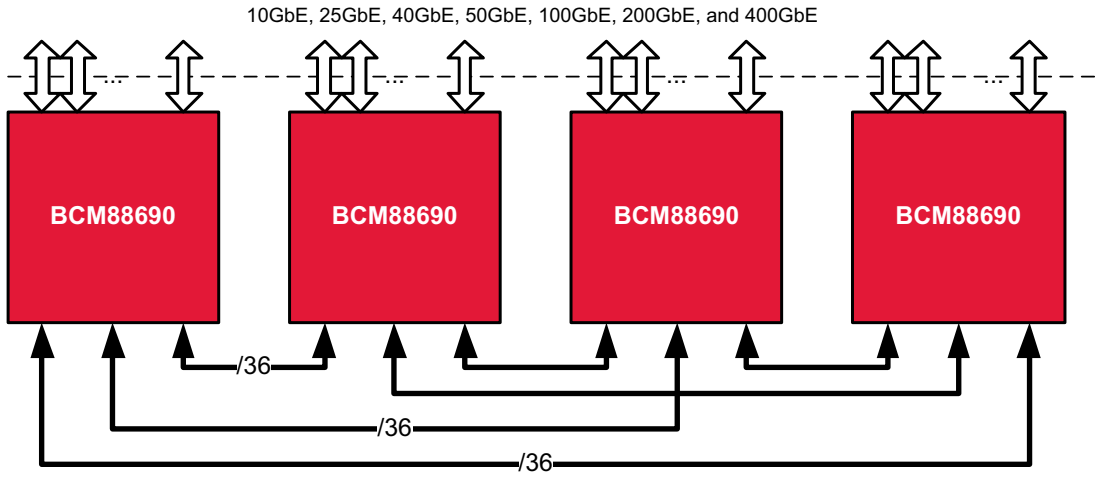
As shown in Figure 3, the BCM88690 offers a flexible set of user interfaces, supporting a mix of 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE, and 400GbE Ethernet ports.

In the upstream direction from the network interfaces into the system, the integrated TM is used to intelligently manage the oversubscription. In the downstream direction, the integrated TM may be used to schedule and shape traffic, possibly per customer and application.

2.3 Mesh Fabric Configurations

The BCM88690 devices may be interconnected in a mesh configuration without the use of StrataDNX fabric elements. In Figure 4, four BCM88690 devices are meshed with 36 links between every pair of devices, providing a net bandwidth of about 1.5 Tb/s between each two BCM88690 devices.

Figure 4: Four BCM88690 Devices in a Mesh Configuration

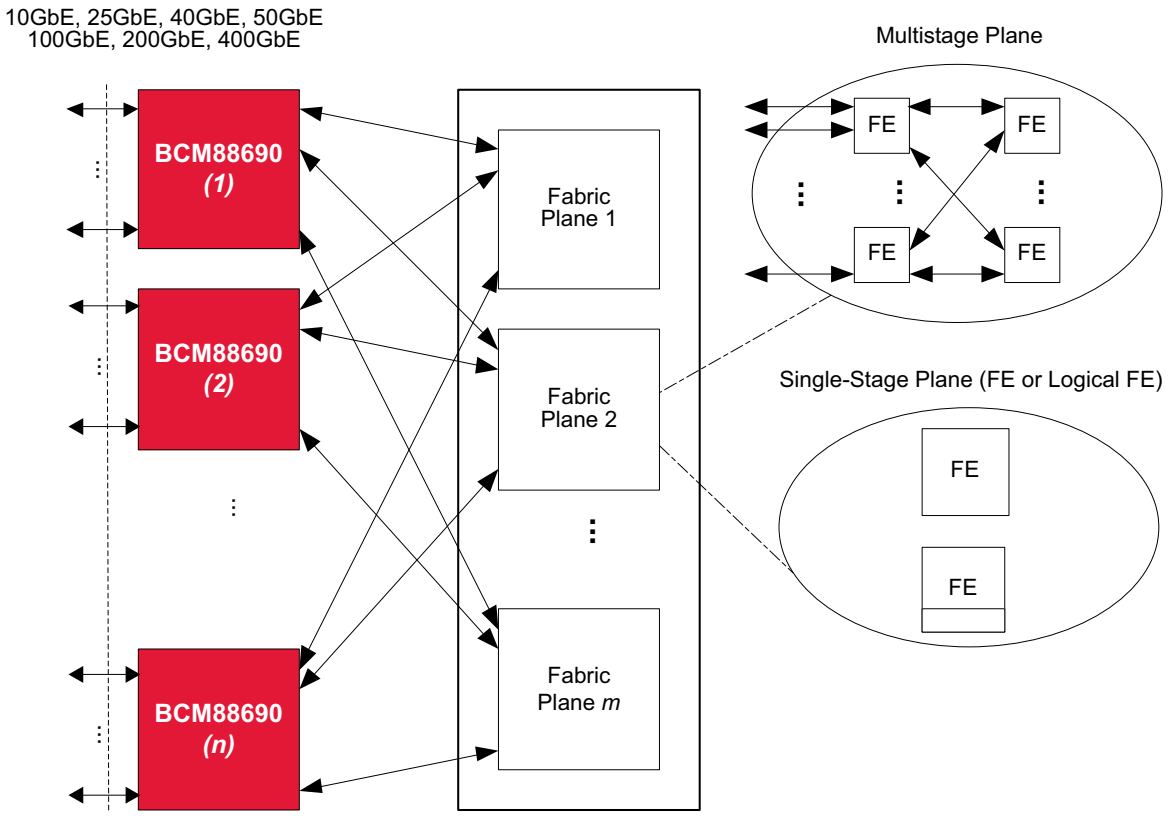


A mesh of three BCM88690 devices is also applicable, connecting 56 links between every pair of devices and creating a fabric-less systems that can support rates above 10 Tb/s. Another option is to connect two BCM88690 devices back-to-back (using all 112 fabric links), creating a 9.6-Tb/s fabric-less switching system.

2.4 StrataDNX CLOS Fabric Configurations

For medium to large nonblocking configurations, a StrataDNX fabric with fabric element devices, for example the BCM88790, is used to interconnect the FAP devices. With the BCM88690, the StrataDNX fabric scales from 4.8 Tb/s to 2500 Tb/s.

Figure 5: FAPs Interconnected by StrataDNX Fabric



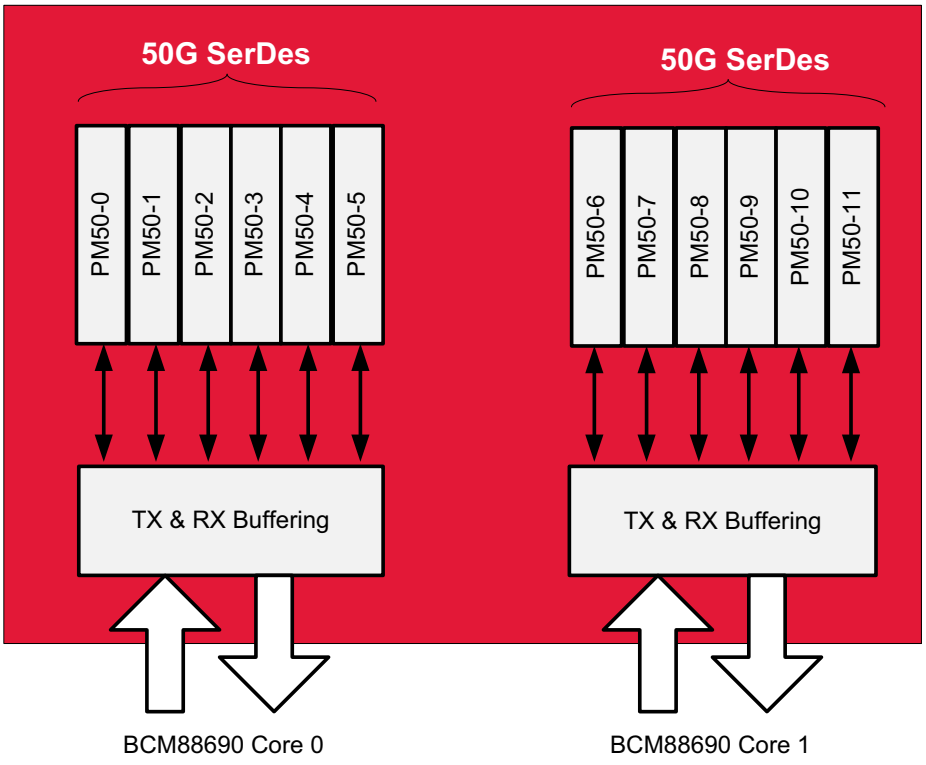
In Figure 5, “n” FAP devices are interconnected through a Clos fabric composed of fabric elements. The number of interconnected FAP devices can range from 1 to 512. A StrataDNX fabric based on the BCM88790 or BCM88770 accommodates a mix of BCM88690, BCM88680, and BCM88670 FAP devices, all of which are interconnected and interoperate simultaneously.

Chapter 3: System Interfaces

3.1 Network Interface

The BCM88690 network interface (NIF) includes 12 PM50s. Six PM50s are connected to core device 0, and six are connected to core 1. Figure 6 shows the BCM88690 network interface and a functional block diagram of the BCM88690 NIF.

Figure 6: BCM88690 Network Interface Block Diagram



As shown in Figure 6, the BCM88690 network interface includes the following items:

- Ethernet Port Macros (PMs):
  - Twelve Ethernet PMs supporting SerDes rates up to 53.125G (PM50).
  - Each PM50 includes an octal SerDes (Blackhawk) supporting up to 53.125G.
  - A group of six PM50 is connected to one device core. PM50-0 to PM50-5 are connected to core 0, and PM50-6 to PM50-11 are connected to core 1.
  - Each PM50 supports the following configurations:
    - 1 × 400GbE port over eight lanes (PAM4)
    - 2 × 200GbE ports over four lanes (PAM4)
    - 4 × 100GbE ports over two lanes (PAM4)
    - 2 × 100GbE ports over four lanes
    - 8 × 50GbE ports over one lane (PAM4)
    - 4 × 50GbE ports over two lanes
    - 4 × 40GbE ports over two lanes
    - 2 × 40GbE ports over four lanes
    - 8 × 25GbE ports over one lane
    - 8 × 10GbE ports over one lane
- Receive buffering:
  - Per port buffer
  - Temporary buffering before injection into the ingress packet processor pipeline.
  - Used for burst absorption in case the total packet rate is higher than the device core processing capability.
  - Interface (link level) flow-control generation.
- Transmit buffering:
  - Temporary buffering before transmission through the Ethernet port.
  - Enable interface (link level) flow-control reception fast reaction time.

Each device core has its own network interfaces. Ethernet ports have hardcoded connections to one of the FAP cores.

3.1.1 Network Interface Configurations

The following table describes the mapping of PMs to SerDes and provides the naming convention of the interfaces.

Table 1: BCM88690 NIF SerDes Interface Mapping

PM	SRD Number	Core ID	Available for ELK[a]
PM50-0	0 to 7	0	ELK 0
PM50-1	8 to 15	0	ELK 0
PM50-2	16 to 23	0	—
PM50-3	24 to 31	0	—
PM50-4	32 to 39	0	—
PM50-5	40 to 47	0	—
PM50-6	48 to 55	1	ELK 1
PM50-7	56 to 63	1	ELK 1
PM50-8	64 to 71	1	—
PM50-9	72 to 79	1	—
PM50-10	80 to 87	1	—
PM50-11	88 to 95	1	—

a. For details on ELK usage, see Section 3.2, External Lookup Engine.

NOTE: Consider distributing network ports and network traffic evenly between the two cores when allocating SerDes for network, ELK, and statistics purposes. An even distribution enables better usage of internal resources.

3.1.2 Ethernet Ports

Ethernet ports are implemented by the Ethernet Port Macro (PM). The PMs include the MAC and PCS layers of Ethernet ports. The BCM88690 includes PM50 based on an octal SerDes block (Blackhawk) that supports SerDes rates up to 53.125 Gb/s.

The following table shows the port modes supported by PM50.

NOTE:

- RS272 FEC is a Broadcom-proprietary protocol to achieve lower latency.
- For 100G and 50G ports using RS-272 FEC mode, the FEC engine serves four SerDes lanes. If using RS-272, no other FEC mode can be used in the same FEC engine.
- BASE-R FEC indicates IEEE 802.3, Clause 74-compliant FEC.

Table 2: PM50 Supported Port Modes

Port Speed	Number of Lanes	Port Mode	SerDes Rate (Gb/s)	VCO Rate (GHz)	SerDes Mode	FEC	Related Standard
400GbE	8	400GAUI-8 C2C	53.125	26.5625	PAM4	RS-544	IEEE 802.3 Annex 120D
		400GAUI-8 C2M	53.125	26.5625	PAM4	RS-544	IEEE 802.3 Annex 120E
		400GBASE-KR8	53.125	26.5625	PAM4	RS-544	This is a 400GAUI-8 with KR interface as defined in IEEE 802.3cd Clause 137
		400GBASE-CR8	53.125	26.5625	PAM4	RS-544	This is a 400GAUI-8 with CR interface as defined in IEEE 802.3cd Clause 136
200GbE	4	200GAUI-4 C2C	53.125	26.5625	PAM4	RS-544	IEEE 802.3 Annex 120D
		200GAUI-4 C2M	53.125	26.5625	PAM4	RS-544	IEEE 802.3 Annex 120E
		200GBASE-KR4	53.125	26.5625	PAM4	RS-544	IEEE 802.3cd Clause 137
		200GBASE-CR4	53.125	26.5625	PAM4	RS-544	IEEE 802.3cd Clause 136
100GbE	2	100GAUI-2 C2C	53.125	26.5625	PAM4	RS-544, RS-272	IEEE 802.3cd Annex 135F
		100GAUI-2 C2M	53.125	26.5625	PAM4	RS-544, RS-272	IEEE 802.3cd Annex 135G
		100GBASE-KR2	53.125	26.5625	PAM4	RS-544, RS-272	IEEE 802.3cd Clause 137
		100GBASE-CR2	53.125	26.5625	PAM4	RS-544, RS-272	IEEE 802.3cd Clause 136
		CAUI-2 C2C	51.5625	25.78125	PAM4	RS-528	IEEE 802.3 (CAUI-4) port, bit muxed to two lanes with C2C interface as defined in IEEE 802.3cd Annex 135F
		CAUI-2 C2M	51.5625	25.78125	PAM4	RS-528	IEEE 802.3 (CAUI-4) port, bit muxed to two lanes with C2M interface as defined in IEEE 802.3cd Annex 135G

Table 2: PM50 Supported Port Modes (Continued)

Port Speed	Number of Lanes	Port Mode	SerDes Rate (Gb/s)	VCO Rate (GHz)	SerDes Mode	FEC	Related Standard
100GbE	4	CAUI-4 C2C	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 Annex 83D
		CAUI-4 C2M	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 Annex 83E
		100GBASE-KR4	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 Clause 93
		100GBASE-CR4	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 Clause 92
		100GAUI-4 C2C	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135D
		100GAUI-4 C2M	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135E
50GbE	1	50GAUI-1 C2C	53.125	26.5625	PAM4	RS-544, RS-272	IEEE 802.3cd Annex 135F
		50GAUI-1 C2M	53.125	26.5625	PAM4	RS-544, RS-272	IEEE 802.3cd Annex 135G
		50GBASE-KR	53.125	26.5625	PAM4	RS-544, RS-272	IEEE 802.3cd Clause 137
		50GBASE-CR	53.125	26.5625	PAM4	RS-544, RS-272	IEEE 802.3cd Clause 136
50GbE	2	Consortium 50G C2C	25.78125	25.78125	NRZ	RS-528, no FEC	Consortium 50GE with C2C interface as defined in IEEE 802.3 Annex 83D
		Consortium 50G C2M	25.78125	25.78125	NRZ	RS-528, no FEC	Consortium 50GE with C2M interface as defined in IEEE 802.3 Annex 83E
		LAUI-2 C2C	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3cd Annex 135B
		LAUI-2 C2M	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3cd Annex 135C
		Consortium 50G KR2	25.78125	25.78125	NRZ	RS-528, no FEC	Consortium 50GbE with KR interface as defined in IEEE 802.3 Clause 93
		Consortium 50G CR2	25.78125	25.78125	NRZ	RS-528, no FEC	Consortium 50GbE with CR interface as defined in IEEE 802.3 Clause 92
		50GAUI-2 C2C	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135D
		50GAUI-2 C2M	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135E
40GbE	2	XLAUI-2 KR	20.625	20.625	NRZ	No FEC	XLAUI-4, bit muxed to two lanes, with KR interface as defined in IEEE 802.3 Clause 93 (masks scaled to 20.625G)
		XLAUI-2 CR	20.625	20.625	NRZ	No FEC	XLAUI-4, bit muxed to two lanes, with CR interface as defined in IEEE 802.3 Clause 92 (masks scaled to 20.625G)
		XLAUI-2 C2C	20.625	20.625	NRZ	No FEC	XLAUI-4, bit muxed to two lanes, with C2C interface as defined in IEEE 802.3 Annex 83D (masks scaled to 20.625G)
		XLAUI-2 C2M	20.625	20.625	NRZ	No FEC	XLAUI-4, bit muxed to two lanes, with C2M interface as defined in IEEE 802.3 Annex 83E (masks scaled to 20.625G)
40GbE	4	XLAUI	10.3125	20.625	NRZ	BASE-R, no FEC	IEEE 802.3 Annex 83A
		40GBASE-KR4	10.3125	20.625	NRZ	BASE-R, no FEC	IEEE 802.3 Clause 84
		40GBASE-CR4	10.3125	20.625	NRZ	BASE-R, no FEC	IEEE 802.3 Clause 85
		XLPPI	10.3125	20.625	NRZ	BASE-R, no FEC	IEEE 802.3 Annex 86A

Table 2: PM50 Supported Port Modes (Continued)

Port Speed	Number of Lanes	Port Mode	SerDes Rate (Gb/s)	VCO Rate (GHz)	SerDes Mode	FEC	Related Standard
25GbE	1	25GAUI C2C	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 Annex 109A
		25GAUI C2M	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 Annex 109B
		25GBASE-KR/ 25GBASE-KR-S	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 Clause 111
		25GBASE-CR/ 25GBASE-CR-S	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 Clause 110
10GbE	1	10GBASE-KR	10.3125	20.625	NRZ	BASE-R, no FEC	IEEE 802.3 Clause 72
		XFI	10.3125	20.625	NRZ	BASE-R, no FEC	XFI+ (FC-PI-3)
		SFI	10.3125	20.625	NRZ	BASE-R, no FEC	SFF-8431
		Direct Attached Cable (DAC)	10.3125	20.625	NRZ	BASE-R, no FEC	—

3.1.2.1 Mixed Port Types on PM50

Different port types can be supported on the same Port Macro (PM). Mixing port types is allowed when all ports in the same PM are derived from one or two PLL rates.

Table 3 defines the PLL (VCO) combinations and available ETH ports on each combination.

NOTE: For Ethernet ports, TVCO (PLL1) and OVCO (PLL0) do not have the same functionality. (See Section 3.1.2.1.1, PM50 Mixed Ports Limitations.)

Table 3: PM50 PLL VCO Combinations and Supported Port Types

			TVCO		25.78125G	25.78125G	25.78125G	26.5625G	26.5625G	26.5625G
			OVCO		20.6250G	Non-ETH[a]	26.5625G	20.6250G	25.78125G	Non-ETH[a]
VCO Rate	**Port BW**	**Lanes**	**SRD Rate**							
26.5625	400GbE	8	53.125				+	+	+	+
26.5625	200GbE	4	53.125				+	+	+	+
26.5625	100GbE	2	53.125				+	+	+	+
26.5625	100GbE	4	26.5625				+	+	+	+
26.5625	50GbE	1	53.125				+	+	+	+
26.5625	50GbE	2	26.5625				+	+	+	+
25.78125	100GbE	2	51.5625		+	+	+		+	
25.78125	100GbE	4	25.78125		+	+	+		+	
25.78125	50GbE	1	51.5625		+	+	+		+	
25.78125	50GbE	2	25.78125		+	+	+		+	
25.78125	25GbE	1	25.78125		+	+	+		+	
20.6250	40GbE	2	20.625		+			+		
20.6250	40GbE	4	10.3125		+			+		
20.6250	10GbE	1	10.3125		+			+		

a. The term “Non-ETH” represents ILKN rates that are not standard ETH rates.

3.1.2.1.1 PM50 Mixed Ports Limitations

The main limitations of the PM50 are as follows:

- Up to eight lanes can be supported.
- Up to two VCO rates can be supported.
- Any modification of TVCO causes ETH ports based on OVCO to be reset as well.

3.1.2.1.2 Software Sequence and Rules for Port Allocation

This section describes the software sequence and rules for port allocation. The goal is to provide a better understanding of the device options. For more information and updates regarding PM50 mixed ports, refer to the *Traffic Manager Programming Gu*ide (88690-PG2xx).

Ports can be allocated to the PM50 by a single port assignment or by a multi-port assignment using the following APIs:

- `bcm_port_resource_set()`
- `bcm_port_resource_multi_set()`

Ports are allocated only if the new configuration meets the TVCO and OVCO combinations in Table 3 and the following software limitations are met:

- Initial allocation (no active ports on the PM):
  - When the initial port allocation has a single VCO:
    - If it is a rate based on 25.78125G or 26.5625G, software allocates it on TVCO.
    - If it is a rate based on 20.625G, software allocates it on OVCO, and 25.78125G or 26.5625G on TVCO (according to the software SOC configuration).
  - When the initial port allocation requires two VCOs, software allocates the fast VCO on TVCO and the slow VCO on OVCO (if ELK-over-ILKN is defined, its rate is allocated to the TVCO).
- Allocation update (active ports on the PM):
  - If all ports in the PM are included in the update command, software treats the update as if this is the initial allocation.
  - If only some of the PM ports are included in the update command, software tries to perform the PLL update without impacting used resources.
  - To update TVCO, all ETH ports using TVCO and OVCO, as well as all ELK-over-ILKN ports using TVCO, should be included in the update command. All of these ports will go through the port-down and port-up sequence. (Only ELK-over-ILKN ports using OVCO are not affected.)
  - To update OVCO, all ETH ports using OVCO and all ELK-over-ILKN ports using OVCO should be included in the update command. All of these ports will go through the port-down and port-up sequence. (Ports using TVCO are not affected).

3.1.2.1.3 PM50 Mixed-Port Allocation Restrictions

The scenarios in this section show examples of configurations that can result in errors.

Scenario I

If a PM is configured using a 40G port (four lanes, VCO = 20.6250G) and a 50G port (two lanes, VCO = 25.78125G), a dynamic configuration adding a 100GbE port (four lanes, VCO = 25.78125G) results in an error indication because more than eight lanes are required.

Scenario II

If a PM is configured using a 40G port (four lanes, VCO = 20.6250G) and a 50G port (two lanes, VCO = 26.5625G), a dynamic configuration that adds a 50GbE port (two lanes, VCO = 25.78125G) results in an error indication because three VCO rates are required.

Scenario III

Static configuration of a 1 × 200GbE port (four lanes, VCO = 26.5625G), and 4 × 10GbE ports (four lanes, VCO = 20.6250G) results in {PLL1 = 26.5625G, PLL0 = 20.6250G}.

A dynamic configuration that replaces the 200GbE port with a 100GbE port (four lanes, VCO = 25.78125G) results in an error indication because PLL1 should be updated, causing a port-down event on the 10GbE ports as well.

If it is acceptable to allow the 10GbE ports to go down and back up, they should be added to the allocation update (by using bcm_port_resource_multi_set).

3.1.2.2 400GbE Port

The BCM88690 device supports standard 400GbE according to IEEE 802.3.

The 400GbE port supports the following interfaces:
- 400GAUI-8 (chip-to-chip IEEE 802.3 Annex 120D and chip-to-module IEEE 802.3 Annex 120E)
- 400GBASE-KR8 (This is 400GAUI-8 with a KR interface as defined in IEEE 802.3cd Clause 137.)
- 400GBASE-CR8 (This is 400GAUI-8 with a CR interface as defined in IEEE 802.3cd Clause 136.)

When using the 400GbE port, Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3 Clause 119, RS(544,514).

3.1.2.3 200GbE Port

The BCM88690 device supports standard 200GbE according to IEEE 802.3 and IEEE 802.3cd.

The 200GbE port supports the following interfaces:
- 200GAUI-4 (chip-to-chip IEEE 802.3 Annex 120D and chip-to-module IEEE 802.3 Annex 120E)
- 200GBASE-KR4 (IEEE 802.3cd Clause 137)
- 200GBASE-CR4 (IEEE 802.3cd Clause 136)

When using the 200GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3 Clause 119, RS(544,514).

3.1.2.4 100GbE Port

3.1.2.4.1 100GbE over Two Lanes

The BCM88690 device supports standard 100GbE according to IEEE 802.3cd.

The 100GbE port supports the following interfaces:
- 100GAUI-2 (chip-to-chip IEEE 802.3cd Annex 135F and chip-to-module IEEE 802.3cd Annex 135G)
- 100GBASE-KR2 (IEEE 802.3cd Clause 137)
- 100GBASE-CR2 (IEEE 802.3cd Clause 136)
- CAUI-2, which is the IEEE 802.3 (CAUI-4) port bit muxed to two lanes (chip-to-chip and chip-to-module)

When using the 100GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3 Clause 91, both RS(528,514) and RS(544,514).

3.1.2.4.2 100GbE over Four Lanes

The BCM88690 device supports standard 100GbE according to IEEE 802.3.

The 100GbE port supports the following interfaces:
- CAUI-4 (chip-to-chip IEEE 802.3 Annex 83D and chip-to-module IEEE 802.3 Annex 83E)
- 100GBASE-KR4 (IEEE 802.3 Clause 93)
- 100GBASE-CR4 (IEEE 802.3 Clause 92)
- 100GAUI-4 (chip-to-chip IEEE 802.3cd Annex 135D and chip-to-module IEEE 802.3cd Annex 135E)

When using the 100GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3 Clause 91, both RS(528,514) and RS(544,514).

3.1.2.5 50GbE Port

3.1.2.5.1 50GbE over One Lane

The BCM88690 supports 50GbE according to IEEE 802.3cd.

The 50GbE port supports the following interfaces:

- 50GAUI-1 (chip-to-chip IEEE 802.3cd Annex 135F and chip-to-module IEEE 802.3cd Annex 135G)
- 50GBASE-KR (IEEE 802.3cd Clause 137)
- 50GBASE-CR (IEEE 802.3cd Clause 136)

When using the 50GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3 Clause 134, RS(544,514).

3.1.2.5.2 50GbE over Two Lanes

The BCM88690 supports 50GbE according to IEEE 802.3cd and the 25G/50G Ethernet consortium.

The 50GbE port supports the following interfaces:

- 50GbE over two lanes according to the 25G/50G Ethernet consortium
- LAUI-2 (chip-to-chip IEEE 802.3cd Annex 135B and chip-to-module IEEE 802.3cd Annex 135C)
- 50GBASE-KR2 (This is Ethernet consortium 50GbE with a KR interface as defined in IEEE 802.3 Clause 93.)
- 50GBASE-CR2 (This is Ethernet consortium 50GbE with a CR interface as defined in IEEE 802.3 Clause 92.)
- 50GAUI-2 (chip-to-chip IEEE 802.3cd Annex 135D and chip-to-module IEEE 802.3cd Annex 135E)

When using the 50GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant to IEEE 802.3 Clause 134, RS(544,514), or Clause 91, RS(528,514).

3.1.2.6 40GbE Port

3.1.2.6.1 40GbE over Two Lanes

The BCM88690 supports standard 40GbE according to IEEE 802.3.

The 40GbE ports support the following interfaces:

- XLAUI-2 – This is XLAUI-4, bit-muxed to two lanes, with a KR interface as defined in IEEE 802.3 Clause 93 (masks scaled to 20.625G).
- XLAUI-2 – This is XLAUI-4, bit-muxed to two lanes, with a CR interface as defined in IEEE 802.3 Clause 92 (masks scaled to 20.625G).
- XLAUI-2 – This is XLAUI-4, bit-muxed to two lanes, with a chip-to-chip interface as defined in IEEE 802.3 Annex 83D (masks scaled to 20.625G).
- XLAUI-2 – This is XLAUI-4, bit-muxed to two lanes, with a chip-to-module interface as defined in IEEE 802.3 Annex 83E (masks scaled to 20.625G).

No FEC is supported for the 40GbE port over two lanes.

3.1.2.6.2 40GbE over Four Lanes

The BCM88690 supports standard 40GbE according to IEEE 802.3.

The 40GbE ports support the following interfaces:

- XLAUI (IEEE 802.3 Annex 83A)
- 40GBASE-KR4 (IEEE 802.3 Clause 84)
- 40GBASE-CR4 (IEEE 802.3 Clause 85)
- XLPPI (IEEE 802.3 Annex 86A)

When using the 40GbE port in four-lane mode, an optional FEC is supported. The FEC is compliant to IEEE 802.3 Clause 74.

3.1.2.7 25GbE Port

The BCM88690 supports 25GbE according to IEEE 802.3, and the 25G/50G Ethernet consortium.

The 25GbE ports support the following interfaces:

- 25GAUI (chip-to-chip IEEE 802.3 Annex 109A and chip-to-module IEEE 802.3 Annex 109B)
- 25GBASE-KR/25GBASE-KR-S (IEEE 802.3 Clause 111)
- 25GBASE-CR/25GBASE-CR-S (IEEE 802.3 Clause 110)

When using the 25GbE port, an optional FEC is supported. The FEC can be either IEEE 802.3 Clause 108, RS(528, 514) or IEEE 802.3 Clause 74 FEC.

3.1.2.8 10GbE Port

The BCM88690 supports 10GbE port according to IEEE 802.3.

The 10GbE ports support the following interfaces:

- XFI or SFI for direct connect to optical module[1]
- 10GBASE-KR (IEEE 802.3 Clause 72)
- Direct-attach cable (DAC)

When using the 10GbE port with the KR interface, an optional FEC is supported. The FEC is compliant to IEEE 802.3 Clause 74.

1. Supported: SR (limiting), LR (limiting), ER (limiting).
   Not supported: ZR (limiting), ZR (linear), LRM (linear), DWDM (linear).

3.2 External Lookup Engine

The packet processing engine uses various types of databases. To address the requirement of some applications for greater database capacity, the BCM88690 supports the expansion of some databases with the use of an External Lookup (ELK) interface. The BCM88690 has two ELK interfaces: one for each processing core. For an application that requires database expansion, use both of the ELK interfaces and connect them to the external KBP device.

NOTE: The BCM88690 does not support MAC table expansion over the ELK interface.

The BCM88690 ELK interface is designed to connect directly to Broadcom Knowledge-based Processor (KBP) devices.

NOTE: The KBP devices have two Interlaken (ILKN) ports. One KBP device can support a single BCM88690 device.

Each ELK interface uses a dedicated ILKN interface and can be connected over either NIF SerDes or Fabric SerDes.

3.2.1 ILKN FEC

The BCM88690 supports optional RS-FEC on the Interlaken interface used for ELK. The FEC is compliant to FEC extension of the Interlaken Reed-Solomon Forward Error Correction Extension Protocol Definition from the Interlaken Alliance.

The following FEC usage guidelines apply to the ELK-ILKN interfaces:

- For an ELK-ILKN interface using a SerDes rate of up to 30G in NRZ mode, FEC is optional.
- For an ELK-ILKN interface using a SerDes rate above 30G in PAM4 mode, FEC is mandatory.
- When using non-FEC NRZ mode, 16 lanes are available per port.
- When using FEC mode (NRZ or PAM4), only 12 lanes are available per port.

3.2.2 ELK SerDes Connectivity Options

Table 4 summarizes the connectivity options for ELK interface 0, and Table 5 summarizes the connectivity options for ELK interface 1.

Table 4: ELK 0 Connectivity Options

Interface	FEC Mode	SerDes Number	Comments
NIF	Without FEC	0 to 15	NIF PM50-0, PM50-1
	With FEC	0 to 11	NIF PM50-0, and 4 lower lanes from PM50-1
Fabric	Without FEC	0 to 15	FAB Octets 0, 1
	With FEC	0 to 11	FAB Octet 0, and 4 lower lanes from Octet 1

Table 5: ELK 1 Connectivity Options

Interface	FEC Mode	SerDes Number	Comments
NIF	Without FEC	48 to 63	NIF PM50-6, PM50-7
	With FEC	48 to 59	NIF PM50-6, and 4 lower lanes from PM50-7
Fabric	Without FEC	56 to 71	FAB Octets 7, 8
	With FEC	56 to 67	FAB Octet 7, and 4 lower lanes from Octet 8

NOTE: Consider distributing network ports and network traffic evenly between the two cores when allocating SerDes for network, ELK, and statistics purposes. An even distribution enables better usage of internal resources.

3.2.3 ELK (over ILKN) SerDes Supported Rates and Electrical Standards

The ELK-over-ILKN interface is targeted to comply with the electrical specifications of the standards as listed in Table 6.

Table 6: ELK-over-ILKN Supported Rates and Electrical Specifications Standards

SerDes Rate (Gb/s)	SerDes Mode	Standard Electrical Specifications
53.125	PAM4	200GAUI-4 C2C: IEEE 802.3 Annex 120D
		200GAUI-4 C2M: IEEE 802.3 Annex 120E
25.78125	NRZ	CAUI-4 C2C: IEEE 802.3 Annex 83D
		CAUI-4 C2M: IEEE 802.3 Annex 83E

3.3 Out-of-Band Flow Control

The BCM88690 supports Out-of-Band Flow Control (OOBFC) from the user to the BCM88690 (egress flow control or reception) and from the BCM88690 to the user (ingress flow control or generation).

The BCM88690 has two independent bidirectional OOBFC interfaces. Each interface can work in SPI-4.2 mode or Interlaken mode.

In all modes, the OOBFC interface supports the following:

- Reception – Each calendar entry is mapped to a flow-control reaction point that is either:
  - Link-level (NIF port)
  - Channel-level (OTM port)
  - Priority-level (egress queue pair)
- Generation (flow-control transmission) – Each calendar entry represents a flow-control generation point that is either:
  - Status of a virtual-statistics queue
  - Status of the global resources, in other words, DRAM buffers
  - Status of port (MAC) receive buffer (link level)
- XON/XOFF signaling (no concept of credits, like SPI-4.2)

In SPI-4.2 mode, the OOBFC interface has the following characteristics:

- SPI-4.2 status channel-like framing
- Calendar length of up to 512
- Three-wire signaling for each direction—Two data, one clock (support XON/XOFF indications):
  - On TX STARVING = XON and SATISFIED = XOFF
  - On RX XON = (HUNGRY or STARVING) and XOFF = SATISFIED
- SDR operation for data signals
- Transmission clock rate: Core frequency divided by 6, 8, 10, 12, 14, or 16 (maximum rate is 166 MHz)
- Reception clock rate: DC to 200 MHz

In Interlaken mode, the OOBFC interface has the following characteristics:

- Interlaken protocol
- Calendar length of up to 512
- Reception and generation of Interlaken retransmit requests
- Three-wire signaling for each direction—One each for: clock, data, sync
- 4b CRC protection
- DDR operation for data and sync signals
- Transmission clock rate: Core frequency divided by 6, 8, 10, 12, 14, or 16 (maximum rate is 166 MHz)
- Reception clock rate: DC to 180 MHz

NOTE: In-band and out-of-band flow-control signaling may be used simultaneously.

3.4 Synchronous Ethernet

The BCM88690 supports Synchronous Ethernet (SyncE) applications. The support includes two functions: controlling the transmit clock of network ports, and recovering a clock from a network port.

3.4.1 Transmit Clock

The transmit clock of each SerDes is locked to one of the external reference clocks driving the NIFx_LCPLL_REFCLK_P/N input pins.

By connecting the system transmit clock to the NIFx_LCPLL_REFCLK_P/N inputs, it is possible to control the transmit clock of the SerDes.

3.4.2 Recovered Clock

The BCM88690 can provide up to two recovered clocks that may be used as reference clocks for an external synchronization unit. The source for the recovered clocks can be any of the NIF SerDes configured as an Ethernet port. The BCM88690 drives two recovered clocks, each as a differential signal. Two additional pads are used for VALID indication, one per recovered clock

NOTE: Clock recovery is supported for a NIF interface configured as an Ethernet port. It is not supported for fabric or Inerlaken ports.

The VALID indication is asserted when the clock is good, and the clock may be used for synchronization. The VALID indication may be configured to operate based on PCS lock or based on link-up indication.

The clock at the SYNCE_[1:0]_CLK_OUT_P/N pins is the CDR output of the relevant SerDes. The output for these clocks is halted if the clock is not valid.

If there are multilane ports (for example, 40GbE and 100GbE), the recovered clock is derived from the first SerDes of the relevant port, and the VALID signal is according to PCS status of the whole port.

The recovered clock frequency is 25 MHz.

NOTE: An external clock filtering device is required to clean the recovered clock before using it as a reference for the rest of the system.

3.5 IEEE 1588

The BCM88690 is a highly integrated device with many hardware hooks for designs that require network time synchronization. The following features make the device ideally suited for time synchronization applications that comply with IEEE 1588:

- Supported modes:
  - E2E and P2P Transparent clock (TC).
  - Boundary clock (BC).
  - TC + OC timeReceiver, BC + OC timeReceiver.
- One-step clock features:
  - On-the-fly egress packet modification including UDP checksum update and CRC update.
  - All modifications to the correction field are handled in hardware.
  - Very short residence time.
  - All packets timestamped on ingress.
  - Uses switch-packet processing engines to identify IEEE 1588 packets.
- Two-step features:
  - Egress timestamps are stored in per-port FIFO, along with IEEE 1588 sequence number.
  - The CPU can indicate which packets should generate a timestamp on egress.
  - All packets are timestamped on ingress.
  - Uses switch packet processing engines to identify IEEE 1588 packets and trap to CPU.
- Synchronizable timestamp counter:
  - Can be phase-locked to external source.
  - BroadSync® (timecode + event clock) interface.
  - Broadcom PHY Sync interface.
  - Timestamped GPIOs.
- Frequency synthesizer:
  - Additional clock divider: 10 MHz + 1 pps.
  - Low jitter.

NOTE: PTP/IEEE 1588 functionality is supported over network (NIF) Ethernet ports only. Timestamping is not supported over fabric or Interlaken interfaces.

3.5.1 BroadSync External Interfaces

The BroadSync block provides the following external interfaces for providing timing information to off-chip devices or for retrieving timing information from external devices:

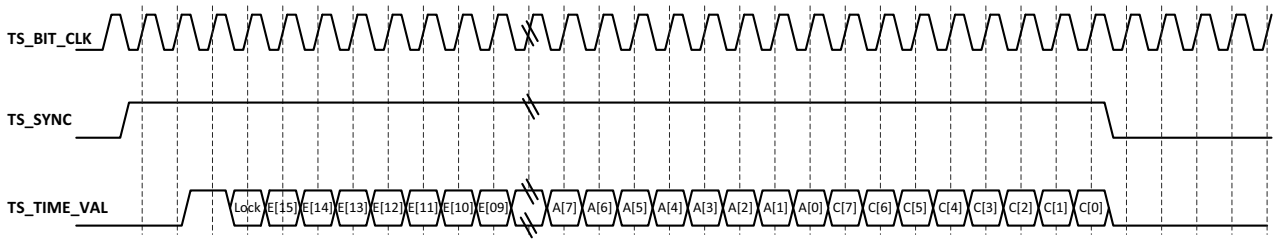
- Reference clock (input)
- External Sync 1 (input or output)
- External Sync 2 (input or output)
- 3-pin BroadSync interface (input or output):
  - TS_BIT_CLK
  - TS_SYNC
  - TS_TIME_VAL

The reference clock input is used for the clocking of all of the logic in the BroadSync block. The BroadSync block operates on a separate clock domain than the rest of the switch logic. The reference clock input should be driven from a low-jitter source to ensure that all time-related functions are accurate.

The External Sync 1 and 2 signals can be used as either inputs or outputs. When the signals are being used as inputs, a rising edge on the signal can be used to sample the current value of the internal timer, which can then be retrieved by the CPU. When these signals are being used as outputs, the signal can be programmed to toggle based on a configurable interval.

The BroadSync interface is configured through the CMIC_BS_CONFIG register and is composed of three signals: the clock, the heartbeat, and the time code. The BroadSync interface can be configured to operate as either a timeTransmitter (output) or timeReceiver (input). The interface clocks out or takes in serial data as shown in Figure 7.

Figure 7: BroadSync Interface I/O



When the BroadSync interface is operating in timeReceiver mode, an external device is used to clock a time code into the BCM88690. External hardware provides the TS_BIT_CLK, TS_SYNC, and TS_TIME_VAL signals. During each heartbeat period, the external hardware shifts in a time code value, which consists of the following:

- Start bit
- Lock bit
- 16-bit epoch
- 32-bit seconds
- 2-bit zero
- 30-bit nanoseconds
- 8-bit accuracy
- CRC8 (covers all bits from LOCK to ACCURACY[0])

The time value shifted in corresponds to the time of the most recent rising edge of the heartbeat signal. All of the bits clocked in from the time code are stored in the CMIC_BS_INPUT_TIME[0:2] registers. Additionally, the received CRC8 is compared against the computed CRC8, and the result of the comparison is present in the CHECKSUM_ERROR field in the CMIC_BS_INPUT_TIME_2 register.

The internal time value is calibrated to the external signals through the following process:

1. The rising edge of TS_SYNC is used to sample the device's internal free-running clock value.
2. The sampled free-running clock value is compared to the time value subsequently shifted in using the TS_TIME_VAL signal.
3. These pairs of values (shifted-in time and sampled free-running time) are provided to the CPU on an occasional basis.
4. The differences and rates of change of the differences of the two time bases are used to a derive drift value.
5. The computed drift value is used to correct the internal time counter.

When the BroadSync interface is operating in timeTransmitter mode, the interface is used to drive a time code to external devices. How frequently a new time code is clocked out depends on how often the heartbeat signal goes high. The heartbeat signal toggling frequency can be configured through the CMIC_BS_HEARTBEAT_CTRL register. When the heartbeat goes high, the contents of the CMIC_BS_OUTPUT_TIME memory is clocked out. The BCM88690 automatically computes and appends the correct CRC8 value immediately after the 8-bit accuracy field is clocked out. The TS_BIT_CLK used to clock out the time code is synthesized from the BroadSync Clock domain.

The BCM88690 can optionally synthesize the TS_BIT_CLK from a highly accurate internal PLL. The PLL generates an extremely low-jitter clock that is ITU-T G.824 and ITU-T G.823 compliant.

3.6 Fabric Interface

The fabric block integrates 112 SerDes links. The SerDes core is an octal (x8) lane 53.125-Gb/s PAM4 or 25.78125-Gb/s NRZ and is suitable for optical and backplane applications. The SerDes core has two PLLs that can be configured independently, and each lane can select between the two VCO clocks. The SerDes core supports data rates from 23.0 Gb/s to 25.78125 Gb/s in NRZ (backward-compatible with the BCM88770) and a data rate of up to 53.125 Gb/s in PAM4 mode. Each lane can be configured independently to run in PAM4 or NRZ modes with one of the two PLLs' configured rates. For example, supported rates per lane can be one of the following rates: 50/25 Gb/s (PLL-0) or 23/11.5 (PLL-1).

SerDes supports a built-in PRBS functionality. PRBS is also supported on the fabric MAC layer per lane.

The following table lists the supported SerDes rates as well as the associated electrical specification standards.

Table 7: Fabric Supported Rates and the Electrical Specifications Standards

SerDes Rate (Gb/s)	SerDes Mode	Standard Electrical Specifications
53.125	PAM4	50GBASE-CR: IEEE 802.3cd Clause 136
		50GBASE-KR: IEEE 802.3cd Clause 137
		50GAUI-1 C2C: IEEE 802.3cd Annex 135F
		50GAUI-1 C2M: IEEE 802.3cd Annex 135G
50	PAM4	50GBASE-KR: IEEE 802.3cd Clause 137[a]
25.78125	NRZ	100GBASE-CR4: IEEE 802.3 Clause 92
		100GBASE-KR4: IEEE 802.3 Clause 93
		CAUI-4 C2C: IEEE 802.3 Annex 83D
		CAUI-4 C2M: IEEE 802.3 Annex 83E
25	NRZ	100GBASE-KR4: IEEE 802.3 Clause 93[a]
23	NRZ	100GBASE-KR4: IEEE 802.3 Clause 93[a]

a. Scaled to the appropriate rate.

NOTE: For more information about the supported rates, see Table 45, Fabric SerDes Supported Rates.

3.6.1 PCS Layer Line Coding

Each fabric link supports one of the following line coding options:

- 64b/66b encoding
- 25G Reed-Solomon FEC
- Low-Latency 25G Reed-Solomon FEC
- 50G Reed-Solomon FEC
- Low-Latency 50G Reed-Solomon FEC

3.6.1.1 64b/66b Encoding

The 64b/66b line coding is based on the standard 10GbE 64b/66b coding (IEEE 802.3 Clause 49). KR-FEC is not supported.

The effective bandwidth of 64b/66b is ~97% (64b/66b) of the SerDes rate.

3.6.1.2 25G Reed-Solomon FEC (RS-FEC)

The RS-FEC is based on the Reed-Solomon error correction code and can be configured on a per-link basis.

For 25-Gb/s links, the BCM88690 supports RS (206, 196, t=5) coding using 10-bit symbols. This means that each 2060-bit frame consists of 1960 bits of data and 100 bits RS Syndrome, which is used by the decoder to correct errors.

The selected code is able to correct any five symbols in the frame. This RS code can correct any single-error burst of 41 bits per RS frame, and up to 50 bits of error burst if it spans no more than five symbols.

Out of the 1960 data bits of the RS-FEC frame, the BCM88690 uses only 1950 bits for real data and 10 bits as overhead. The effective bandwidth of a link running RS-FEC is ~93.2% of the link rate (64/65 × 1950/2060).

The 25G RS-FEC decoder on the receive side adds a delay equivalent to ~1.5 RS-FEC frame time (the computation logic takes ~0.5 FEC frame time). For example, RS-FEC adds a latency of ~130 ns on 23-Gb/s links (~116 ns on 25.78125-Gb/s links).

The RS-FEC supports the option to indicate uncorrectable RS-FEC frames. When enabled, the RX MAC drops all cells that are part of an uncorrectable RS-FEC frame. Enabling this indication adds one additional RS-FEC frame time delay (total of ~2.5 RS-FEC frame time). For example, RS-FEC with error indication adds a latency of ~220 ns on 23-Gb/s links (~196 ns on 25.78125-Gb/s links).

3.6.1.3 Low-Latency 25G Reed-Solomon FEC (LL 25G RS-FEC)

The BCM88690 supports a lower-latency version of the RS-FEC (for 25 Gb/s links only). The LL 25G RS-FEC is based on the same 25G RS (206, 196, t=5) coding using 10-bit symbols; however, only half the data is transmitted. The LL 25G RS-FEC code is able to correct any five symbols in the frame, which is the same as 25G RS-FEC.

The LL 25G RS-FEC transmitted frame is 1080 bits (975 data bits, 5 overhead bits and 100 RS Syndrome bits). The effective bandwidth of a link running LL 25G RS-FEC is ~88.9% of the link rate (64/65 × 975/1080).

The LL 25G RS-FEC has a delay equivalent to ~2 LL 25G RS-FEC frame time (computation logic takes ~1 LL 25G RS-FEC frame time) and ~3 LL 25G RS-FEC frame time when the uncorrectable error indication is enabled. For example, LL 25G RS-FEC adds a latency of ~84 ns on 23-Gb/s links without uncorrectable error indication (~76 ns on 25.78125-Gb/s links) and ~131 ns on 23-Gb/s links when uncorrectable error indication is enabled (~118 ns on 25.78125-Gb/s links).

3.6.1.4 50G Reed-Solomon FEC (RS-FEC)

For 50-Gb/s links, the BCM88690 supports RS (545, 515, t=15) coding using 10-bit symbols. This means that each 5450-bit frame consists of 5150 bits of data and 300 bits RS Syndrome, which the decoder uses to correct errors.

This code is able to correct any 15 symbols in the frame. This RS code can correct any single error burst of 141 bits per RS frame, and up to 150 bits of error burst if it spans no more than 15 symbols.

Out of the 5150 data bits of the RS-FEC frame, the BCM88690 uses only 5056 bits for real data. The effective bandwidth of a link running RS-FEC is ~92.7% of the link rate (5056/5450).

The 50-Gb/s RS-FEC decoder on the receive side adds a delay equivalent to ~1.8 RS-FEC frame time (the computation logic takes ~0.8 FEC frame time). For example, RS-FEC adds a latency of ~185 ns on 53.125-Gb/s links.

3.6.1.5 Low-Latency 50G Reed-Solomon FEC (LL 50G RS-FEC)

The BCM88690 supports a lower-latency version of the 50G RS-FEC. The LL 50G RS-FEC is based on the same 50G RS (545, 515, t=15) coding using 10-bit symbols; however, only half the data is transmitted. The LL 50G RS-FEC code is able to correct any 15 symbols in the frame, which is the same as 50G RS-FEC.

The LL 50G RS-FEC transmitted frame is 3040 bits (2688 data bits). The effective bandwidth of a link running LL 50G RS-FEC is ~88.4% of the link rate. The LL 50G RS-FEC has a delay equivalent to ~2 LL 50G RS-FEC frame time (computation logic takes ~1 LL 50G RS-FEC frame time) and ~3 LL 50G RS-FEC frame time when the uncorrectable error indication is enabled.

3.6.1.6 Line Coding Overheads and FEC Latency

Table 8 and Table 9 show technical specifications for the line coding options.

Table 8: Line Coding Overheads

Code	Block Length (Bits)	Data Length (Bits)	Utilization	SerDes Rate (Gb/s)	Encoded SerDes Rate (Gb/s)
64b/66b	66	64	96.97%	23	22.3
25G RS-FEC	2060	1920	93.20%	23	21.43
Low-Latency 25G RS FEC	1080	975	88.9%	23	20.45
64b/66b	66	64	96.97%	25.78125	25
25G RS-FEC	2060	1920	93.20%	25.78125	24
Low-Latency 25G RS FEC	1080	975	88.9%	25.78125	22.92
50G RS-FEC	5450	5150	92.7%	50	46.35
50G RS-FEC	5450	5150	92.7%	53.125	49.24
Low-Latency 50G RS FEC	3040	2688	88.4%	50	44.21
Low-Latency 50G RS FEC	3040	2688	88.4%	53.125	46.97

Table 9: FEC Latency

Code	Frame Size (Bits)	SerDes Rate (Gb/s)	Frame Transmit (ns)	Total without Marking (ns)	Total with Marking (ns)
25G RS-FEC	2060	23	90	130	220
Low-Latency 25G RS FEC	1080	23	47	84	131
25G RS-FEC	2060	25.78125	80	116	196
Low-Latency 25G RS FEC	1080	25.78125	42	76	118
50G RS-FEC	5450	50	109	198	307
50G RS-FEC	5450	53.125	102.6	184.6	287.2

3.6.2 Fabric SerDes Connectivity

When connecting devices using fabric SerDes, use the following guidelines:

- Minimize the maximum cable length. Using a cable length greater than 100 meters or using three pipes requires special approval from Broadcom.
- Minimize the cable length variance. It is recommended to use similar cable lengths for all links.
- To be able to support link level flow control (LLFC), the device has further requirements. When a link input FIFO is building up, LLFC is asserted to prevent input FIFO overflow. When the LLFC is deasserted, the input FIFO should have enough data to prevent the FIFO from getting empty, resulting in potential performance loss. The LLFC assertion/deassertion threshold must be able to handle the LLFC delivery time, as well as data in-flight, which depends on various parameters. The significant parameters are the PCS line encoding, the cell size, and the cable length. The LLFC settings depend on the size of the input-link FIFO:
  - In single-pipe mode the input-link FIFO size is 512 entries of 128 bytes per link (using the memory from the other pipes).
  - In two-pipe mode in the BCM88690, the input-link FIFO size can be set to 256 entries of 128 bytes.
  - In three-pipe mode, the input-link FIFO size is 170 entries of 128 bytes per link, per pipe.

Table 10 describes the cable length limitations when the BCM88690 requires generating LLFC indication, which is calculated according to the BCM88690 input link FIFO size. The LLFC cable length limitations of a link partner device must be calculated separately and may be greater or lesser than the data presented in this table.

Table 10: LLFC Fiber-Optic Cable Length Summary

Number of Fabric Pipes	Max. Link Rate (Gb/s)	Uncorrectable Error Marking?	Line Coding	Cable Length (Meters)	Remark
Single	53.125	Any	Any	100	—
Single	50	Any	Any	100	—
Single	25.78125	Any	Any	100	—
Two	53.125	No	Any	70/60	70 if connected with BCM88790 60 if connected in mesh
Two	53.125	Yes	50G RS-FEC	48/39	48 if connected with BCM88790 39 if connected in mesh
Two	50	No	Any	76/67	76 if connected with BCM88790 67 if connected in mesh
Two	50	Yes	50G RS-FEC	54/44	54 if connected with BCM88790 44 if connected in mesh
Two	25.78125	Any	25G RS-FEC	100	—

3.7 Statistics Interface

The statistics interface is an event-driven interface through which statistics are pushed out. Statistics records are continuously reported at a maximal rate of one record per clock in ingress and egress of each core, in other words, a maximum rate of four records per clock. The BCM88690 supports one of the following global configurable options:

- Queue-Size – The statistics interface reports the queue size of ingress enqueue actions and ingress dequeue actions. This mode can be used to build an image of queues size and infer congestion and also enable congestion management by an ingress PP.
- Billing – The statistics interface reports ingress received packets and egress transmitted packets. Packets are tagged with information that maps into counters at the external statistic processing device.
- Ingress-Enqueue/Dequeue – In this mode, the statistics interface reports per each ingress packet enqueued and dequeued. Packets are tagged with information that map into counters at the external statistic processing device.

The statistics interface has three modes:

- Single mode – The statistics interface is a single port up to 400GbE. Each packet contains records from ingress and egress of both cores. This mode allows different record sizes for the ingress and the egress. Thus, it is possible to mix larger ingress records with shorter egress records without compromising the rate of the statistics interface.
- Dual mode – The statistic interface is made of two ports (up to 200GbE each). Each interface caters to the ingress and egress of a single core. This mode also benefits different record sizes for the ingress and the egress.
- Quad mode – The statistics interface is made of four 100GbE interfaces. Each interface caters to the ingress or egress of a single core. In this mode, mixing larger ingress record with shorter egress records would compromise the statistics interface bandwidth.

The external statistics processor can be Broadcom KBP or TAP devices, or a custom FPGA. When connecting to the Broadcom KBP or TAP as an external statistics processor, the statistics interface should be configured to Dual mode.

The statistics interface uses Ethernet ports from the NIF. Any NIF port can be used as a statistics interface, and any NIF port can serve as statistics interface for each of the cores.

- Up to four Ethernet ports are used in quad mode (it is expected that in Quad mode, the ports will be 100GbE).
- Up to two Ethernet ports are used in Dual mode (it is expected that in Dual mode, the ports will be 200GbE).
- A single Ethernet port is used in Single mode (it is expected that in Single mode, the port will be 400GbE).

NOTE:

- A mix of statistics interface ports and NIF Ethernet ports on the same PM, is *not* supported. A mix of statistics interface ports and ELK-over-ILKN is supported.
- To keep the maximum number of lanes for ETH, it is recommended to allocate all ports used for the statistics interface on the same PM50.
- Only the TX direction of the Ethernet port is used for the statistics interface. The RX direction is not used for data (statistics records) transfer, and it can be left unconnected. However, it is recommended to connect the RX direction to enable the use of link-training and allow more debug capabilities over the interface.

An Ethernet-like MAC is used to send statistics packets:

- Standard Ethernet 8-byte preamble.
- 32b FCS, which is the same as standard Ethernet.
- Average IPG of 12B.

NOTE: Consider distributing network ports and network traffic evenly between the two cores when allocating SerDes for network, ELK, and statistics purposes. An even distribution enables better usage of internal resources.

3.8 HBM Packet Buffers

The BCM88690 integrates two HBM Gen2 modules. The HBM technology integration enables low-power and high-performance memory access. The integrated HBM modules are 4-Hi for a total of 8 GB of deep buffering.

3.9 CPU Interface

The Broadcom iProc block provides an interface between the host CPU and the internal registers and tables within the switch device, enabling complete management of the switch.

The iProc block is made up of the following components:

- PCIe x4 lane Gen3 interface at up to 8 Gb/s:
  - Compatible with x1,or x2 lane PCIe.g4.
  - Compatible with PCIe Gen1 at 2.5 Gb/s or Gen2 at 5 Gb/s.
- BSC (I^2C-compatible) 2-line interface.
  - Basic device debug and register access (PCIe only).
  - PCIe QSPI flash programming.
- Microcontroller subsystem:
  - Includes two Arm Cortex-R5 microcontrollers.
  - Runs at 875 MHz (independent of core clock).
  - 32-KB I-Cache, 32-KB D-Cache for each microcontroller core.
  - 128-KB I-tightly coupled memory, 128-KB D-Tightly coupled memory for each microcontroller core.
  - 1-MB internal system memory.
- MIIM interface:
  - MDIO compatible interface.
- LED interface.
- SBUS DMA: Enables the BCM88690 to read from host memory and update the BCM88690 tables, and to read BCM88690 tables and write to the host memory using DMA.
- FIFO DMA.
- Packet TX/RX DMA.
- Remote CPU over network or fabric interface.
- Miscellaneous (endian order, reset controls).

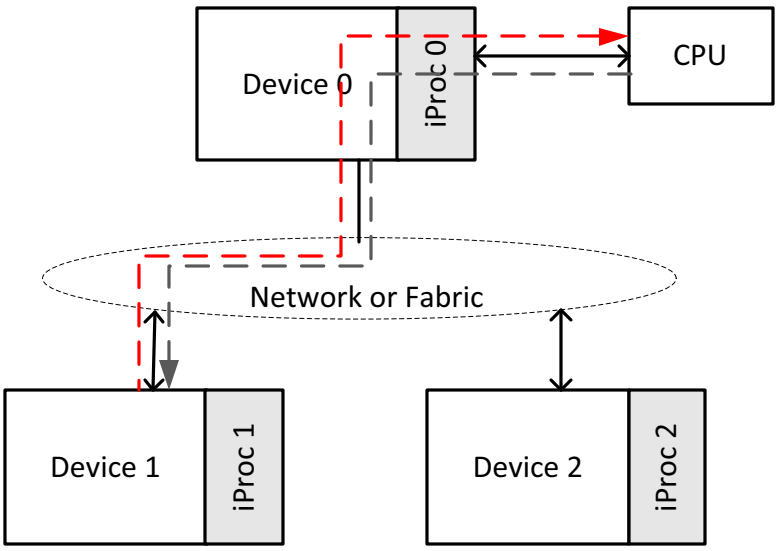
3.9.1 Remote CPU Support

The BCM88690 can be programmed from a remote CPU after initialization. Upon power-up, the device must be initialized using the PCIe interface. After the device has been initialized, the following functions are supported:

- iProc register access
- Generating RCPU packets when interrupts are triggered
- SCHAN register access
- SCHAN table access

The BCM88690 can operate in a system that is managed by a remote CPU. The CMIC communicates with the remote CPU through Ethernet packets with a special EtherType. These packets are referred to as remote CPU packets. Figure 8 represents a system managed by a remote CPU.

Figure 8: System Managed by Remote CPU



For the CPU to generate an S-channel operation in Device 1:

- The CPU generates an Ethernet packet with MACDA addressed to iProc1 with a special EtherType value reserved for remote CPU packets. The packet is an SCHAN_REQUEST.
- iProc0 injects this packet into the ingress pipeline of Device 0. The packet is forwarded based on the MACDA.
- The packet is received at Device 1 and is forwarded to iProc1.
- iProc1 interprets the packet and performs the S-channel operation.
- iProc1 creates a new SCHAN_REPLY packet based on the result of the S-channel operation. This is also an Ethernet packet with MACDA addressed to the CPU with a special EtherType. This packet is injected into the ingress pipeline of Device 1.
- Device 1 forwards the SCHAN_REPLY packet based on the MACDA and the packet is sent to Device 0.
- Device 0 receives the packet and forwards it to iProc0.
- iProc 0 sends the packet to the CPU.

3.9.2 Remote Packet Operations

Remote packets are those that are sent or received by the iProc without a local CPU (whether internal or external) being involved. The iProc receives a remote packet from the switch egress pipe. The iProc matches this packet and performs some operation based on the packet data. The iProc may then send a packet back to the sender of the original packet.

The remote CPU is able to perform certain SCHAN operations without the local CPU's intervention. This is especially useful in stacks where the master CPU in the stack may want to perform L2 insert or delete operations. The means for having the CMIC match incoming packets and perform an SCHAN operation is provided. The CMIC may then send a reply packet back to the requesting remote CPU with the SCHAN operation's status and result data.

Although remote CPUs can send arbitrary SCHAN control packets to the device using this mechanism, it does not remove the requirement for a local CPU to configure the switch (either internal or external). The remote CPU SCHAN packets contain control information to match a reply to a request, but higher layer software must be provided to deal with lost packets, whether they are request or reply packets. Some SCHAN operations are potentially destructive in that they cannot easily be replayed if a reply is lost. There is no mechanism provided in this device to deal with such situations.

3.9.3 PCIe Interface

The PCIe interface of the BCM88690 switch conforms to PCIe 3.1 specifications. The BCM88690 supports four lanes of Gen3 PCIe (8G in each direction). No external glue logic is required to support this interface. The protocols and electrical requirements of the PCIe specifications are strictly implemented.

3.9.4 MIIM

The iProc supports the IEEE 802.3 standard MII Management (MIIM) interface. This is a two-wire serial bus controlled by the iProc that allows register access to external PHYs in the system. The two signals for MIIM are MDC (clock) and MDIO (bidirectional data).

The CPU programs the external PHY registers using this interface. The MIIM interface can be configured to support Clause 22 or Clause 45.

The BCM88690 supports eight MIIM interfaces.

3.9.5 UART

The BCM88690 has two UART interfaces. UART interfaces are used for debugging software running on the microcontrollers (one UART for each microcontroller). The UART interfaces can be used for Time-of-Day (ToD) synchronization.

The UART interface includes only the following two data lines:

- One RxData line
- One TxData line

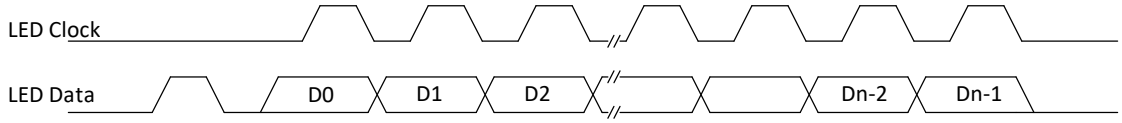
3.9.6 LED Interface

The device provides five serial LED output interfaces. The microcontroller has control of all five interfaces, allowing the user to select which interface(s) are used to provide serial LED bitstreams. For example, a user can write code for the microcontroller that collects status for 96 × 50GbE ports, forms a single stream of status bits, and then shifts this out using any one of the LED interfaces.

The output frequency and refresh rate are user-configurable. These parameters are common across all five of the LED status interface outputs.

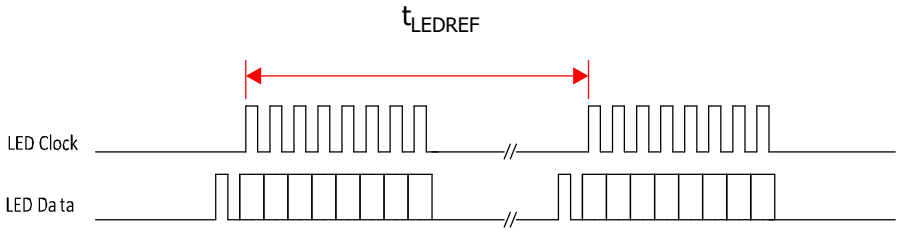
A two-wire (clock and data) LED interface is provided to control system LEDs. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED data bits. The LED data signal is pulsed high at the start of each LED refresh cycle (see Figure 9).

Figure 9: Single LED Refresh Cycle



The LED refresh cycle is repeated periodically to refresh the LEDs (see Figure 10).

Figure 10: LED Refresh Timing

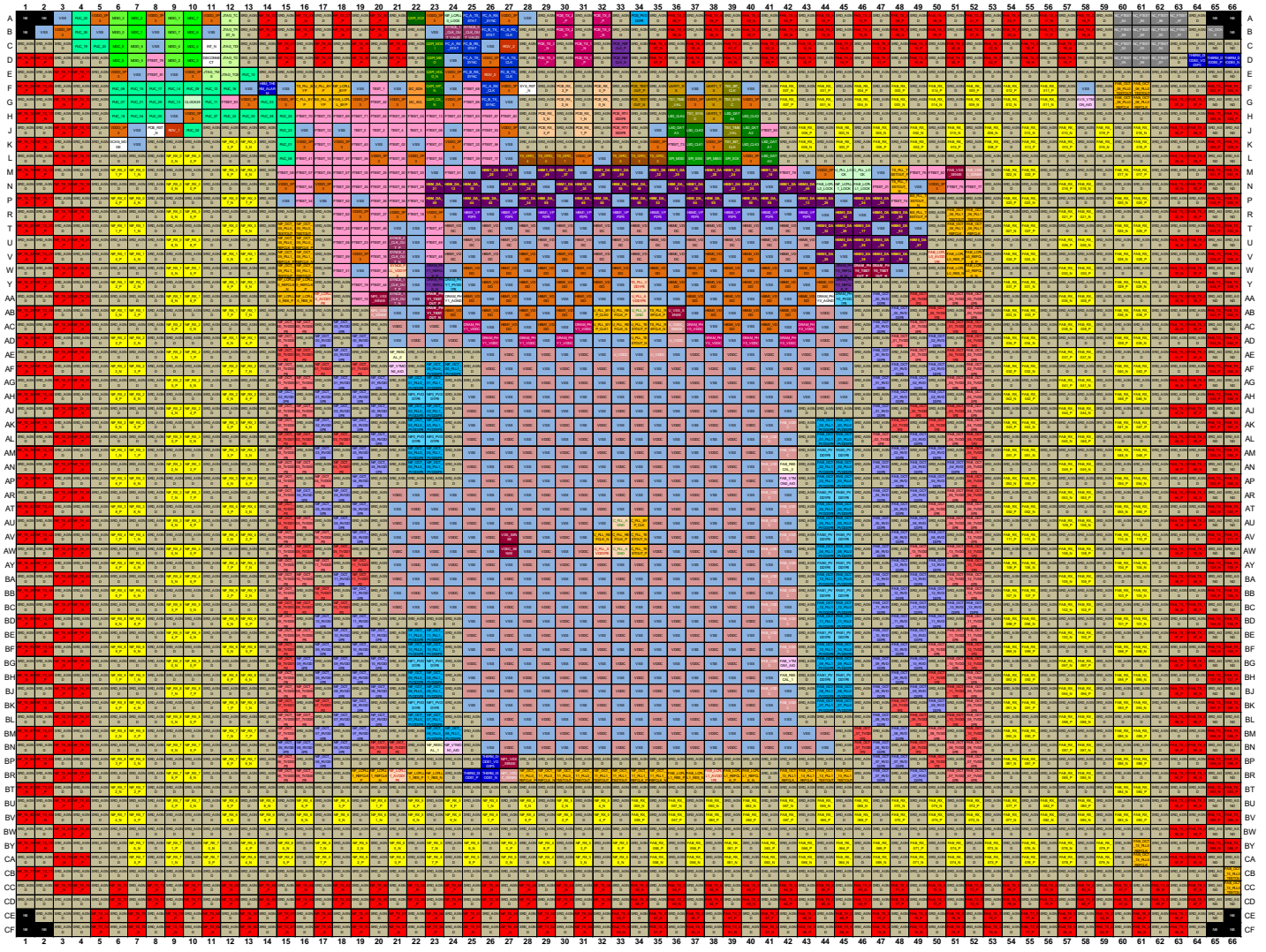


Chapter 4: Pin Signal Description

4.1 Pin Map and Pin List

The BCM88690 pin list and pin map are provided in spreadsheet format on the Broadcom docSAFE collateral distribution site. The spreadsheet serves as the official document containing the device's signal mapping. Refer to the *BCM88690 PinList* file (see Related Documents).

Figure 11: Pin Map



4.2 Pin I/O Type Description

Table 11 lists the conventions that are used to describe the I/O nature of the pins.

Table 11: Signal I/O Type Description

I/O	Description
B	Bidirectional signal
B_{OD}	Open drain bidirectional signal
B_{PD}	Bidirectional signal, with internal pull-down[a]
B_{PU}	Bidirectional signal, with internal pull-up[a]
I	Input signal
I_{PD}	Input signal, with internal pull-down[a]
I_{PU}	Input signal, with internal pull-up[a]
NC	No Connect
O	Output signal
O_{OD}	Open drain output signal
O_{PD}	Output, with internal pull-down[a]
O_{PU}	Output, with internal pull-up[a]

a. Pull-up and pull-down values are minimum = 40 kΩ, maximum = 60 kΩ.

4.3 Pin Description – Grouped by Function

Table 12 provides an overview of the pins on the BCM88690.

NOTE: In the following table, the term HWDG refers to the *Hardware Design Guidelines for StrataDNX 16-nm Devices* application note (DNX16-AN1xx).

Table 12: Pin List by Function

Signal/Bus Name	Qty.	Type	Tech	Description
PCIe Interface				PCIe interface supporting Gen1, Gen2 and Gen3. According to connectivity (x1, x2, x4), use lanes [0], [1:0], or [3:0].
PCIE_TX_[3:0]_P/N	2 × 4	O	Differential	PCIe differential TX pairs. The lanes should be AC coupled. When not in use, leave open.
PCIE_RX_[3:0]_P/N	2 × 4	I	Differential	PCIe differential RX pairs. The lanes should be AC coupled. RX is internally terminated. When not in use, leave open.
PCIE_REFCLK_P/N	2	I	Differential CML	PCIe reference clock inputs. 100 MHz. External 100Ω termination is required between P and N pins. Follow the HWDG [1] for connectivity.
PCIE_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
PCIE_RST_N	1	I_{PD}	CMOS 3.3V	PCIe reset, active low. Follow the functionality described in Section 5.5, Power-Up, Power-Down, and Reset Sequence (This function is required for PCIe Gen1, Gen2, and Gen3.) Use external pull down to force 0 while control logic is not initiated.
PCIE_PVDD0P8	1	PWR	0.8V	PCIe PLL power supply. Follow the HWDG [1] for the recommended filter.
PCIE_RTVDD0P8	2	PWR	0.8V	PCIe SerDes analog power supply. Follow the HWDG [1] for the recommended filter
QSPI				The QSPI interface is used to access a serial flash memory device. The flash memory holds the PCIe SerDes firmware and configuration that is required in all PCIe modes (Gen1, Gen2, and Gen3). Output pins are driven even when the device is in reset.
QSPI_CS_N	1	O_{PD}	CMOS 3.3V	Chip select (active low) from device to flash.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
QSPI_HOLD_N	1	O_{PD}	CMOS 3.3V	Hold (active low) from device to flash. Can be used to pause the serial communication with the master device without resetting the serial sequence.
QSPI_MISO	1	I_{PD}	CMOS 3.3V	Serial data from flash (SO) to device (MI).
QSPI_MOSI	1	O_{PD}	CMOS 3.3V	Serial data from device (MO) to flash (SI).
QSPI_SCK	1	O_{PD}	CMOS 3.3V	Serial clock from device to flash.
QSPI_WP_N	1	O_{PD}	CMOS 3.3V	The write protect (WP_N) allows normal read/write operations when held high. When the WP_N is brought low, all write operations are blocked.
BSC/I^{2}C Interface				The BCM/I^{2}C is an alternate management interface that can be used for PCIe debugging and QSPI image programing.
I2C_SCL	1	I_{OD}	CMOS 3.3V	BSC/I^{2}C CPU interface (responder only). Clock. Open drain. Must be pulled up externally to 3.3V.
I2C_SDA	1	B_{OD}	CMOS 3.3V	BSC/I^{2}C CPU interface (responder only). Data in/out. Open drain. Must be pulled up externally to 3.3V.
Miscellaneous Signals				
INT_N	1	O	CMOS 3.3V	CPU interrupt output. Pseudo open drain, active low. Must be pulled up externally to 3.3V.
SYS_RST_N	1	I_{PD}	CMOS 3.3V	Device reset input. Active low. Use external pull down to force 0 when control logic is not initiated.
DISCONNECT	1	I_{PD}	CMOS 3.3V	Disconnect control input. When 1, the device indicates to fabric link partner to stop sending data to it. This pin can be used for graceful shutdown by external logic that implements early detection of power-down or card removal. Normal operation: 0 Graceful shutdown: 1
MIIM Interface				
MDC_[7:0]	8	O_{PU}	CMOS 3.3V	Clock output of MIIM interface chains. Enables controlling external PHY (master mode only). Supports Clause 22/45 protocol formats with CMOS 3.3V signaling. When not in use, leave open.
MDIO_[7:0]	8	B_{PU}	CMOS 3.3V	Data in/out of MIIM interface chains. Enables controlling external PHY (master mode only). Supports Clause 22/45 protocol formats with CMOS 3.3V signaling. When not in use, leave open.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
Power-Up Configuration Word				
PUC_[29:0]	30	I	CMOS 3.3V	Power-Up Configuration (PUC) word. For PUC bus information see Section 5.5, Power-Up, Power-Down, and Reset Sequence and Section 5.6, Power-Up Configuration Word.
Recommended Operating Voltage				
ROV_[2:0]	3	O	CMOS 3.3V	Recommended operating voltage. Pull to GND, R < 5 kΩ These pins define the required VDDC voltage levels the specific device should work with. Working with a VDDC level that is different from the value required by the ROV may cause the device to fail normal operation or exceed power limits. For ROV information, see Section 5.2.1, Recommended Operating Voltage.
LED Controller				
LED_CLK[4:0]	5	O_{PD}	CMOS 3.3V	LED clocks of the five LED buses. Used to latch the LED output data. When not in use, leave open.
LED_DATA[4:0]	5	O_{PD}	CMOS 3.3V	LED data outputs of the five LED buses. Serially indicates ports status. When not in use, leave open.
UART				
UART[1:0]_RX	2	I_{PD}	CMOS 3.3V	UART data receive, one for each UART interface. Might be used for on-chip Arm debug. Usage options: ■ When using the Broadcom IEEE 1588 stack, both UART[1:0]_RX can be used as input of Time of Day (ToD) for Grand Master (GM) clock. ■ When not in use, leave open.
UART[1:0]_TX	2	O_{PU}	CMOS 3.3V	UART data transmit, one for each UART interface. Might be used for on-chip Arm debug. Usage options: ■ When using Broadcom IEEE 1588 stack, both UART[1:0]_TX can be used as output of Time of Day (ToD) for timeReceiver-clock. ■ When not in use, leave open.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
BroadSync and Broadcom IEEE 1588 Stack Interfaces				
TS_GPIO_[5:0]	6	B_{PU}	CMOS 3.3V	User-programmable general-purpose I/Os. Each pin can be individually configured to act as input or output. Usage options: ■ When not in use, leave open. ■ When using BroadSync, TS_GPIO_1 can be used as 1 PPS for testing. ■ When using Broadcom IEEE 1588 stack, TS_GPIO_[5:0] can be used as 1 PPS input or 1 PPS output.
TS_PLL_BYP	1	I_{PD}	CMOS 3.3V	Factory test only. Pull to GND, R ≤ 1 kΩ.
BS_PLL_BYP	1	I_{PD}	CMOS 3.3V	Factory test only. Pull to GND, R ≤ 1 kΩ.
TS_PLL_REFCLK_P/N	2	I	Differential CML	TSPLL (time stamp PLL) and BSPLL (BroadSync PLL) reference clock differential input. Clock rate is 25 MHz. Follow the HWDG [1] for connectivity. Usage options: ■ When not in use, leave open. ■ When using BroadSync, can be sourced from a simple free-running local oscillator. ■ When using Broadcom IEEE 1588 stack, must be sourced from TDPLL, which is sourced from OCXO.
TS_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
BS_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
TS_PLL_VDD1P8	1	PWR	1.8V	PLL analog power 1.8V. Follow the HWDG [1] for the recommended filter Also supplies the AVS circuit.
TS[1:0]_BIT_CLK	2	B_{PD}	CMOS 3.3V	Usage options: ■ When not in use, leave open. ■ When using BroadSync: – TS0_BIT_CLK is used as BroadSync bit clock, usually 10 MHz. – The signal can be configured as input for BroadSync timeReceiver or output for BroadSync timeTransmitter. – TS1_BIT_CLK is not used. ■ When using Broadcom IEEE 1588 stack, both TS[1:0]_BIT_CLK are optional 10-MHz output.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
TS[1:0]_SYNC	2	B_{PD}	CMOS 3.3V	Usage options: ■ When not in use, leave open. ■ When using BroadSync – TS0_SYNC is used as BroadSync heartbeat pulse, 4 kHz. – Marks the start of the transmission of the synchronize time value. – Can be configured as input for BroadSync timeReceiver or output for BroadSync timeTransmitter. – TS1_SYNC is not used. ■ When using Broadcom IEEE 1588 stack, both TS[1:0]_SYNC are optional 4-kHz input or output.
TS[1:0]_TIME_VAL	2	B_{PD}	CMOS 3.3V	Usage options: ■ When not in use, leave open. ■ When using BroadSync – TS0_TIME_VAL is used as BroadSync synchronized time value. Serially shifts the time value, one bit per rising edge of the TS0_BIT_CLK. – Can be configured as input for BroadSync timeReceiver or output for BroadSync timeTransmitter. – TS1_TIME_VAL is not used. ■ When using Broadcom IEEE 1588 stack, both TS[1:0]_TIME_VAL are not used.
Synchronous Ethernet (SyncE)				
SYNCE_[1:0]_CLK_OUT_P/N	2x2	O	Differential CML	SyncE recovered clock. With an additional external circuit, these signals can be used for system-level clock synchronization for SyncE applications. See Section 3.4.2, Recovered Clock.
SYNCE_[1:0]_CLK_OUT_VALID	2	O	CMOS 3.3V	SyncE valid indication. With an additional external circuit, these signals can be used for system-level clock synchronization for SyncE applications. See Section 3.4.2, Recovered Clock. When using this output, connect an external pull-down.
SYNCE_PLL_VDD1P8	1	PWR	1.8V	PLL analog power 1.8V. Follow the HWDG [1] for the recommended filter.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
Out-of-Band Flow Control				
FC_A_RX_CLK	1	I_{PD}	CMOS 3.3V	Flow-control interface A, RX clock. When not in use, leave open.
FC_A_RX_STAT	1	I_{PD}	CMOS 3.3V	Flow-control interface A, RX status information. Usage options: ■ When operating in ILKN mode, the functionality is xx_STAT. ■ When operating in SPI mode, the functionality is xx_STAT[0]. ■ When not in use, leave open.
FC_A_RX_SYNC	1	I_{PD}	CMOS 3.3V	Flow-control interface A, RX sync signal. Usage options: ■ When operating in ILKN mode, the functionality is xx_SYNC. ■ When operating in SPI mode, the functionality is xx_STAT[1]. ■ When not in use, leave open.
FC_A_TX_CLK	1	O	CMOS 3.3V	Flow-control interface A, TX clock. When not in use, leave open.
FC_A_TX_STAT	1	O	CMOS 3.3V	Flow-control interface A, TX status information. Usage options: ■ When operating in ILKN mode, the functionality is xx_STAT. ■ When operating in SPI mode, the functionality is xx_STAT[0]. ■ When not in use, leave open.
FC_A_TX_SYNC	1	O	CMOS 3.3V	Flow-control interface A, TX sync signal. Usage options: ■ When operating in ILKN mode, the functionality is xx_SYNC. ■ When operating in SPI mode, the functionality is xx_STAT[1]. ■ When not in use, leave open.
FC_B_RX_CLK	1	I_{PD}	CMOS 3.3V	Flow-control interface B, RX clock. When not in use, leave open.
FC_B_RX_STAT	1	I_{PD}	CMOS 3.3V	Flow-control interface B, RX status information. Usage options: ■ When operating in ILKN mode, the functionality is xx_STAT. ■ When operating in SPI mode, the functionality is xx_STAT[0]. ■ When not in use, leave open.
FC_B_RX_SYNC	1	I_{PD}	CMOS 3.3V	Flow-control interface B, RX sync signal. Usage options: ■ When operating in ILKN mode, the functionality is xx_SYNC. ■ When operating in SPI mode, the functionality is xx_STAT[1]. ■ When not in use, leave open.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
FC_B_TX_CLK	1	O	CMOS 3.3V	Flow-control interface B, TX clock. When not in use, leave open.
FC_B_TX_STAT	1	O	CMOS 3.3V	Flow-control interface B, TX status information. Usage options: ■ When operating in ILKN mode, the functionality is xx_STAT. ■ When operating in SPI mode, the functionality is xx_STAT[0]. ■ When not in use, leave open.
FC_B_TX_SYNC	1	O	CMOS 3.3V	Flow-control interface B, TX sync signal. Usage options: ■ When operating in ILKN mode, the functionality is xx_SYNC. ■ When operating in SPI mode, the functionality is xx_STAT[1]. ■ When not in use, leave open.
DRAM PHY				
DRAM_PHY[1:0]_REFCLK_P/N	2 × 2	I	Differential CML	DRAM PHY reference clock inputs. 100 MHz. Follow the HWDG [1] for connectivity.
DRAM_PHY[1:0]_TESTOUT_P/N	2 × 2	O	Differential CML	Factory test only. Leave open.
DRAM_PHY[1:0]_PVDD1P8	2	PWR	1.8V	PLL analog power 1.8V. Follow the HWDG [1] for the recommended filter.
DRAM_PHY[1:0]_VDDC	2 × 5	PWR	0.88V	DRAM PHY core power supply.
DRAM_PHY[1:0]_AGND	2	GND	GND	PLL analog ground. On the board, it should share the same common GND plane as VSS pins.
HBM				
HBM_THERM_ALARM	1	O_{PD}	CMOS 3.3V	An indication that a CATTRIP signal from one of the two HBM dies was asserted. Indicates that the HBM die temperature has reached a certain level where catastrophic damage may occur unless power is reduced. The CATTRIP output is sticky in that to clear a CATTRIP, power-off of the device is required to return the CATTRIP output to 0. When HBM_THERM_ALARM is asserted, the following HBM power supplies should be powered down: ■ HBM[1:0]_VDDC ■ HBM[1:0]_VDDO ■ HBM[1:0]_VPP2P5
HBM[1:0]_VDDC	2 × 13	PWR	1.2V	HBM core supply voltage. On the board, HBM0 and HBM1 supplies can be shared. Follow the HWDG [1] for the recommended filter.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
HBM[1:0]_VDDO	2 × 21	PWR	1.2V	Supply voltage for I/O, for the HBM and the controller DRAM PHY. On the board, HBM0 and HBM1 supplies can be shared. Follow the HWDG [1] for the recommended filter.
HBM[1:0]_VPP2P5	2 × 5	PWR	2.5V	HBM VPP supply. On the board, HBM0 and HBM1 supplies can be shared. Follow the HWDG [1] for the recommended filter.
Direct Access (DA) Test Port				HBM direct access port for vendor-specific test implementations.
HBM_DA_##	18	I/O	Not defined	Multi Drop (MD) DA pins that are connected in parallel to both HBM devices. Factory test only. Leave open.
HBM[1:0]_DA_##	2 × 20	I/O	Not defined	Point-to-point (P2P) DA pins that are connected each to a single HBM DRAM device. HBM0_DA_## pins are connected to HBM0, and HBM1_DA_## pins are connected to HBM1. Factory test only. Leave open.
Calibration Resistors				
FAB_RESCAL_[1:0]	2	Analog	Analog	Resistor calibration terminal for SerDes. Connect each pin through an external resistor of 4.53 kΩ (1%) to SRD_AGND. The resistor should be located between this signal via and the nearest SRD_AGND via. FAB_RESCAL_0: Calibrate SerDes [55:00] and PCIE SerDes. FAB_RESCAL_1: Calibrate SerDes [111:56].
NIF_RESCAL_[1:0]	2	Analog	Analog	Resistor calibration terminal for SerDes. Connect each pin through an external resistor of 4.53 kΩ (1%) to SRD_AGND. The resistor should be located between this signal via and the nearest SRD_AGND via. NIF_RESCAL_0: Calibrate SerDes [47:00]. NIF_RESCAL_1: Calibrate SerDes [95:48].
Thermal Diode				
THERM_DIODE[1:0]_N	2	Analog	Analog	Cathode (N) pin for the thermal diode. One for each diode. Using an external thermal diode reader is strongly recommended. When not in use, connect to GND.
THERM_DIODE[1:0]_P	2	Analog	Analog	Anode (P) pin for the thermal diode. One for each diode. Using an external thermal diode reader is strongly recommended. When not in use, connect to GND.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
THERM_DIODE[1:0]_VDD3P3	2	PWR	3.3V	Thermal diode 3.3V supply. The power of the external thermal diode reader should be connected to a separate source from the source of the device VDDO_3P3 supply. This enables temperature reading when the device power is down. If temp diode is not in use, can be connected to VDDO_3P3.
PLLs and Clocks				
CLOCK25	1	I	CMOS 3.3V	25 MHz clock.
C_PLL_REFCLK_P/N	2	I	Differential CML	Core PLL reference clock inputs. 25 MHz. Follow the HWDG [1] for connectivity.
C_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
C_PLL_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V. Follow the HWDG [1] for the recommended filter.
C_PLL_AGND	2	GND	GND	PLL analog ground. On the board, it should share the same common GND plane as VSS pins.
C_PLL_LOCK	1	O_{PD}	CMOS 3.3V	PLL lock indication. High indicates PLL is locked.
U_PLL_REFCLK_P/N	2	I	Differential CML	Microcontroller PLL reference clock inputs. 25 MHz. Follow the HWDG [1] for connectivity.
U_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
U_PLL_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V. Follow the HWDG [1] for the recommended filter.
U_PLL_AGND	1	GND	GND	PLL analog ground. On the board, it should share the same common GND plane as VSS pins.
U_PLL_LOCK	1	O_{PD}	CMOS 3.3V	PLL lock indication. High indicates PLL is locked.
FAB_LCPLL[1:0]_REFCLK_P/N	2 × 2	I	Differential CML	Fabric LCPLL reference clock inputs. 156.25 MHz. Follow the HWDG [1] for connectivity.
NIF_LCPLL[1:0]_REFCLK_P/N	2 × 2	I	Differential CML	NIF LCPLL reference clock inputs. 156.25 MHz. Follow the HWDG [1] for connectivity.
FAB_LCPLL[1:0]_RES_P/N	2 × 2	O	Differential CML	FAB LCPLL resistor calibration. Connect a 5-kΩ, or 4.99-kΩ (±1%) resistor between P and N pins. Place the resistor as close as possible to the via.
NIF_LCPLL[1:0]_RES_P/N	2 × 2	O	Differential CML	NIF LCPLL resistor calibration Connect a 5-kΩ, or 4.99-kΩ (±1%) resistor between P and N pins. Place the resistor as close as possible to the via.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
FAB_LCPLL[1:0]_AVDD1P8	2	PWR	1.8V	PLL analog power 1.8V. Follow the HWDG [1] for the recommended filter
NIF_LCPLL[1:0]_AVDD1P8	2	PWR	1.8V	PLL analog power 1.8V. Follow the HWDG [1] for the recommended filter
C_PLL_BYP	1	I_{PD}	CMOS 3.3V	Factory test only. Pull to GND, R ≤ 1 kΩ.
U_PLL_BYP	1	I_{PD}	CMOS 3.3V	Factory test only. Pull to GND, R ≤ 1 kΩ.
C_PLL_BYP_CLK	1	I_{PD}	CMOS 0.8V	Factory test only. Leave open.
U_PLL_BYP_CLK[1:0]	2	I_{PD}	CMOS 0.8V	Factory test only. Leave open.
FAB_LCPLL[1:0]_LOCK	2	O_{PD}	CMOS 3.3V	FAB_LCPLL lock indication. High indicates PLL is locked. Lock indication is available only after software initializes and enables the PLL.
NIF_LCPLL[1:0]_LOCK	2	O_{PD}	CMOS 3.3V	NIF_LCPLL lock indication. High indicates PLL is locked. Lock indication is available only after software initializes and enables the PLL.
FAB_LCPLL_BYP	1	I_{PD}	CMOS 3.3V	Factory test only. Pull to GND, R ≤ 1 kΩ.
NIF_LCPLL_BYP	1	I_{PD}	CMOS 3.3V	Factory test only. Pull to GND, R ≤ 1 kΩ.
FAB SerDes Links				
FAB_TX_[111:0]_P/N	2 × 112	O	Differential	Fabric SerDes differential TX pairs. The link should be AC coupled and have a termination on the link-partner receiver. Verify that the link partner includes this circuitry.
FAB_RX_[111:0]_P/N	2 × 112	I	Differential	Fabric SerDes differential RX pairs. The SerDes receiver includes internal serial AC coupling and termination. If external AC coupling is required, see Chapter 5, Electrical Specifications.
NIF SerDes Links				
NIF_TX_[95:0]_P/N	2 × 96	O	Differential	NIF SerDes differential TX pairs. The link should be AC coupled and have a termination on the link-partner receiver. Verify that the link partner includes this circuitry.
NIF_RX_[95:0]_P/N	2 × 96	I	Differential	NIF SerDes differential RX pairs. The SerDes receiver includes internal serial AC coupling and termination. If external AC coupling is required, see Chapter 5, Electrical Specifications.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
Octal SerDes Supply and Tests				
FAB_OCT_##_PLL[1:0]_REFCLK_P/N	4 × 2	I	Differential CML	Factory test only. Leave open.
FAB_OCT_##_PLL[1:0]_TESTOUT_P/N	4 × 2	O	Differential CML	Factory test only. Leave open.
FAB_OCT_[13:0]_PLL[1:0]_PVDD0P8	28	PWR	0.8V	SerDes octet PLL power 0.8V Follow the HWDG [1] for the recommended filter.
FAB_OCT_##_RVDD0P8	4 × 14	PWR	0.8V	SerDes octet receiver power 0.8V. Follow the HWDG [1] for the recommended filter.
FAB_OCT_##_TVDD0P8	3 × 14	PWR	0.8V	SerDes octet transmitter power 0.8V. Follow the HWDG [1] for the recommended filter.
FAB_OCT_##_TVDD1P2	2 × 14	PWR	1.2V	SerDes octet transmitter power 1.2V. Follow the HWDG [1] for the recommended filter.
NIF_OCT_##_PLL[1:0]_REFCLK_P/N	2 × 4	I	Differential CML	Factory test only. Leave open.
NIF_OCT_##_PLL[1:0]_TESTOUT_P/N	2 × 4	O	Differential CML	Factory test only. Leave open.
NIF_OCT_[11:0]_PLL[1:0]_PVDD0P8	24	PWR	0.8V	SerDes octet PLL power 0.8V. Follow the HWDG [1] for the recommended filter.
NIF_OCT_##_RVDD0P8	4 × 12	PWR	0.8V	SerDes octet receiver power 0.8V Follow the HWDG [1] for the recommended filter.
NIF_OCT_##_TVDD0P8	3 × 12	PWR	0.8V	SerDes octet transmitter power 0.8V. Follow the HWDG [1] for the recommended filter.
NIF_OCT_##_TVDD1P2	2 × 12	PWR	1.2V	SerDes octet transmitter power 1.2V. Follow the HWDG [1] for the recommended filter.
FAB[1:0]_PVDD1P8	2 × 7	PWR	1.8V	SerDes octet PLL power 1.8V. FAB0 serves FAB octets 0 to 6. FAB1 serves FAB octets 7 to 13. Follow the HWDG [1] for the recommended filter.
NIF[1:0]_PVDD1P8	2 × 4	PWR	1.8V	SerDes octet PLL power 1.8V NIF0 serves NIF octets 0 to 5. NIF1 serves NIF octets 6 to 11. Follow the HWDG [1] for the recommended filter.
BRCM Internal Test and Debug				
SCAN_MODE	1	I_{PD}	CMOS 3.3V	Factory test only. Pull to GND, R ≤ 1 kΩ.
TEST_[4:0]	5	I_{PD}	CMOS 3.3V	Factory test only. Pull to GND, R ≤ 1 kΩ.
FTEST_[83:0]	84	B	CMOS 3.3V	Factory test only. Required connectivity: ■ FTEST_[14:13] should be connected to GND. ■ FTEST_[22:17] should be connected to GND. ■ Other FTEST pins should be left open.
AVS_VTMON_AIO	1	B	Analog	Factory test only. Pull to GND, R = 0Ω.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
FAB_VTMON[1:0]_AIO	2	B	Analog	Factory test only. Pull to GND, R = 0Ω.
NIF_VTMON[1:0]_AIO	2	B	Analog	Factory test only. Pull to GND, R = 0Ω.
SPI				
SPI_MISO	1	O_{PU}	CMOS 3.3V	Factory test only. Leave open.
SPI_MOSI	1	I_{PU}	CMOS 3.3V	Factory test only. Leave open.
SPI_SCK	1	I_{PU}	CMOS 3.3V	Factory test only. Leave open.
SPI_SSN	1	I_{PU}	CMOS 3.3V	Factory test only. Leave open.
JTAG				
JTAG_TCE	1	I	CMOS 3.3V	JTAG test enable. 0 during normal device operation. 1 to enable JTAG functionality. An option is to connect with JTAG_TRST_N.
JTAG_TCK	1	I	CMOS 3.3V	JTAG, clock input.
JTAG_TDI	1	I	CMOS 3.3V	JTAG, input data.
JTAG_TDO	1	O	CMOS 3.3V	JTAG, output data.
JTAG_TMS	1	I	CMOS 3.3V	JTAG, TMS test mode input.
JTAG_TRST_N	1	I_{PD}	CMOS 3.3V	JTAG TAP controller reset. Pull down to GND. (R ≤ 10 kΩ).
VDDC	262	PWR	VDDC	Core power supply. Must be adjusted according to ROV. Working with a VDDC level different from the value required by the ROV may cause the device to fail normal operation or exceed power limits. **NOTE:** ROV levels might be updated toward final product definitions.
U_VDDC	3	PWR	U_VDDC	Microcontroller core power supply. Connect to VDDC.
FAB_VDDC	19	PWR	BH_VDDC	Blackhawk SerDes core power supply. Connect to VDDC.
VDDO_3P3	38	PWR	3.3V	IO 3.3V power supply.
VSS	461	GND	GND	Connect to ground.
SRD_AGND	1905	GND	GND	Analog ground (return path) for Blackhawk SerDes and PCIe SerDes and their supplies (PVDD, RVDD TVDD). On the board, it should share the same common GND plane as with VSS pins.
VDDC_SENSE	1	O	Analog	Core VDD sense, from the VDDC supply grid. Should be used by the system as a feedback to the voltage supply monitor.

Table 12: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
VSS_SENSE	1	O	Analog	Core VSS sense, from the VSS ground grid. Should be used by the system as a feedback to the voltage supply monitor.
FAB_VDDC_SENSE	1	O	Analog	Test VDDC sense. Leave open.
FAB_VSS_SENSE	1	O	Analog	Test VSS sense. Leave open.
NIF[1:0]_VDDC_SENSE	2	O	Analog	Test VDDC sense. Leave open.
NIF[1:0]_VSS_SENSE	2	O	Analog	Test VSS sense. Leave open.
U_VDDC_SENSE	1	O	Analog	Test VDDC sense. Leave open.
U_VSS_SENSE	1	O	Analog	Test VSS sense. Leave open.
NC_FTEST_[97:84]	14	NC	None	Not connected. Leave open.
NC_OCHK	1	NC	None	Orientation check for Broadcom testing systems. Leave not connected on customer board.

Chapter 5: Electrical Specifications

5.1 Absolute Maximum Ratings

The specifications shown in the following table indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 13: Absolute Maximum Rating

Parameter	Min.	Max.	Unit
VDDO_3P3 supply voltage	–0.25	+3.8	V
Supply voltage 1.8V	–0.25	+2.0	V
DDR and HBM VDDO supply voltage[a]	–0.3	+1.5	V
HBM VDDC supply voltage[a]	–0.3	+1.5	V
DDR PHY VDDC supply voltage (0.88V)	–0.25	+0.92	V
HBM VDDP supply voltage[a]	–0.3	+3.0	V
Supply voltage 1.2V (SerDes TX driver)	–0.25	+1.38	V
Supply voltage 0.8V, digital core	–0.25	+0.92	V
Supply voltage 0.8V, SerDes analog	–0.25	+0.92	V
Storage temperature	–40	+100	°C

a. HBM VDDC, VDDO, and VDDP are from the HBM specification.

5.2 Recommended Operating Conditions

5.2.1 Recommended Operating Voltage

The BCM88690 is equipped with a preprogrammed Recommended Operating Voltage (ROV) stamp indicating the nominal voltage at which the core (VDDC) of the specific BCM88690 device must be operated. The ROV stamp indicates the silicon process of this specific device. Working with a VDDC level that is different from the value required by the ROV may cause the device to fail normal operation or exceed power limits.

Power-up the BCM88690 with the initial state voltage level (according to Table 14) for the VDDC. Next, read the ROV stamp from the ROV[2:0] pins. Then, trim the VDDC power supply to the ROV stamp voltage. Perform VDDC trimming before the BCM88690 is initialized. ROV does not change from power-up to power-up.

NOTE: If more than one device is on the card, make sure each device has its own VDDC power supply. This VDDC power rail cannot be shared with any other supply rail.

Table 14: VDDC Voltage Level According to ROV Stamp

ROV[2:0]	VDDC Voltage Level	Notes
000	0.82	Initial state, detected before device power up
001	0.82	—
010	0.76	—
011	0.78	—
100	0.80	—
101	0.84	—
110	0.86	—
111	0.88	—

5.2.2 Recommended Operating Voltage Range for DC Supplies

The following table shows the operating voltage range of the DC supplies.

Table 15: Supply Voltage Range

Parameter	Symbol	Min. (%)	Typ. (V)	Max. (%)
Core 0.8V ROV digital supply	VDDC	–0.5%	VDDC according to ROV[a]	+0.5%
SerDes 0.8V PLL supply[b]	xxx_OCT_##_PLL#_PVDD0P8	–3%	0.80	+3%
SerDes 0.8V RX supply[b]	xxx_OCT_##_RVDD0P8	–3%	0.80	+3%
SerDes 0.8V TX supply[b]	xxx_OCT_##_TVDD0P8	–3%	0.80	+3%
SerDes 1.2V TX driver supply[b]	xxx_OCT_##_TVDD1P2	–3%	1.20	+3%
PCIe SerDes 0.8V PLL supply	PCIe_PVDD0P8	–3%	0.80	+3%
PCIe SerDes 0.8V RX/TX supply	PCIe_RTVDD0P8	–3%	0.80	+3%
xPLL 1.8V supply[c]	xPLL_xVDD1P8	–3%	1.80	+3%
I/O 3.3V digital supply	VDDO_3P3	–5%	3.30	+5%
DDR PHY VDDO and HBM VDDO supply voltage	HBM[1:0]_VDDO	–3%	1.2	+3%
HBM VDDC supply voltage	HBM[1:0]_VDDC	–3%	1.2	+3%
HBM VPP supply voltage	HBM[1:0]_VPP2P5	–3%	2.5	+3%
DDR_PHY_VDDC (Fixed, not related to ROV VDDC)	DRAM_PHY[1:0]_VDDC	–3%	0.88	+3%

a. Recommended Operating Voltage (ROV).

b. “xxx_” is used for “FAB_” and “NIF_”.

c. xPLL_xVDD1P8 is defined for the following signals:

- C_PLL_AVDD1P8
- U_PLL_AVDD1P8
- FAB_LCPLL[1:0]_AVDD1P8
- NIF_LCPLL[1:0]_AVDD1P8
- FAB[1:0]_PVDD1P8
- NIF[1:0]_PVDD1P8
- TS_PLL_VDD1P8
- SYNCE_PLL_AVDD1P8
- DRAM_PHY[1:0]_PVDD1P8

5.3 Device Power Consumption

NOTE: Under the worst-case process, voltage, and temperature (main die at the 110°C junction temperature and HBM die at the 95°C junction temperature[2]), the power consumption for the defined application (NIF 4.8T, two HBM, no ILKN) is 400W (note that 24W of the 400W is for HBM).

Broadcom does not provide a separate value for thermal power. Use the maximum power as the thermal power.

Table 16 shows the current drawn by the different supply rails.

2. For more information, see Footnote b in Table 48, Absolute Thermal Limit Specifications.

Table 16: Supply Rails and Their Drawn Current

Power Rail	Related Ball	Nominal Voltage (V)	BCM88690 Instances[a]	Max. Current per Instance (mA)	Max. Current from Power Supply (mA)
Device Core Supply	VDDC U_VDDC FAB_VDDC	0.82	1	405,000	405,000
General CMOS IO supply	VDDO_3P3	3.3	1	1000	1000
System PLLs and Analog	C_PLL_AVDD1P8 U_PLL_AVDD1P8 FAB_LCPLL[1:0]_AVDD1P8 NIF_LCPLL[1:0]_AVDD1P8	1.8	6	70	500
	DRAM_PHY[1:0]_PVDD1P8	1.8	2	10	
	SYNCE_PLL_VDD1P8 TS_PLL_VDD1P8 (TS_PLL_VDD1P8 also drives BS_PLL_VDD1P8)	1.8	3	20	
HBM and DRAM PHY					
DRAM_PHY_VDDC	DRAM_PHY[1:0]_VDDC	0.88	2	2000	4000
HBM_VDDO and PHY_VDDO	HBM[1:0]_VDDO[b]	1.2	2	5500	11,000
HBM_VDDC	HBM[1:0]_VDDC[b]	1.2	2	6000	12,000
HBM_VPP	HBM[1:0]_VPP2P5[b]	2.5	2	500	1000
PCIe SerDes rails					
PCIe core PVDD0P8 (PLL)	PCIE_PVDD0P8	0.8	1	32.5	32.5
PCIe lane RVDD0P8 and TVDD0P8	PCIE_RTVDD0P8	0.8	4	38.75	155
BlackHawk SerDes Rails					
BlackHawk Core PVDD1P8	FAB[1:0]_PVDD1P8 NIF[1:0]_PVDD1P8	1.8	26	1	26
BlackHawk Core PVDD0P8	FAB_OCT_[13:0]_PLL[1:0]_PVDD0P8 NIF_OCT_[11:0]_PLL[1:0]_PVDD0P8	0.8	26	282	7332
BlackHawk lane RVDD0P8	FAB_OCT_##_RVDD0P8 NIF_OCT_##_RVDD0P8	0.8	208	250	52,000
BlackHawk lane TVDD0P8	FAB_OCT_##_TVDD0P8 NIF_OCT_##_TVDD0P8	0.8	208	43	8944
BlackHawk lane TVDD1P2	FAB_OCT_##_TVDD1P2 NIF_OCT_##_TVDD1P2	1.2	208	20.5	4264

a. The number of instances represent the number of modules, PLLs, SerDes cores, or SerDes lanes in the BCM88690 device. This number is not related to the number of power pins used for the module, PLL, or SerDes core.

b. The two HBMs use 24W of the total power consumed by HBM[1:0]_VDDO, HBM[1:0]_VDDC, and HBM[1:0]_VPP2P5. The main die uses the rest of the power (because the HBMs share HBM[1:0]_VDDO with the PHYs, which are part of the main die). For more information, see Footnote b in Table 48, Absolute Thermal Limit Specifications.

5.4 Power Supply Filtering

The following table lists the magnitude of supply noise allowed on the different supply rails.

Table 17: Supply Noise Specifications (AC)

Description	Symbol	Condition	Max.	Unit
Core 0.8V digital supply	VDDC	< 0.3 mΩ; 10 kHz to 10 MHz	30	mVpp
SerDes 0.8V PLL supply[a]	xxx_OCT_##_PLL[1:0]_PVDD0P8	100 kHz to 20 MHz	3	mVpp
SerDes 0.8V RX supply[a]	xxx_OCT_##_RVDD0P8	100 kHz to 20 MHz	10	mVpp
SerDes 0.8V TX supply[a]	xxx_OCT_##_TVDD0P8	100 kHz to 20 MHz	10	mVpp
SerDes 1.2V TX driver supply[a]	xxx_OCT_##_TVDD1P2	100 kHz to 20 MHz	10	mVpp
PCIe SerDes 0.8V PLL supply	PCIe_PVDD0P8	100 kHz to 20 MHz	3	mVpp
PCIe SerDes 0.8V supply	PCIe_RTVDD0P8	100 kHz to 20 MHz	10	mVpp
PLL 1.8V supply[b]	xPLL_xVDD1P8	100 kHz to 20 MHz	3	mVpp
3.3V I/O supply	VDDO_3P3	100 kHz to 20 MHz	100	mVpp
DRAM_PHY VDDO and HBM VDDO (@1.2V)	HBM[1:0]_VDDO	100 kHz to 20 MHz	24 (2%)	mVpp
HBM VDDC (@ 1.2V)	HBM[1:0]_VDDC	100 kHz to 20 MHz	24 (2%)	mVpp
HBM VPP (2.5V)	HBM[1:0]_VPP2P5	100 kHz to 20 MHz	25	mVpp
DRAM_PHY VDDC (0.88V)	DRAM_PHY[1:0]_VDDC	100 kHz to 20 MHz	17.5	mVpp

a. “xxx_” is used for “FAB_” and “NIF_”.

b. xPLL_xVDD1P8 is defined for the following signals:

- C_PLL_AVDD1P8
- U_PLL_AVDD1P8
- FAB_LCPLL[1:0]_AVDD1P8
- NIF_LCPLL[1:0]_AVDD1P8
- FAB[1:0]_PVDD1P8
- NIF[1:0]_PVDD1P8
- TS_PLL_VDD1P8
- SYNCE_PLL_AVDD1P8
- DRAM_PHY[1:0]_PVDD1P8

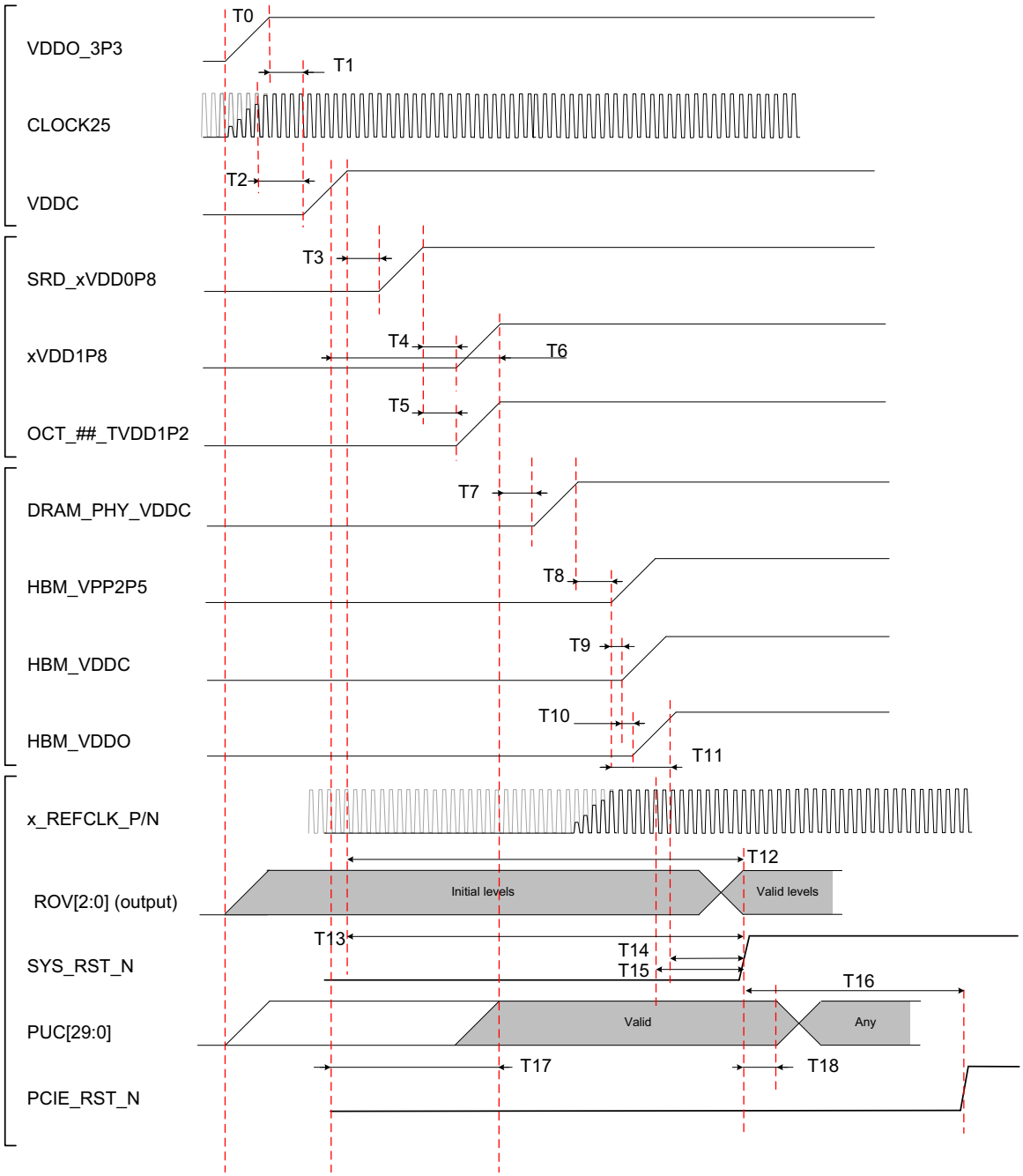
5.5 Power-Up, Power-Down, and Reset Sequence

NOTE: Compliance with the power-up, power-down, and fail-safe requirements is mandatory for proper operation and long-term reliability.

5.5.1 Power-Up Sequence

The following figure illustrates the power-up sequence.

Figure 12: Power-Up Sequence



SRD_xVDD0P8 represents the following rails:

- PCI_PVDD0P8
- PCI_TRVDD0P8
- FAB_OCT_[13:0]_PLL[1:0]_PVDD0P8
- FAB_OCT_[13:0]_RVDD0P8
- FAB_OCT_[13:0]_TVDD0P8
- NIF_OCT_[11:0]_PLL[1:0]_PVDD0P8
- NIF_OCT_[11:0]_RVDD0P8
- NIF_OCT_[11:0]_TVDD0P8

SRD_TVDD1P2 represents following rails:

- FAB_OCT_##_TVDD1P2
- NIF_OCT_##_TVDD1P2

xVDD1P8 represents the following rails:

- TS_PLL_VDD1P8
- SYNCE_PLL_AVDD1P8
- DRAM_PHY[1:0]_PVDD1P8
- C_PLL_AVDD1P8
- U_PLL_AVDD1P8
- FAB_LCPLL[1:0]_AVDD1P8
- NIF_LCPLL[1:0]_AVDD1P8
- FAB[1:0]_PVDD1P8
- NIF[1:0]_PVDD1P8

x_REFCLK_P/N represents the differential reference clocks:

- PCIE_REFCLK_P/N
- TS_PLL_REFCLK_P/N
- DRAM_PHY[1:0]_REFCLK_P/N
- C_PLL_REFCLK_P/N
- U_PLL_REFCLK_P/N
- FAB_LCPLL[1:0]_REFCLK_P/N
- NIF_LCPLL[1:0]_REFCLK_P/N

NOTE: The power-up sequence can be easily met for voltage ramp-ups as slow as 1V/3 ms.

Table 18: Power-Up Sequence Timing

T Number	Description	Min.	Max.	Unit
T0	Initial condition: ■ All voltage rails are below 100 mV ■ SCAN_MODE, TEST[4:0], JTAG_TCE are 0 ■ All non fail-safe are either 0 or below 1.8V (recommended to be set to 0V) ■ SYS_RST_N, PCIE_RST_N are '0'	—	—	—
Vramp	Voltage ramp-up time rate. The rise time rate should be between 50 µs/V and 5 ms/V.	50	5000	µs/V
T1	(VDDO_3P3 > 95%) to (VDDC start)	0	15	ms
T2	(CLOCK25 valid) to (VDDC start)	0		ms
T3	(VDDC > 95%) to (SRD_xVDD0P8 start)	0	3	ms
T4[a, b]	(SRD_xVDD0P8 > 95%) to (xVDD1P8 start)	0	3	ms
T5[a, c]	(SRD_xVDD0P8 > 95%) to (SRD_TVDD1P2 start)	0	3	ms
T6	(VDDC = 0.55V) to (xVDD1P8 > 95%)	—	10	ms
T7	(xVDD1P8 > 95%) to (DRAM_PHY_VDDC start)	0	3	ms
T8	(DRAM_PHY_VDDC > 95%) to (HBM_VPP2P5 start)	0	3	ms
T9[d]	(HBM_VPP2P5 start) to (HBM_VDDC start)	0	2	ms
T10[e]	(HBM_VDDC start) to (HBM_VDDO start)	0	See [e]	ms
T11	(HBM_VPP2P5 start) to (HBM_VDDC, HBM_VDDO > 95%)	0.01	12.5	ms
T12	(VDDC > 95%) to ROV valid	—	60	ms
T13	(VDDC > 95%) to SYS_RST_N deassertion (rising from 0 to 1)	60	—	ms
T14[f]	(Last power to reach 95%) to SYS_RST_N de-assertion (rising from 0 to 1)	10	—	ms
T15	x_REFCLK_P/N valid to SYS_RST_N deassertion	10	—	ms
T16	SYS_RST_N = 1 to PCIE_RST_N deassertion (rising from 0 to 1)	100	—	ms
T17	(VDDC = 0.55V) to PUC valid	—	10	ms
T18	PUC hold time after SYS_RST_N deassertion	160	—	ns

a. Timing between xVDD1P8 and SRD_TVDD1P2 is not required.

b. xVDD1P8 should *not* exceed SRD_xVDD0P8 by more than 1.2V (xVDD1P8 - SRD_xVDD0P8 < 1.2V).

c. SRD_TVDD1P2 should *not* exceed SRD_xVDD0P8 by more than 0.6V (SRD_TVDD1P2 – SRD_xVDD0P8 < 0.6V).

d. The HBM_VPP2P5 supply must be applied before or at the same time as HBM_VDDC and must be equal to or higher than HBM_VDDC at all times.

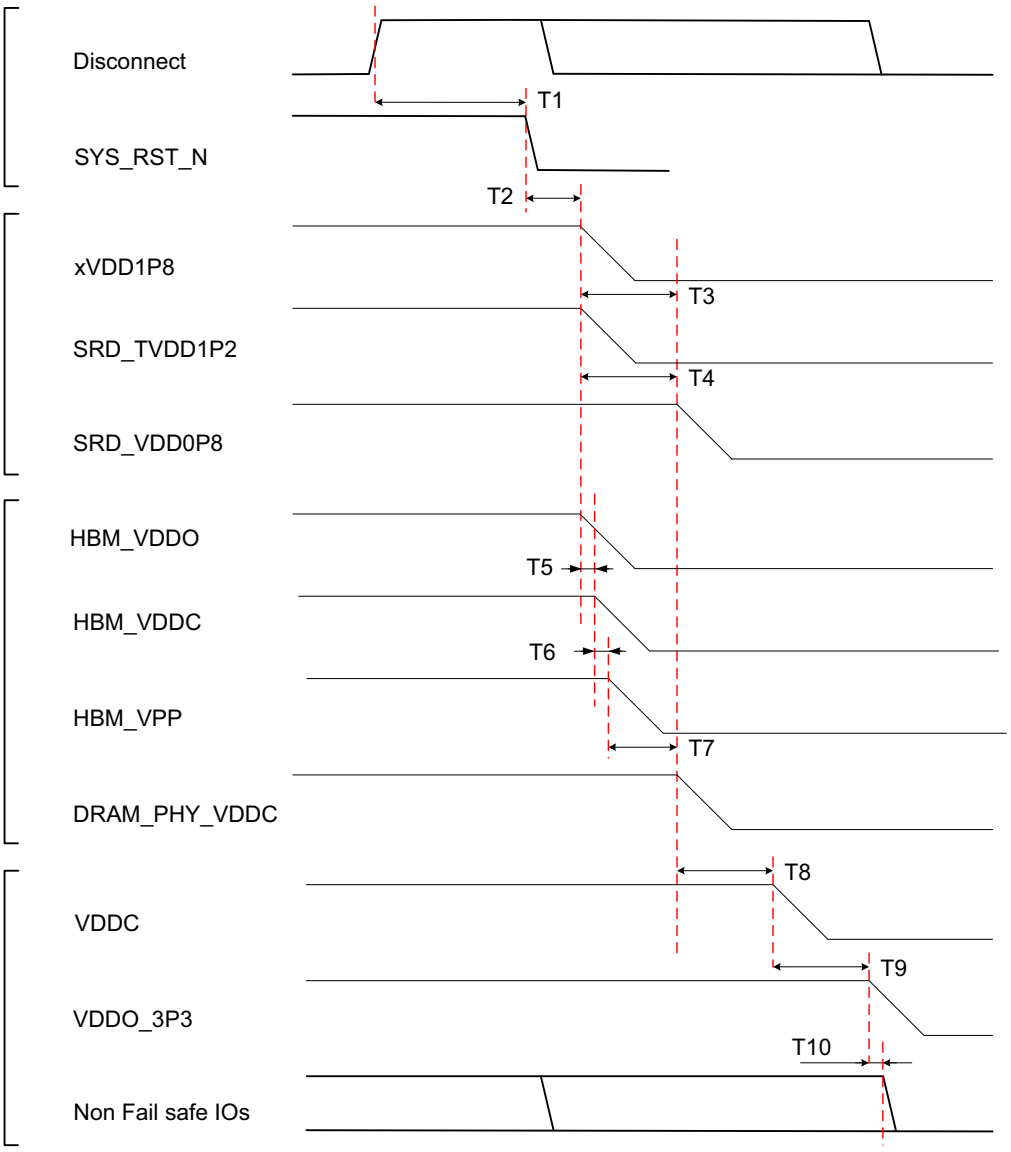
e. The HBM_VDDC supply must be applied before or at the same time as HBM_VDDO. During the power ramp, HBM_VDDC must be equal to or higher than HBM_VDDO, and (HBM_VDDC – HBM_VDDO) must be less than 0.3V.

f. Last power rail out of xVDD1P8, SRD_TVDD1P2, or DRAM_PHY_VDDC.

5.5.2 Power-Down Sequence

The following figure illustrates the power-down sequence.

Figure 13: Power-Down Sequence



SRD_xVDD0P8 represents the following rails:

- PCI_PVDD0P8
- PCI_TRVDD0P8
- FAB_OCT_[13:0]_PLL[1:0]_PVDD0P8
- FAB_OCT_[13:0]_RVDD0P8
- FAB_OCT_[13:0]_TVDD0P8
- NIF_OCT_[11:0]_PLL[1:0]_PVDD0P8
- NIF_OCT_[11:0]_RVDD0P8
- NIF_OCT_[11:0]_TVDD0P8

SRD_TVDD1P2 represents following rails:

- FAB_OCT_##_TVDD1P2
- NIF_OCT_##_TVDD1P2

xVDD1P8 represents the following rails:

- TS_PLL_VDD1P8
- SYNCE_PLL_AVDD1P8
- DRAM_PHY[1:0]_PVDD1P8
- C_PLL_AVDD1P8
- U_PLL_AVDD1P8
- FAB_LCPLL[1:0]_AVDD1P8
- NIF_LCPLL[1:0]_AVDD1P8
- FAB[1:0]_PVDD1P8
- NIF[1:0]_PVDD1P8

Table 19: Power-Down Sequence Timing

T Number	Description	Min.	Max.	Unit
T1	DISCONNECT pin or SW disconnect before reset (for single stage system). This is optional to keep traffic data integrity during reset and graceful shutdown.	15	—	µs
T1	DISCONNECT pin or SW disconnect before reset (for multi stage system). This is optional to keep traffic data integrity during reset and graceful shutdown.	10	—	ms
T2[a, b]	SYS_RST_N asserted to first power-off start. This is optional to minimize the number of packets with errors during reset.	5	—	µs
T3[a, c]	xVDD1P8 drop start to SRD_xVDD0P8 drop start.	0	—	ms
T4[a, d]	SRD_TVDD1P2 drop start to SRD_xVDD0P8 drop start.	0	—	ms
T5	HBM_VDDO drop start to HBM_VDDC drop start	0	—	ms
T6	HBM_VDDC to HBM_VPP drop start. (HBM_VPP2P5 supply must be equal to or higher than HBM_VDDC and HBM_VDDO at all times, including during the entire power-down sequence.)	0	—	ms
T7	HBM_VPP drop start to DRAM_PHY_VDDC drop start.	0	—	ms
T8	SRD_xVDD0P8/DRAM_PHY_VDDC drop start to VDDC drop start.	0	—	—
T9	VDDC drop start to VDDO_P3 drop start.	0	—	ms
T10	VDDO_3P3 drop to non-fail I/O in 0 state.	—	0	ns

a. Timing is not required between xVDD1P8 and SRD_TVDD1P2.

b. Power rails can start the drop without delay, however Footnote c and Footnote d must be met.

c. xVDD1P8 should *not* exceed SRD_xVDD0P8 by more than 1.2V (xVDD1P8 – SRD_xVDD0P8 < 1.2V).

d. SRD_TVDD1P2 should *not* exceed SRD_xVDD0P8 by more than 0.6V (SRD_TVDD1P2 – SRD_xVDD0P8 < 0.6V).

5.5.3 Fail-Safe Considerations

The following I/Os are part of the VDDO_3P3 rail domain but are fail-safe to 1.8V (not fail-safe to 3.3V). The system should **not** force (or pull) any voltage higher than 1.8V on these I/Os when the VDDO_3P3 rail is unpowered.

Table 20: Fail-Safe Considerations by Pin

Pin Name	Suggested Solution
TEST_[4:0]	Should be 5'b0 on customer board.
SCAN_MODE	Should be 0 on customer board (if pull-up is required during debug, connect to the VDDO_3P3 plane of the BCM88690).
JTAG interface: ■ JTAG_TCE ■ JTAG_TDI ■ JTAG_TDO ■ JTAG_TMS ■ JTAG_TCK ■ JTAG_TRST_N	Pull to GND or to the VDDO_3P3 plane of the BCM88690. A JTAG tester should force 0 before the VDDO_3P3 power-up is completed.
PUC_[29:0]	In case of connectivity to pull-up or pull-down resistor: ■ Pull to GND or to the VDDO_3P3 plane of the BCM88690. ■ If driven by logic, force 0 before VDDO_3P3 power-up is completed.
NIF_LCPLL[1:0]_LOCK FAB_LCPLL[1:0]_LOCK	Do not force > 1.8V by sampling logic before power-up is completed.
SYNCE_0_CLK_OUT_VALID SYNCE_1_CLK_OUT_VALID	Do not force > 1.8V by sampling logic before power-up is completed.
OOB FC: ■ FC_A_RX_CLK ■ FC_A_RX_STAT ■ FC_A_RX_SYNC ■ FC_A_TX_CLK ■ FC_A_TX_STAT ■ FC_A_TX_SYNC ■ FC_B_RX_CLK ■ FC_B_RX_STAT ■ FC_B_RX_SYNC ■ FC_B_TX_CLK ■ FC_B_TX_STAT ■ FC_B_TX_SYNC	For inputs: Force 0 before power up is completed. (If not used, leave open) For outputs: Do not force > 1.8V by sampling logic before power-up is completed.
PLL bypass: ■ C_PLL_BYP ■ U_PLL_BYP ■ NIF_LCPLL_BYP ■ FAB_LCPLL_BYP ■ TS_PLL_BYP ■ BS_PLL_BYP	Force 0 before power-up is completed.
FTEST_[83:0]	Follow the definitions in Table 12, Pin List by Function.

The rest of the VDDO_3P3 rail domain I/Os are failsafe to 3.3V, which means that the I/O can be pulled or set to 3.3V even when the VDDO_3P3 rail is unpowered.

5.5.4 Warm Reset

It is possible to reset the device during normal device operation and not just during power-up. To place the device in reset, assert SYS_RST_N and PCIE_RST_N to low. Keep SYS_RST_N low for at least 10 µs before setting it high (releasing the device from the reset condition). The PCIE_RST_N should go high 100 mS after the SYS_RST_N.

When taking the device from the reset condition, all the requirements for logic signals that are part of the Power-Up, Power-Down, and Reset Sequence should be met.

Figure 14: Warm Reset Sequence

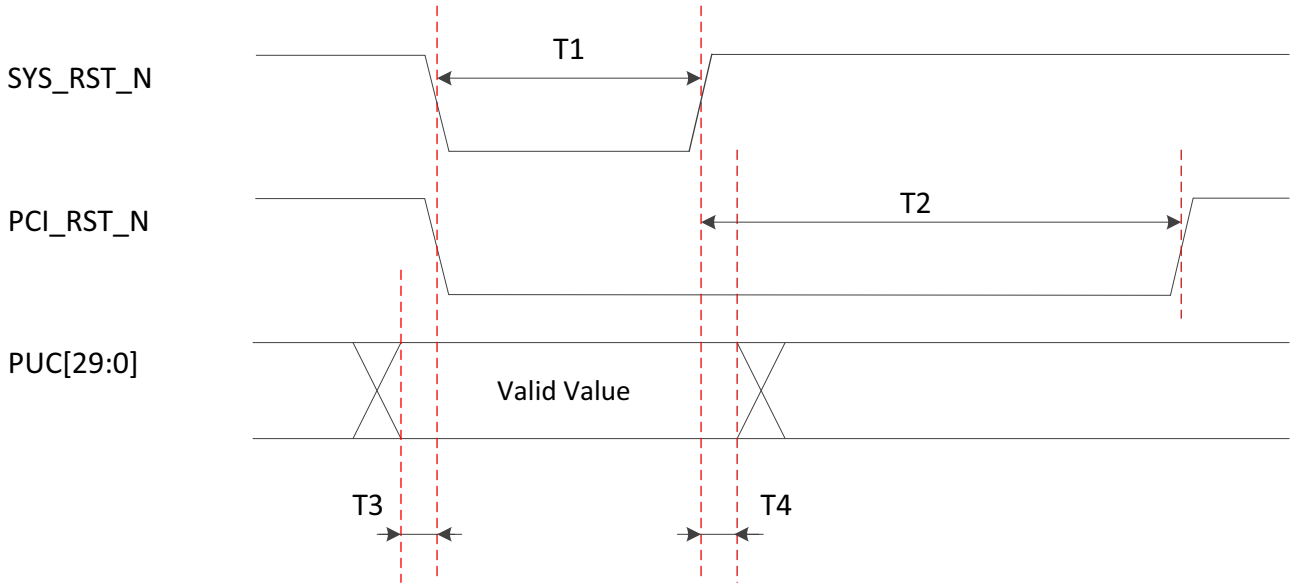


Table 21: Warm Reset Timing

T Number	Description	Min.	Max.	Unit
T1	SYS_RST_N low width	10	—	µs
T2	SYS_RST_N = 1 to PCIE_RST_N deassertion (rising from 0 to 1)	100	—	ms
T3	PUC set-up time to SYS_RST_N assertion	160	—	ns
T4	PUC hold time after SYS_RST_N deassertion	160	—	ns

5.5.5 HBM-Only Power-Down and Power-Up

If it is necessary to power down only the HBM and later power it up, note the following requirements:

- The HBM_VPP2P5 supply must be equal to or higher than HBM_VDDC and HBM_VDDO at all times, including during the entire power-down sequence.
- The HBM_VDDC supply must be applied before or at the same time as HBM_VDDO.
- During the power ramp, HBM_VDDC > HBM_VDDO, and (HBM_VDDC – HBM_VDDO) < 0.3V.

The following figure illustrates these requirements.

Figure 15: HBM-Only Power-Down and Power-Up

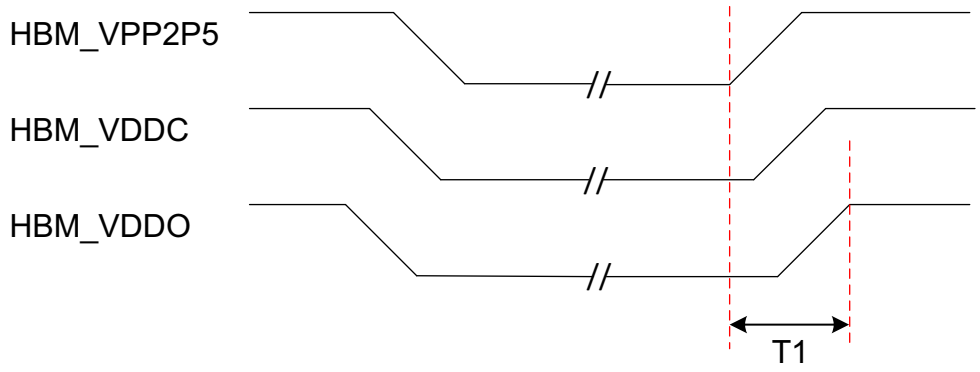


Table 22: T1 Definition

Parameter	Description	Min.	Max.	Unit
T1	(HBM_VPP2P5 start) to (HBM_VDDC, HBM_VDDO > 95%)	0.01	12.5	ms

5.6 Power-Up Configuration Word

The following table describes the power-up configuration word (PUC) functionality for PUC[29:0]. When needed, use pull-up or pull-down resistors where R < 5 kΩ.

PUC inputs are not fail safe, so they should not be driven or pulled-up to 3.3V before the device VDDO_3P3 is up. If pull-up is used, connect to VDDO_3P3. If driven by logic, keep PUC inputs as 0 before the device VDDO_3P3 is up.

Table 23: Power-Up Configuration Signal Description

PUC	Function	Description
PUC_[9:0]	CORE_PLL_N_DIV[9:0]	Set to 240 (PUC[9:0] = 0x0F0).
PUC_[18:10]	CORE_PLL_M_DIV[8:0]	Set to 6 (PUC[19:0] = 0x018F0).
PUC_[19]	Factory test.	Set to 0.
PUC_[21:20]	I2C_SA[1:0]	Device I^2C (BSC) responder address LSB. When the I^2C (BSC) interface is used, the device physical address is made up of the following 7 bits: ■ [A6, A5, A4, A3, A2] fixed as 0x10001. ■ [A1, A0] set according to [PUC_21, PUC_20]. Available addresses are 0x44, 0x45, 0x46, and 0x47.
PUC_[25:22]	Factory test.	Set to 0x0.
PUC_[26]	PCIE_QSPI_ENABLE	Set to 1.
PUC_[29:27]	Factory test.	Set to 0x0

5.7 DC Electrical Specifications

5.7.1 3.3V Digital I/Os

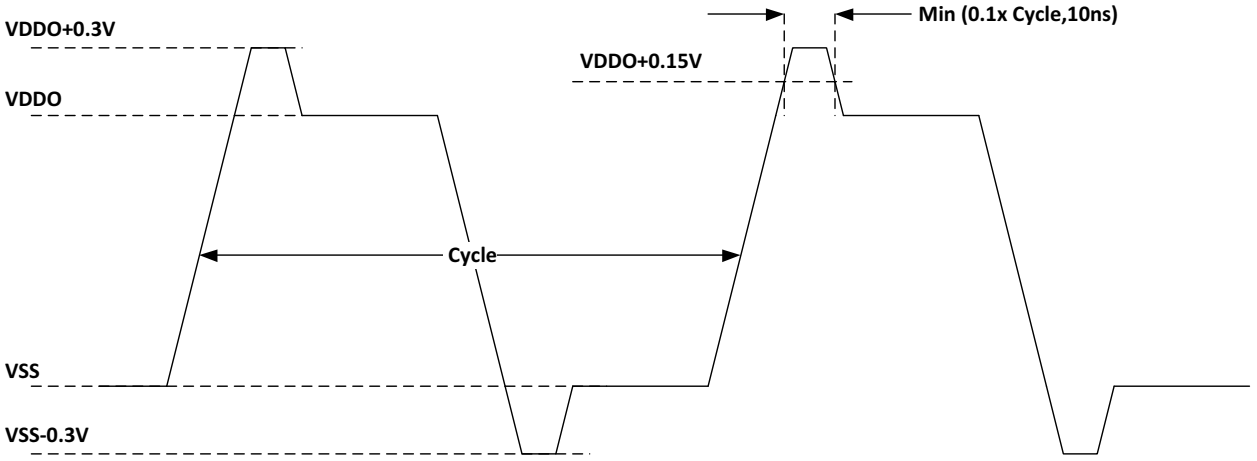
The following table lists the DC specifications of the CMOS3.3V I/Os.

Table 24: DC Specification for CMOS 3.3V I/O

Parameters	Symbol	Conditions	Min.	Max.	Unit
Input low-level voltage	V_{IL}	—	See Figure 16	0.8	V
Input high-level voltage	V_{IH}	—	2.0	See Figure 16	V
Output low-level voltage	V_{OL}	I_{OUT} = 0.4 mA	—	0.4	V
Output high-level voltage	V_{OH}	I_{OUT} = –0.4 mA	VDDO – 0.4	—	V

The following figure shows CMOS 3.3V overshoot definitions.

Figure 16: CMOS 3.3V Overshoot Definitions



The high overshoot can be up to VDDO + 0.3V, and the low overshoot can be down to GND – 0.3V. The duration, measured on a level of half the peak, should be less of 10% of the duty cycle and less than 10 ns.

5.7.2 BSC/I^{2}C

The following table lists the DC specifications of the BSC I/Os.

Table 25: Table 22: DC Specification for CMOS 3.3V BSC/I^{2}C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input low level voltage	V_{IL}	—	—	—	0.3 × VDD	V
Input high level voltage	V_{IH}	—	0.7 × VDD	—	—	V
Output low level current	V_{OL}	V_{OL} = 0.4V	8	—	—	mA

5.8 AC Electrical Specifications

5.8.1 BSC/I^{2}C Interface Timing

The BSC (I^{2}C-compatible) interface supports standard I^{2}C mode and can operate at up to 100 kHz.

The BSC interface of the BCM88690 can operate in responder mode only.

The BCM88690 samples BSC_SDA during a write operation and drives BSC_SDA during a read operation.

Figure 17: BSC Timing Diagram

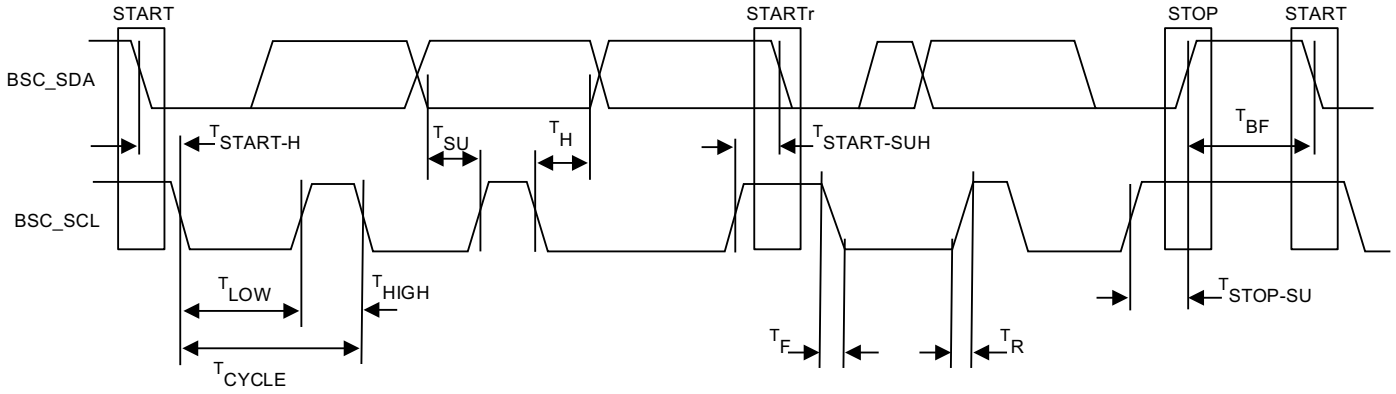


Table 26: BSC Responder Standard-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
BSC_SCL clock frequency	f_{CLK}	—	—	100	kHz
BSC_SCL cycle time	T_{CYCLE}	10	—	—	µs
BSC_SCL low time	T_{LOW}	4.7	—	—	µs
BSC_SCL high time	T_{HIGH}	4.0	—	—	µs
Data hold time	T_H	0.0	—	—	µs
Data setup time	T_{SU}	250	—	—	ns
Rise time, data[a]	T_R	—	—	1000	ns
Fall time, data	T_F	—	—	300	ns
Hold time, start, or repeated start	$T_{START–H}$	4.0	—	—	µs
Setup time, repeated start	$T_{START–SU}$	4.7	—	—	µs
Setup time, stop	$T_{STOP–SU}$	4.0	—	—	µs
Bus free time (between stop and start)	T_{BF}	4.7	—	—	µs

a. BSC_SCL is an open-drain input, and BSC_SDA is an open-drain input/output. The rise time is dependent on the strength of the external pull-up resistor, which must be chosen to meet the rise time requirement.

5.8.2 Management Interface Timing

5.8.2.1 MDIO AC Characteristics

Figure 18: MIIM Interface Timing Diagram

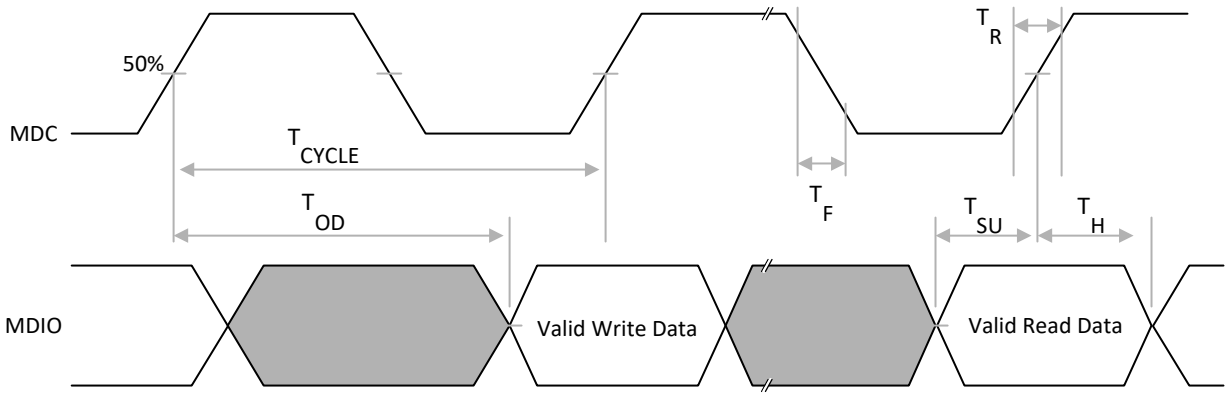


Table 27: 3.3V MDC/MDIO Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
MDC clock frequency	f_{CLK}	—	2.5	12.5	MHz
MDC cycle time	T_{CYCLE}	80	400	—	ns
MDC duty cycle	—	40	—	60	%
MDIO setup time	T_{SU}	20	—	—	ns
MDIO hold time	T_{H}	0	—	—	ns
MDIO output delay	T_{OD}	10	—	35	ns

NOTE:
- Output load conditions = 25 pF.
- External device to conform to IEEE specifications.
- MDC rate and MDIO output delay are configurable.

5.8.3 SyncE Recovered Clocks

The SYNCE_[1:0]_CLK_OUT_P/N recovered clocks are differential CML outputs. The following figure shows the recommended connectivity of these clocks.

Figure 19: SYNCE_[1:0]_CLK_OUT Recommended Connectivity

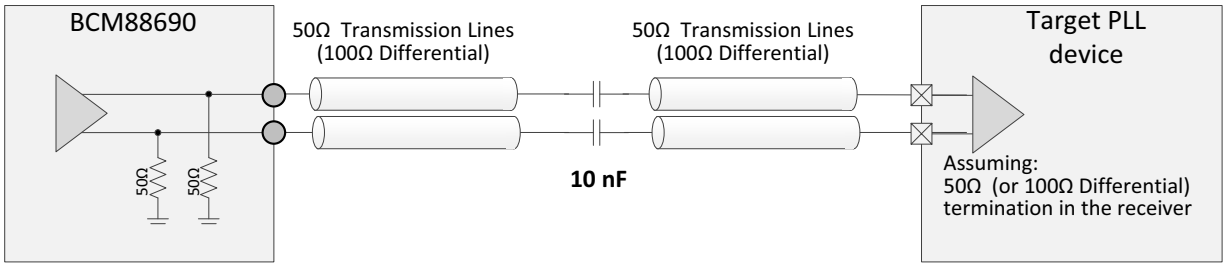


Table 28: SYNCE_[1:0]_CLK_OUT_P/N Output CML Clock Timing

Parameters	Symbol	Min.	Typ.	Max.	Unit
Recovered clock frequency	F_{CLKOUT}	—	25	—	MHz
Output clock swing	$V_{DIFF-PK-PK}$	0.5	0.94	1.2	Vppd

5.8.4 LED Timing

LED[4:0]_CLK and LED[4:0]_DATA are outputs. LED[4:0]_CLK output clock period is 200 ns (5.0 MHz).

Figure 20: LED Timing Diagram

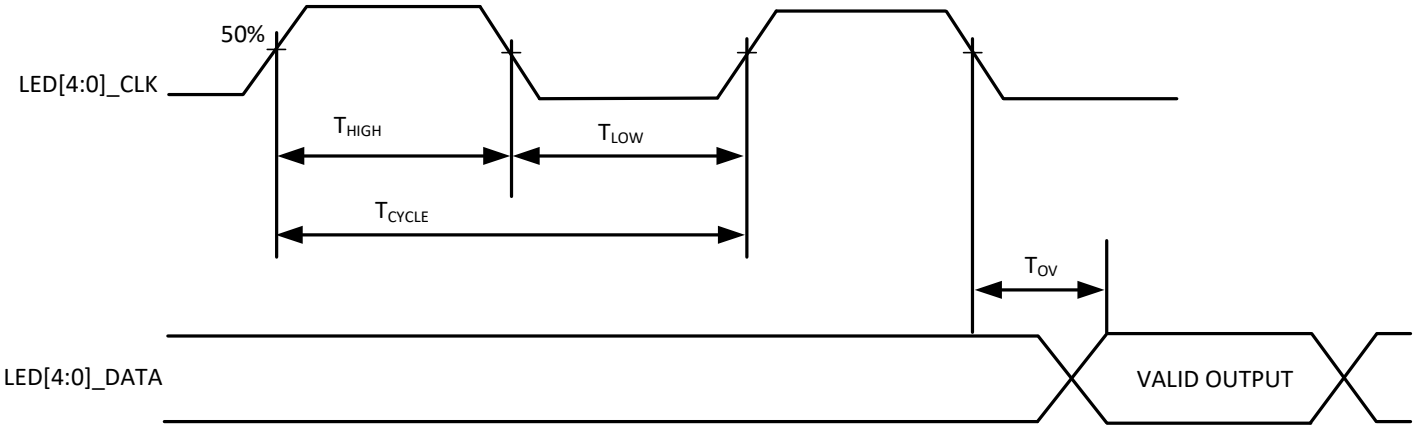


Table 29: LED Timing[a]

Parameter	Symbol	Min.	Typ.	Max.	Unit
LED frequency	F_{TCK}	—	5	5	MHz
LED period	T_{CYCLE}	200	—	—	ns
LED clock HIGH	T_{HIGH}	70	100	130	ns
LED clock LOW	T_{LOW}	70	100	130	ns
LED data output valid	T_{OV}	–15	—	15	ns

a. Timing figures are specified at the 50% crossing thresholds.

5.8.5 Out-of-Band Flow-Control Timing

The out-of-band flow-control (OOBFC) interfaces support two modes of operation, which impact both the protocol and the low level timing.

5.8.5.1 SPI4.2 Flow-Control Mode

Figure 21: OOB Flow-Control Timing in SPI4.2 Mode

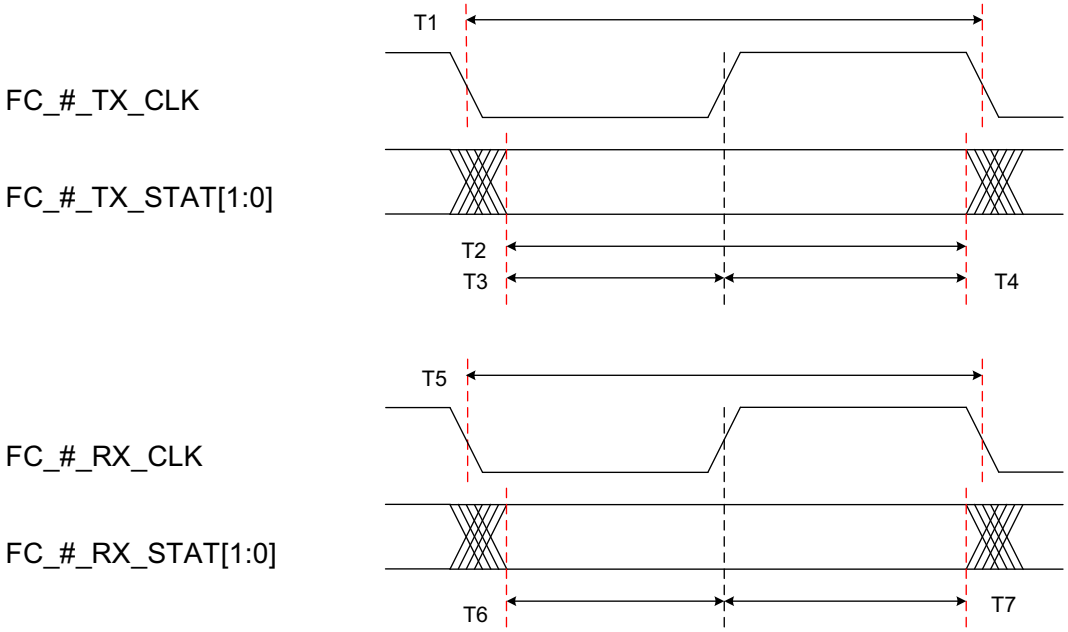


Table 30: OOB Flow-Control Timing Specifications in SPI4.2 Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
FC_#_T_CLK, OOB output clock frequency[a]	1/T1	62.5	FCORE / n	166.66	MHz
FC_#_T_CLK, OOB output clock duty cycle	—	45	—	55	%
FC_#_T_STAT[1:0] output stable window size[b]	T2	5	T1 – 1	15	ns
FC_#_T_STAT[1:0] output stable before clock[c]	T3	—	Programmable	—	ns
FC_#_T_STAT[1:0] output stable after clock[c]	T4	—	Programmable	—	ns
FC_#_R_CLK, OOB input clock frequency	1/T5	—	—	200	MHz
FC_#_R_CLK, OOB input clock duty cycle	—	40	—	60	%
FC_#_R_STAT[1:0] input setup time[d]	T6	0.5	—	—	ns
FC_#_R_STAT[1:0] input hold time[d]	T7	0.5	—	—	ns

a. FC_#_T_CLK output interface clock frequency is user-programmable. Supported rates are core clock divided by 2*n* (where *n* is 3 to 8). For a 1G core clock, this equals 166.66, 125, 100, 83.33, 71.43, or 62.5 MHz.

b. The given value is for FC_#_T_CLK at F(core / 6). For F(core / 8), add 2ns. For F(core / 16), add 10 ns.

c. The phase of FC_#_T_CLK in relation to FC_#_T_STAT[1:0] is programmable.

d. The sampling clock edge of the input FC_#_R_STAT[1:0] with respect to the input clock can be programmed to either the rising or falling edge. Figure 21 illustrates a rising edge configuration.

5.8.5.2 Interlaken Flow-Control Mode

Figure 22: OOB Flow-Control Timing in Interlaken Mode

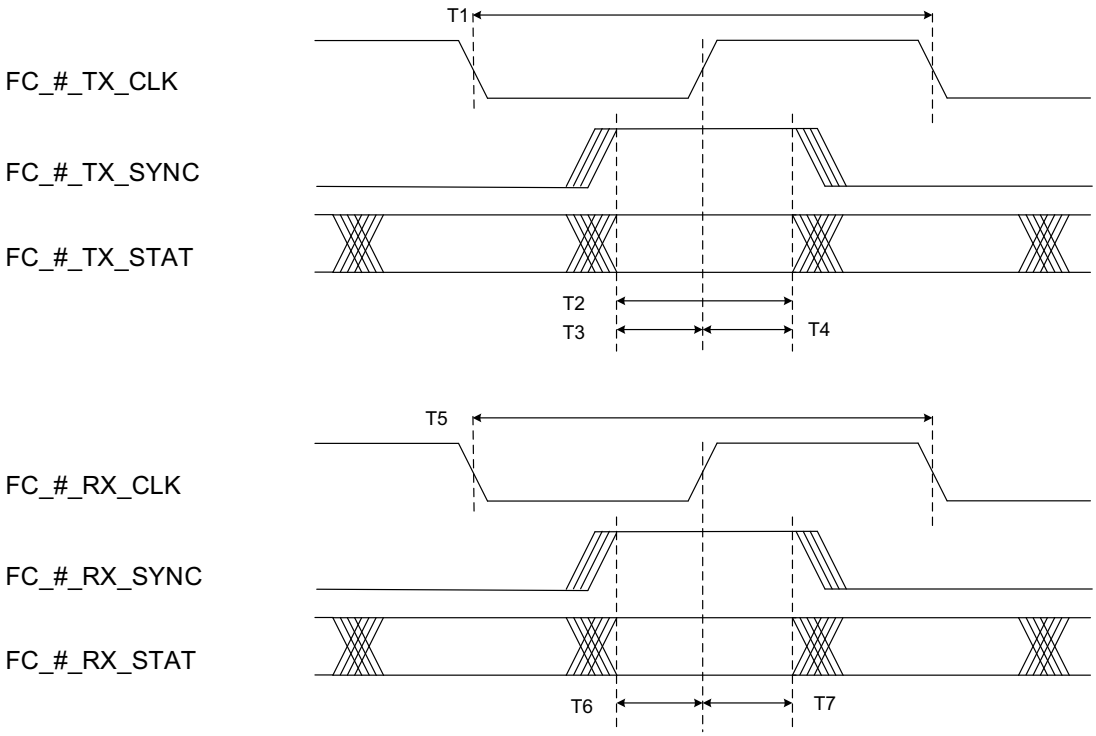


Table 31: OOB Flow-Control Timing Specifications in Interlaken Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
FC_#_T_CLK, OOB output clock frequency[a]	1/T1	62.5	FCORE / n	166.66	MHz
FC_#_T_CLK, OOB output clock duty cycle	—	45	—	55	%
FC_#_T_STAT and FC_#_T_SYNC output stable window size[b]	T2	2	0.5 × T1 – 1	7	ns
FC_#_T_STAT and FC_#_T_SYNC output stable before clock[c]	T3	—	Programmable	—	ns
FC_#_T_STAT and FC_#_T_SYNC output stable after clock[c]	T4	—	Programmable	—	ns
FC_#_R_CLK, OOB input clock frequency	1/T5	—	—	180	MHz
FC_#_R_CLK, OOB input clock duty cycle	—	45	—	55	%
FC_#_R_STAT and FC_#_R_SYNC input setup time[d]	T6	0.5	—	—	ns
FC_#_R_STAT and FC_#_R_SYNC input hold time[d]	T7	0.5	—	—	ns

a. FC_#_T_CLK output interface clock frequency is user-programmable. Supported rates are core clock divided by 6, 8, or 10. For a 1G core clock, this equals 166.66, 125, 100, 83.33, 71.43, or 62.5 MHz.

b. ILKN FC mode is DDR. The value is for FC_#_T_CLK at F(core / 6). For F(core / 8), add 1ns. For F(core / 16), add 5 ns.

c. The phase of FC_#_T_CLK in relation to FC_#_T_STAT and FC_#_T_SYNC is programmable.

d. In ILKN mode, FC_#_R_STAT and FC_#_R_SYNC are sampled on both the rising and the falling edges of RX_CLK. Figure 22 illustrates the parameters relative to the rising edge.

5.8.6 BroadSync and Time Sync Timing

Figure 23 and Table 32 show the timeReceiver mode input timing.

Figure 23: BroadSync Input Timing – timeReceiver Mode

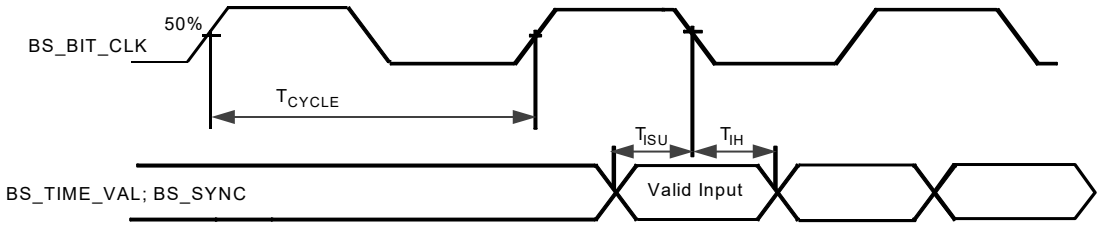


Table 32: BroadSync Input Timing – timeReceiver Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	—	100	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	ns
BS_TIME_VAL; BS_SYNC input setup time	t_{ISU}	20	—	—	ns
BS_TIME_VAL; BS_SYNC input hold time	t_{IH}	0	—	—	ns

Figure 24 and Table 33 show the timeTransmitter mode input timing.

Figure 24: BroadSync Output Timing – timeTransmitter Mode

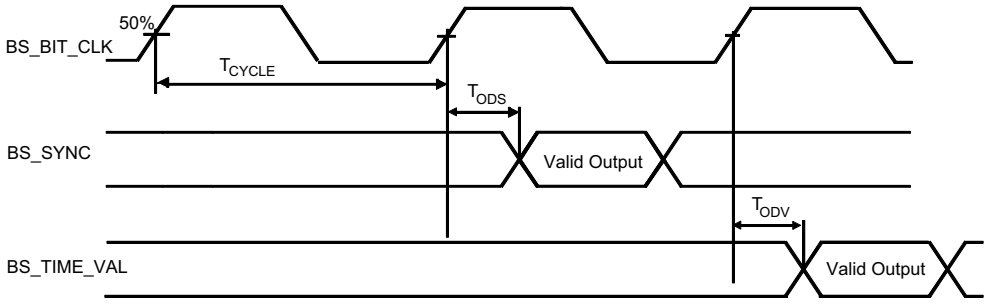


Table 33: BroadSync Output Timing – timeTransmitter Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	—	100	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	ns
BS_SYNC output delay	t_{ODS}	0	—	25	ns
BS_TIME_VAL output delay	t_{ODV}	0	—	25	ns

5.8.7 PCIe Interface

The PCIe core of the BCM88690 supports PCIe Gen1 (2.5G), Gen2 (5G), and Gen3 (8G). The following sections provide basic electrical specifications.

5.8.7.1 PCIe Receiver

The following table lists the specifications of the PCIe SerDes receiver.

Table 34: PCIe SerDes RX Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input differential swing[a]	$V_{IN-DIFF}$	85	—	1200	mVppd
Input differential termination	R_{TERM}	80	100	120	Ω

a. The receiver input should be externally AC coupled.

5.8.7.2 PCIe Transmitter

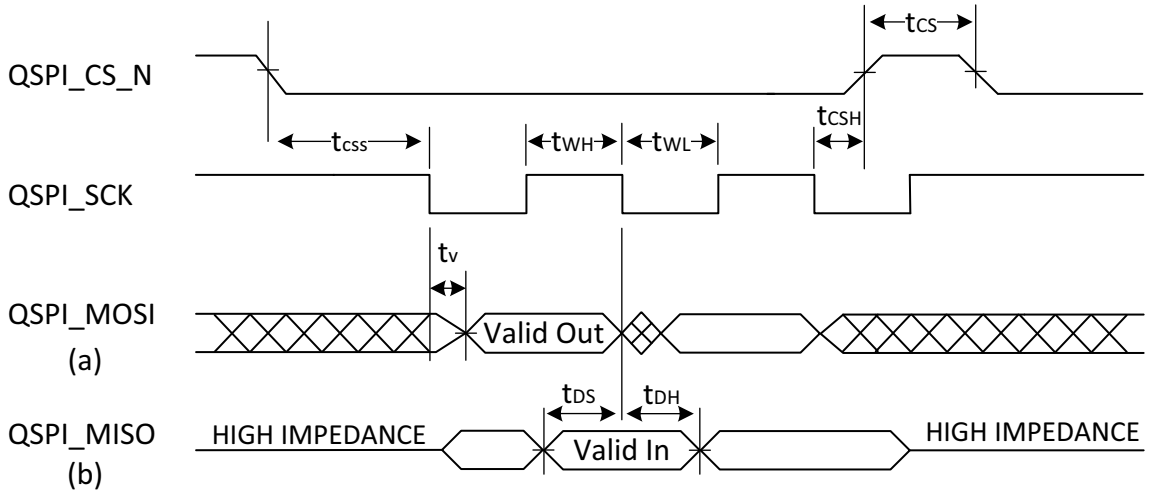
The following table lists the specifications of the PCIe SerDes transmitter.

Table 35: PCIe SerDes TX Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output differential termination	R_{TERM}	80	100	120	Ω
Output differential swing	$V_{OUT-DIFF}$	400	—	1200	mVppd
Output common mode	V_{OUT-CM}	—	400	—	mV

5.8.8 QSPI Flash Interface

Figure 25: QSPI Timing (Boot Read Mode Using BSPI Controller)



(a): Also valid for QSPI_MISO in dual/quad mode; also valid for QSPI_WP_N, QSPI_HOLD_N in quad mode.
(b): Also valid for QSPI_MOSI in dual/quad mode; also valid for QSPI_WP_N, QSPI_HOLD_N in quad mode.

Table 36: QSPI Timing (Boot Read Mode Using BSPI Controller)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	31.25[a]	—	MHz
SCK clock LOW period	t_{WL}	$0.5/F_{SCK} – 0.5$	—	—	ns
SCK clock HIGH period	t_{WH}	$0.5/F_{SCK} – 0.5$	—	—	ns
CS lead time	t_{CSS}	$1/F_{SCK} – 2.9$	—	—	ns
CS trail time	t_{CSH}	–1.6	—	—	ns
MOSI output valid	t_V	–1.6	—	3	ns
MISO input setup	t_{DS}	4	—	—	ns
MISO input hold	t_{DH}	1.3	—	—	ns

a. The QSPI controller issues only FAST_READ commands, as opposed to READ (03h) commands. Therefore, the QSPI device's operating frequency should be based on the Fast Read commands rather than Read (03h) commands.

5.9 Reference Clocks

5.9.1 CLOCK25 Reference Clock

The CLOCK25 is a CMOS 3.3V input. This is a free running clock (without an internal PLL) that is used for SYS_RST_N propagation and other basic operation. The required parameters are specified in the following table.

Table 37: CLOCK25 Specifications

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	—	25	—	MHz
Reference clock accuracy	ACC_{REF}	—	–100	—	+100	PPM
Reference duty cycle	F_{DC}	—	40	—	60	%
Rise/fall time	T_R/T_F	20% to 80%	—	—	4.0	ns
Input jitter cycle-to-cycle, peak-to-peak, 10K samples	J_{IN}	—	—	—	100	ps

5.9.2 Core and Microcontroller PLL Reference Clocks

The BCM88690, holds two PLLs that are used to drive the internal data path and logic. These PLLs are the core clock PLL (C_PLL) and the microcontroller clock PLL (U_PLL). The C_PLL_REFCLK_P/N and U_PLL_REFCLK_P/N, respectively, drive these PLLs.

The following table lists the specifications of the core PLL (C_PLL) and the micro controller PLL (U_PLL) reference clocks.

Table 38: C_PLL and U_PLL Reference Clock Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	25	—	MHz
Reference clock accuracy, total stability	ACC_{REF}	–32	—	+32	PPM
Duty cycle	F_{DC}	45	50	55	%
CML Input reference clock swing (differential)[a]	—	500	—	2000	mVppd
Input CML differential termination	—	80	100	120	Ω
Input CML clock slew. Based on rise/fall time (10-90%)	T_R/T_F	—	—	0.8[b]	ns/Vppd
Input jitter (12 kHz to 5 MHz, RMS)	J_{IN}	—	—	0.35	ps

a. Input should have external AC coupling. The device has an internal 100Ω differential termination.

b. There is a 0.4-ns rise/fall time for a 500-mV swing and 1.6-ns rise/fall time for a 2000-mV swing.

5.9.3 PCIe PLL Reference Clock

The following table lists the specifications of the PCIe PLL reference clock.

Table 39: PCIe PLL Reference Clock Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	100	—	MHz
Reference clock accuracy	ACC_{REF}	–300	—	+300	PPM
Reference duty cycle	F_{DC}	40	—	60	%
Input differential swing[a]	$V_{IN-DIFF}$	600	—	1200	mVppd
Rise/fall time (20% to 80%)	T_R/T_F	200	—	900	ps
Reference clock jitter (RMS, up to 100 MHz)	—	—	—	Follow PCIe specifications	ps

a. The input should be AC coupled and have 100Ω termination between P and N.

5.9.4 SerDes LCPLL Reference Clock

In the BCM88690 device, four PLLs drive the clocks to the SerDes Blackhawk octets. The mapping of the LCPLL to octets and SerDes is described in Section 5.10.1.3, Octet Groups and LCPLL.

The LCPLL reference clocks are named as FAB_LCPLL[1:0]_REFCLK_P/N and NIF_LCPLL[1:0]_P/N.

The following table lists the specifications of the SerDes LCPLL reference clock.

Table 40: SerDes LCPLL Reference Clock Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	156.25	—	MHz
Reference clock accuracy, total stability	ACC_{REF}	–50	—	+50	PPM
Duty cycle	F_{DC}	40	50	60	%
CML input reference clock swing (differential)[a]	—	500	—	2000	mVppd
Input CML differential termination	—	80	100	120	Ω
Input CML clock slew. Based on rise/fall time (10% to 90%)	T_R/T_F	—	—	0.4[b]	ns/Vppd
Input jitter (12 kHz to 20 MHz, RMS)	J_{IN}	—	—	0.15	ps

a. Input should have external AC coupling. The device has an internal 100Ω differential termination.

b. 0.2-ns rise/fall time for a 500-mV swing; 0.8-ns rise/fall time for a 2000-mV swing.

5.9.5 TS_PLL Reference Clock

Table 41: TS_PLL Reference Clock Definitions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	25	—	MHz
Reference clock accuracy	ACC_{REF}	–25	—	+25	PPM
Reference clock duty cycle	F_{REF_DC}	40	—	60	%
CML input reference clock swing[a]	$V_{DIFF-PK-PK}$	0.5	—	1.8	Vppd
Input reference clock rise time/fall time (10% to 90%)	T_R/T_F	—	—	1	ns/Vppd
Input jitter (12 kHz to 20 MHz, RMS)	J_{IN}	—	—	10	ps

a. Input should have external AC coupling.

NOTE: For some IEEE 1588 applications, OCXO is required. For more information, contact Broadcom support.

5.9.6 DRAM PHY PLL Reference Clock

Table 42: DRAM_PHY PLL Reference Clock Definitions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	100	—	MHz
Reference clock accuracy	ACC_{REF}	–100	—	+100	PPM
Reference clock duty cycle	F_{REF_DC}	40	—	60	%
CML input reference clock swing[a]	$V_{DIFF-PK-PK}$	0.5	—	1.8	Vppd
Input reference clock rise time/fall time (10% to 90%)	T_R/T_F	—	—	1	ns/Vppd
Input reference clock jitter (RMS, integration range 12 kHz to 20 MHz)	J_{IN}	—	—	1	ps

a. AMPLITUDE is pk-pk differential (clk_out_p to clk_out_n). The reference clock should be externally AC coupled.

5.10 Blackhawk SerDes Operating Conditions

The following table lists the Blackhawk SerDes operating conditions.

Table 43: Blackhawk SerDes Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Data rate, fabric	F_{b_Fabric}	23	—	53.125	Gb/s
Data rate, NIF Ethernet	F_{b_NIF}	10.3125	—	53.125	Gb/s
Data rate, ELK-over-ILKN	F_{b_ELK}	25.78125	—	53.125	Gb/s
VCO	F_{VCO}	15	—	30	GHz

The Blackhawk SerDes high-speed lanes are organized in cores. Each core, named Blackhawk, includes eight SerDes. Each one of the eight SerDes is an independent lane suitable for optical and backplane applications, operating in either PAM4 or NRZ line coding.

Every group of Blackhawk cores receives its reference clock from the LCPLL as described in Section 5.10.1.3, Octet Groups and LCPLL.

5.10.1 Blackhawk SerDes Features

The following sections describe the main features of the Blackhawk SerDes.

5.10.1.1 General Features

Blackhawk supports the following general features:

- Block of eight SerDes supporting eight serial links.
- Supports line rates (depending on the application) from 10.3125 Gb/s to 53.125 Gb/s per serial link (PAM4 53.125 Gb/s/NRZ 25.78125 Gb/s).
- Each Blackhawk includes two independent PLLs.
- Integrated ARM micro subsystem: monitors the signal and adaptively adjusts the gain, peaking-filter, and DFE coefficients to optimally equalize and restore the signal. During Clause 72 and Clause 93 TX/RX link training, this microcontroller is also responsible for returning feedback to the far link partner to optimally tune its transmitter.

5.10.1.2 Debug Features

Blackhawk supports the following debugging features:

- PRBS 7, 9, 10, 11, 13 15, 20, 23, 31, 49, 58 generator and checker with burst error length measurement.
- Digital loopback: turns around the transmit data before it goes into the analog front-end (this is a digital data path loopback for the data coming from the PCS/MAC transmit side).
- Supports AC-JTAG for both TX and RX.
- Full range horizontal and vertical eye diagnostics.

5.10.1.3 Octet Groups and LCPLL

The SerDes lanes on the NIF side and on the fabric side are organized into octets, sharing two internal independent PLLs that can be configured completely independently. Each transmitter and receiver for each lane can select between the two VCO clocks. In this document, the two PLLs inside an octet are referred to as BHPLL0 and BHPLL1.

The SerDes octets are organized into two NIF SerDes groups and two fabric SerDes groups. Each group has its own dedicated LCPLL that gets an external reference clock and generates an internal clock that is spread among the octets and is used by the two PLLs within each Blackhawk core to generate the desired data rate according to a user-programmable multiplier.

Table 44: Link and Blackhawk Numbering

Interface	LCPLL	Blackhawk	Links	Number of Links
NIF	NIF_LCPLL0	PM50-0 to PM50-5	NIF SRD: 0 to 47	48
NIF	NIF_LCPLL1	PM50-6 to PM50-11	NIF SRD: 48 to 95	48
Fabric	FAB_LCPLL0	FAB BH 0 to 6	FAB SRD: 0 to 55	56
Fabric	FAB_LCPLL1	FAB BH 7 to 13	FAB SRD: 56 to 111	56

5.10.2 Blackhawk SerDes Supported Rates

The following table shows the rates that the fabric SerDes supports.

Table 45: Fabric SerDes Supported Rates

VCO Rate (GHz)	PAM4 Rate (Gb/s)	NRZ OSx1 Rate (Gb/s)	NRZ OSx2 Rate (Gb/s)
20.625	—	20.625	—
23	—	23	—
25	50	25	—
25.78125	—	25.78125	—
26.5625	53.125	—	—

For the rates that the NIF supports, see Table 2, PM50 Supported Port Modes.

For the rates that the ELK interface supports, see Table 6, ELK-over-ILKN Supported Rates and Electrical Specifications Standards.

5.10.3 Blackhawk SerDes Receiver

The Blackhawk receiver features are as follows:

- Integrated AC coupling on RX inputs.
- 3-stage analog peaking filter (PF).
- 3-stage controlled variable gain amplifier (VGA).
- 14-tap DFE (six fixed and eight floating) with adaptive control slicer.
- Clock phase interpolation in receiver timing recovery.
- Programmable RX polarity inversion.

The following table lists the electrical characteristics of the SerDes receiver.

Table 46: SerDes Receiver Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Input common mode	V_{IN-CM}	—	530	900	mV	Higher than the maximum V_{IN-CM} requires external AC capacitor on board, 100 nF.
Input differential swing	$V_{IN-DIFF}$	85	—	1600	mVppd	—
Absolute maximum RX input	V_{IN-Abs}	0	—	1100	mV	Measured RX_P to GND and RX_N to GND.

5.10.4 Blackhawk SerDes Transmitter

The Blackhawk transmitter features are as follows:

- Transmitter with fully programmable 6-tap FIR
- IEEE 802.3 link training
- Programmable TX polarity inversion
- TX disable
- Controlled peak-to-peak amplitude

Table 47 lists the electrical characteristics of the SerDes transmitter.

Table 47: SerDes Transmitter Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Output common mode	V_{OUT-CM}	—	0.45	—	V	When terminated with 100Ω differential
Output differential swing	$V_{OUT-DIFF}$	0	—	1050	mVppd	Programmable

Chapter 6: Thermal Specifications

6.1 Absolute and Operational Thermal Specifications

The BCM88690 is a multi-die device. The package contains the main ASIC die from Broadcom and two HBM dies from the memory vendor. Take this structure into consideration when planning the thermal definitions and thermal design.

The following table shows the specifications for the absolute thermal limits.

Table 48: Absolute Thermal Limit Specifications

Parameter	Min.	Max.	Unit
Storage temperature	–40	+100	°C
Main die maximum junction temperature	N/A	+110[a]	°C
HBM die maximum junction temperature	N/A	+95[b]	°C
HBM CATTRIP assertion temperature	N/A	+120[c]	°C

a. Operating at a temperature above the maximum T_J may cause permanent damage to the device.
A maximum excursion temperature of T_J = 125°C for 15 days per year (for less than 96 consecutive hours) is allowed. Proper functionality and performance cannot be guaranteed when the device operates above the maximum junction temperature.

b. Over the HBM lifetime, a maximum excursion temperature of 105°C for a total of 360 hours per year is allowed. A single excursion period should not be longer than 96 hours, and the time between two consecutive excursion periods is a minimum of 24 hours. During these excursion periods, the HBM performance and reliability are not affected. When violating the excursion conditions, functional operation failures and reliability degradation are expected.
At 105°C, the total power each HBM consumes is 15W (instead of 12W). To calculate the consumption per rail, use a factor of × 1.25 for HBM[1:0]_VDDO, HBM[1:0]_VDDC, and HBM[1:0]_VPP2P5.

c. Operation above the CATTEMP (120°C) will result in immediate and permanent damage to the device.

Table 49: HBM Operating Temperature (Junction, HBM Is Powered On)

Parameter	Symbol	Min.	Max.	Unit
Standard operating temperature	HBM_T_N	0	85	ºC
Extended operating temperature[a]	HBM_T_E	85	95	ºC

a. The HBM extended operating temperature requires additional refresh cycles, which are inserted by the controller.

NOTE: When the HBM is powered-on, it must comply with the HBM_T_N or HBM_T_E values. The HBM must be powered-down if the die temperature is below the HBM_T_N minimum or above the HBM_T_E maximum.

Table 50: HBM Exceeding Temperature (Junction, HBM Is Powered Off)

Parameter	Symbol	Min.	Max.	Unit
Exceeding temperature[a]	HBM_T_{EXCEED}	95	125	ºC

a. The *exceeding* temperature is the temperature that exceeds the extended temperature. For the HBM die, an exceeding junction temperature of 95°C to 125°C for 96 hours per year is allowed as long as the following conditions are met:
1. The HBM is powered-down by the board (follow the power-down sequence as described in Section 5.5.5, HBM-Only Power-Down and Power-Up).
2. The total duration per year is less than 96 hours.
During these exceeding periods, the HBM reliability is not affected. When violating the exceeding temperature conditions, functional operation failures and reliability degradation are expected.

NOTE: For additional thermal information (including information about the temperature excursion), refer to *Thermal Considerations for High-Power Switching Devices* (StrataDNX-StrataXGS-AN1xx).

Table 51: Ambient Temperature Conditions

Parameter	Min.	Max.	Unit
Commercial temperature grade	0	+70	°C

6.2 Package Thermal Specifications

6.2.1 Block Thermal Model

The Block thermal model includes separate entities for the main die and the two HBM dies.

The HBM junction temperature can be read directly from the thermal simulation, and there is no need to use a formula for extracting the HBM temperature from the simulated main die temperature.

In addition, the user can update power consumption values for the main die and HBM dies without needing an updated thermal model. The model default settings are 340W for the main die and 12W for each HBM die. For the device maximum power consumption values, see Section 5.3, Device Power Consumption.

The BCM88690 block thermal model is available on the Customer Support Portal (docSAFE). Refer to the `BCM88690_Block_Thermal_Model_v1.zip` file. For more information about Block models, refer to the `Block_Thermal_Model_Brief.pdf` document, which is part of the Block model package available on docSAFE.

Use only the block thermal model to perform thermal simulations. The block thermal model replaces all previous models, such as the 2R model, modified 2R model, and Delphi model. Accordingly, Broadcom does not provide θ_{JC} and θ_{JB} values for the device.

6.3 Temperature Monitoring

6.3.1 PVTMON

The BCM88690 has four internal on-die temperature sensors that can be accessed by the software API. These monitors (PVTMON) can be used only while the device is operational. They have an accuracy of ±3°C.

According to simulations, the BCM88690 hot-spot junction temperature is 2°C higher than the maximum of all four PVTMONs.

6.3.2 Thermal Diodes

The BCM88690 has two on-die thermal diode that is not coupled to any of the BCM88690 power sources nor associated with any of its logic. This enables the temperature to be read while the device is powered off or in a nonoperational condition (such as during a reset).

The diode circuit has an independent supply rail, THERM_DIODE_VDD3P3.

To measure and read the on-die thermal diode indications, external circuitry is required.

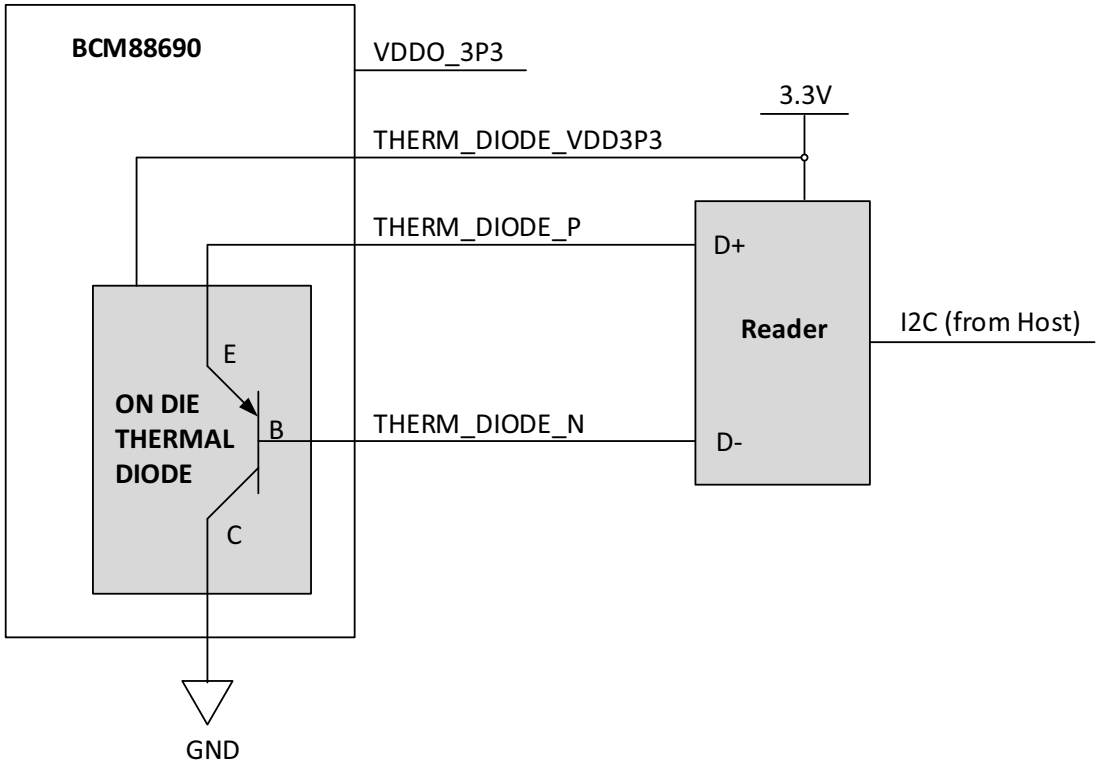
The following table shows the specifications of the on-die thermal diode.

Table 52: On-Die Thermal Diode Specifications

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating temperature	T	—	0	—	+125	°C
Force current	I_D	—	5	—	120	µA
Forward voltage	VBE	Minimum at 5 µA	0.25	—	—	V
		Maximum at 120 µA	—	—	0.95	
Ƞ – Ideality factor	—	—	—	1.008	—	—
Base bias (informative)	—	—	—	0.6	—	V
Accuracy[a]	—	–40°C to 110°C	–2.5	—	+2.5	°C
		110°C to 125°C	–1.5	—	+1.5	

a. The accuracy figures are for diode currents of 120 µA and 6 µA.

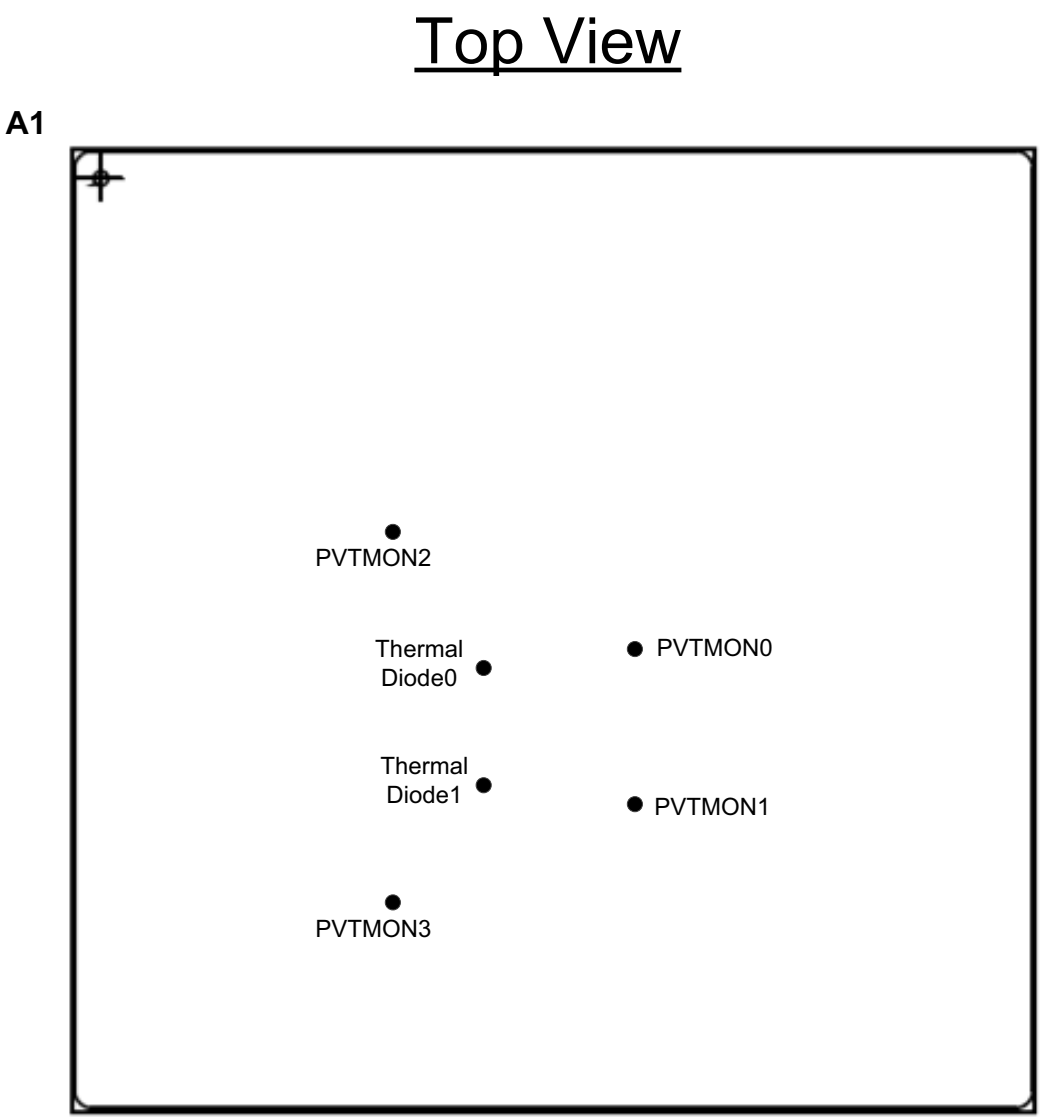
Figure 26: Example Application Using the On-Die Thermal Diode



6.3.3 On-Die Thermal Monitor Locations

The locations of the thermal monitors relative to the device's package are shown in the following figure.

Figure 27: BCM88690 On-Die Thermal Monitors



6.4 Reflow Temperature

Broadcom offers a lead-free package.

NOTE: For additional reflow process recommendations, refer to *Broadcom BCM88690 SMT Recommendations Ver0 04-05-2018* (BCM88690_SMT-Guide-r0_4-05-2018).

Table 53 provides information about the solder ball composition and recommended and maximum reflow temperature.

Table 53: Solder Ball Composition and Recommended and Maximum Reflow Temperature

Part Number	Solder Ball Composition	Recommended Reflow Peak Temperature	Maximum Allowed Reflow Peak Temperature
Pb-free RoHS-compliant package	96.5% Sn, 3% Ag, 0.5% Cu	232°C to 237°C	245°C

6.5 Heat Sink Considerations

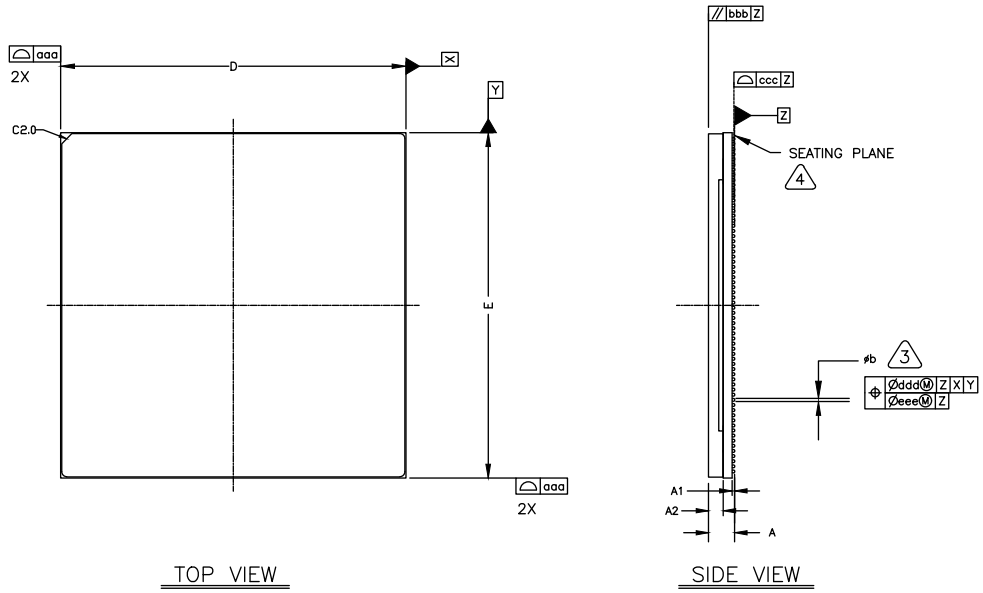
For information about the heat sink, refer to the *DNX16 Hardware Design Guidelines for StrataDNX 16-nm Devices* application note (DNX16-AN1xx).

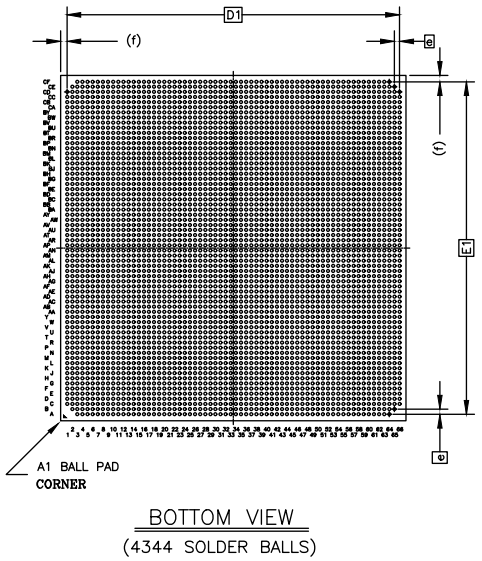
Chapter 7: Packaging

The BCM88690 family uses a Type I (2.5D) package to fit devices that include HBM (see Figure 28).

7.1 Type I: 2.5D Package

Figure 28: 2.5D Package





DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	5.14 REF	5.39 REF	5.64
A1	0.4	0.5	0.6
A2	2.81	2.86	2.91
D	67.40	67.50	67.60
D1		65.00 BSC	
E	67.40	67.50	67.60
E1		65.00 BSC	
b	0.535	0.635	0.735
e		1.00 BSC	
f		1.25 REF.	
aaa	–	–	0.20
bbb	–	–	0.25
ccc	–	–	0.20
ddd	–	–	0.25
eee	–	–	0.10

5. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY E REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

4 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MS-034E.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Related Documents

The references in this section may be used with this document.

NOTE: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (docSAFE) and Downloads and Support site.

For document numbers and file names, replace the “xx” or “X.X” with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Broadcom Items		
[1] *Hardware Design Guidelines for StrataDNX 16 nm Devices*	DNX16-AN1xx	Broadcom CSP
[2] *BCM88690 Packet Processing Programming Guide*	88690-PG1xx	Broadcom CSP
[3] *BCM88690 Traffic Manager Programming Guide*	88690-PG2xx	Broadcom CSP
[4] *BCM88690 Final PinList*	BCM88690_PinList_Rev1pX.zip	Broadcom CSP
[5] *BCM88690 SMT Recommendations Ver0 04-05-2018*	BCM88690_SMT-Guide-r0_4-05-2018	Broadcom CSP
[6] *Thermal Considerations for High-Power Switching Devices*	StrataDNX-StrataXGS-AN1xx	Broadcom CSP
[7] *BCM88690 Device Errata*	88690-ER1xx	Broadcom CSP