BCM56070

Hardware Design Guidelines

Design Guide

Table of Contents

Chapter 1: Introduction

This document describes the hardware design guidelines for the BCM56070 family of devices. It describes the electrical characteristics for the high-speed external I/O interfaces used on these devices, provides a diagram of how each high-speed interface must be connected, and provides routing examples when applicable.

For a complete and detailed functional description on all interfaces in the device, refer to the BCM56070 data sheet (56070-DS1xx).

NOTE: References to the BCM56070 device apply to all part numbers in the BCM56070 device family unless stated otherwise.

Chapter 2: High-Speed SerDes Cores

The BCM56070 device includes the following SerDes cores:

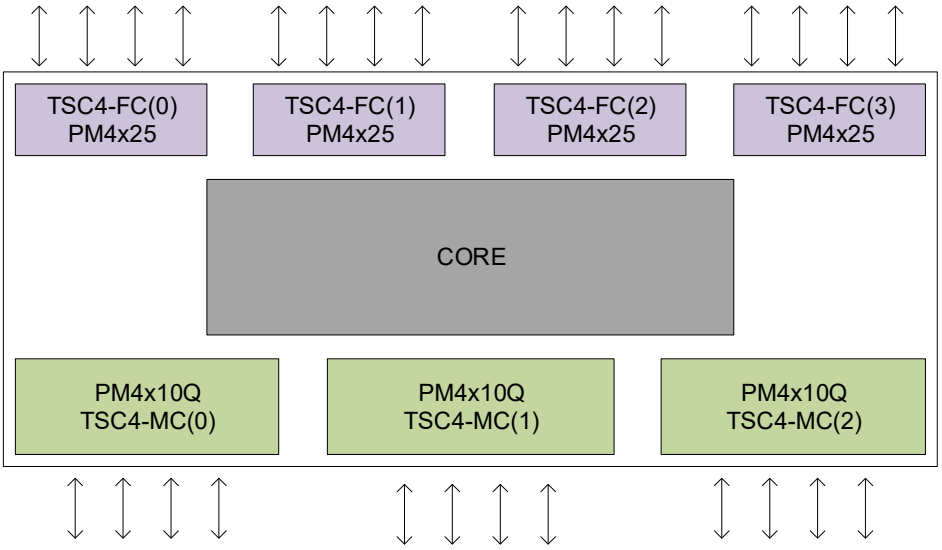
- TDM-based SerDes Controller (TSC) cores for front-panel and backplane ports
- PCIe core for communication with the host processor

2.1 TSC Cores

The BCM56070 device incorporates two different TSC SerDes cores for front-panel and backplane ports:

- Merlin (TSC4-MC)
- Falcon (TSC4-FC)

Figure 1: Chip-Level View of TSC Cores

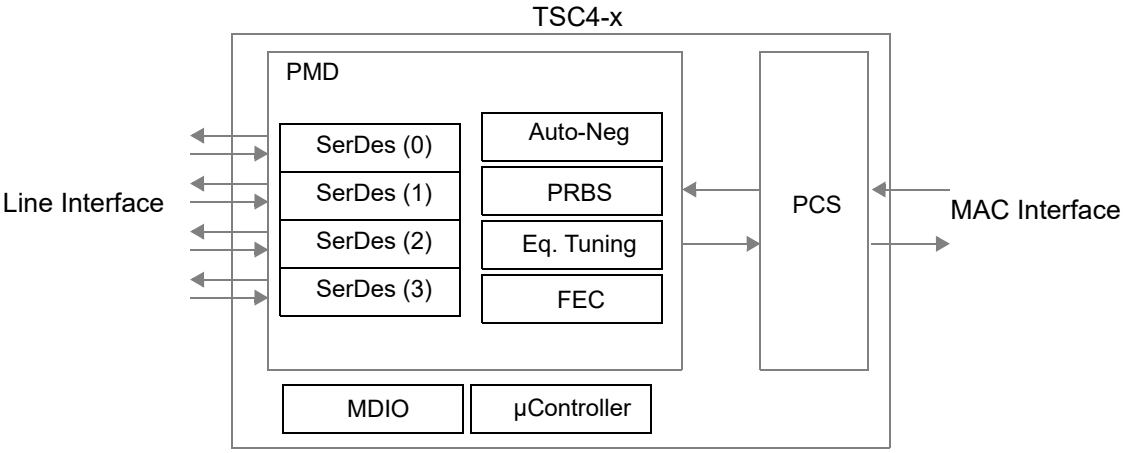


NOTE: Falcon and TSC4-FC may be used interchangeably throughout the document. All instances refer to the TSC Falcon SerDes core. Similarly, Merlin and TSC4-MC refer to the TSC Merlin SerDes core.

The Falcon and Merlin SerDes cores are similar in organization, with four SerDes lanes supporting logic for various lane configurations and speeds. The BCM56070 includes three Merlin instances and four Falcon instances, as the previous figure shows.

Generically, the Merlin and Falcon SerDes cores are referred to as TSC4-x. The following figure illustrates the various functional blocks in the TSC4-x SerDes core, which is made up of four SerDes lanes and the supporting digital logic.

Figure 2: TSC4-x Block Diagram



The TSC4-x interface requires a controlled differential trace impedance. The device has on-chip termination on its receiver inputs, eliminating the need for external resistors in most applications.

In most cases, external AC-coupling capacitors are not required in the RX path because the TSC4-x provides on-die AC capacitors in the receive path. This on-die AC coupling cannot be bypassed.

Any peer device (receiver) that interfaces to the TSC4-x transmitter must have AC-coupling; either an external capacitor on the PCB or an on-chip capacitor in the remote receiver.

External capacitors are required in the TSC4-x receive path if the single-ended voltage on either leg of the differential input is less than –300 mV or greater than 1100 mV.

Hot-plug applications require AC-coupling capacitors on the PCB to prevent in-rush currents into the RX-AFE of the SerDes.

If an external capacitor is required, use a 100-nF capacitor with a 0201 footprint to minimize reflections.

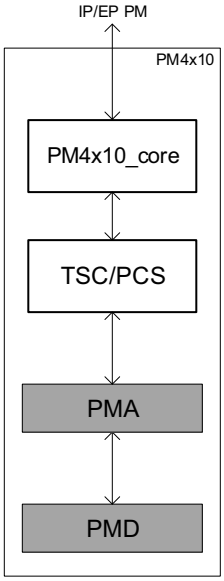
NOTE: Refer to the BCM56070 data sheet (56070-DS1xx) for a complete list of supported speeds and any restrictions regarding Merlin and Falcon core configurations. Also note that half duplex is *not* supported at any speed.

Should discrepancies occur between this document and the data sheet, the data sheet information takes precedence.

2.1.1 Merlin SerDes Core

The BCM56070 includes three Merlin instances. The following figure shows a basic block diagram.

Figure 3: Merlin Basic Block Diagram



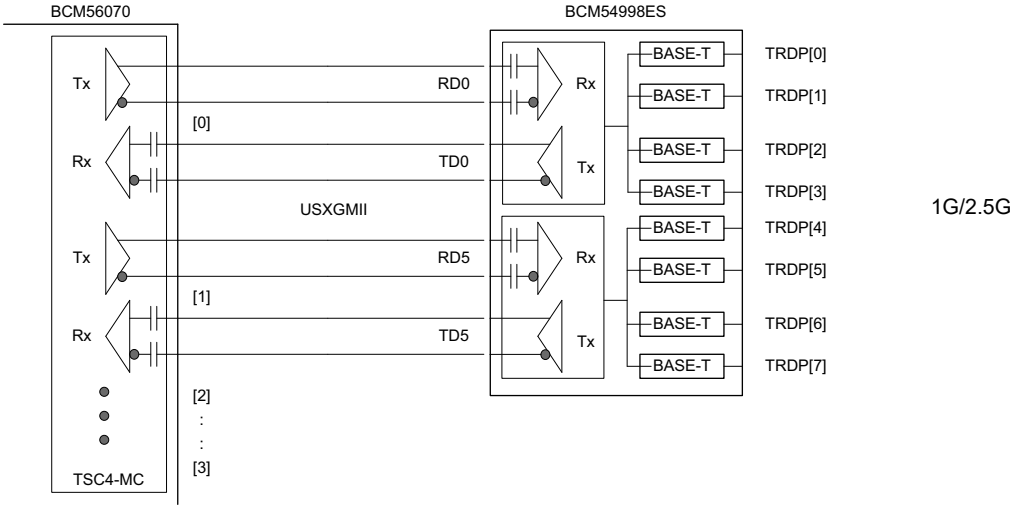
2.1.1.1 Merlin Modes of Operation

The two basic modes of operation for the Merlin SerDes core are as follows:

- QMODE
- TSC mode

In QMODE, the interface is USXGMII, and each lane can support up to four ports and up to 16 ports across the four-lane core. Converting the USXGMII to four physical ports (per lane) requires an external PHY. This mode supports typical speeds of 100M, 5G, 1G, and 2.5G. Mixing Ethernet mode and Q mode lanes is not supported. For a complete list of supported speeds for this SerDes core, refer to the data sheet (56070-DS1xx). The following figure shows an example connection diagram.

Figure 4: Typical Merlin Connection Diagram (QMODE = 1)



In TSC mode (QMODE = 0), each lane can support a single port, or multiple lanes can be aggregated to form a single port. This mode typically supports speeds of 10G, 20G, and 40G.

The Merlin interface has programmable transmit amplitude and preemphasis control. This feature is ideal for backplane and cable applications that may require the interface to drive long trace and cable lengths. To achieve the best performance for a given layout, empirically verify the proper setting.

2.1.1.1.1 Single-Lane Configuration

In single-lane configurations, each Merlin core supports up to four independent ports. Refer to the data sheet for a list of supported single-lane port speeds for the Merlin core.

2.1.1.1.2 Two-Lane Configuration

In two-lane configurations, each Merlin core supports up to two independent two-lane ports. Refer to the data sheet for a list of supported two-lane port speeds for the Merlin core.

2.1.1.1.3 Four-Lane Configuration

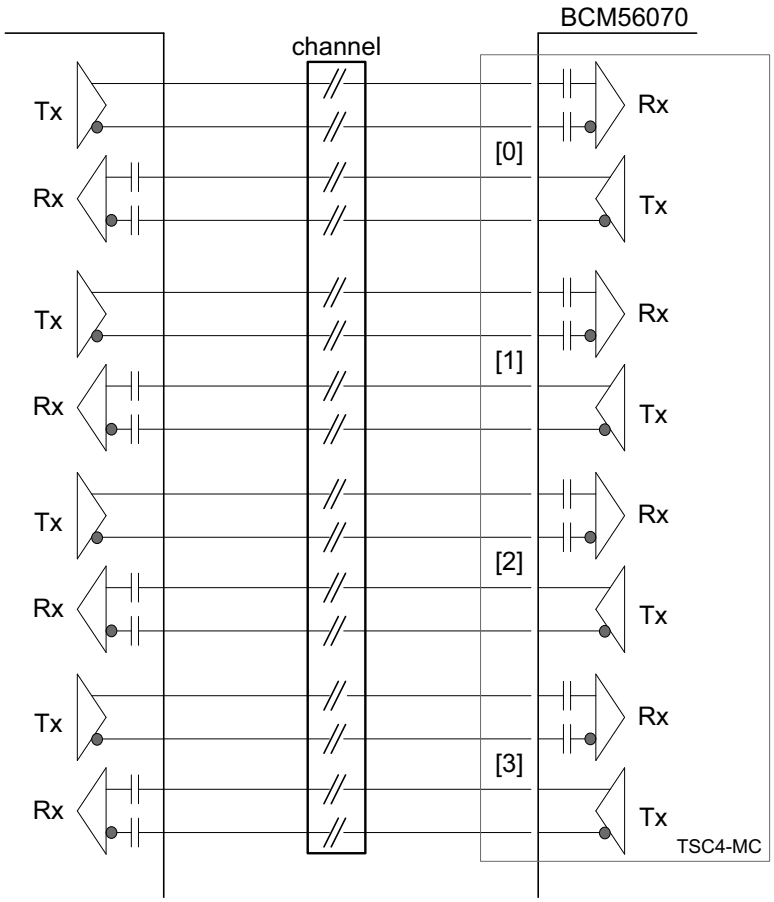
In four-lane configurations, a Merlin core can support a single port spanning all four lanes of the module. Refer to the data sheet for a list of supported four-lane port speeds for the Merlin core.

2.1.1.2 Merlin Connection Diagram

In all configurations, PCB design rules are restrictive and simulations are required. For details, see Section 11, Falcon and Merlin Modeling and Simulations and Section 7.2, 10G PCB Layout Guidelines.

The following figure shows a typical connection diagram.

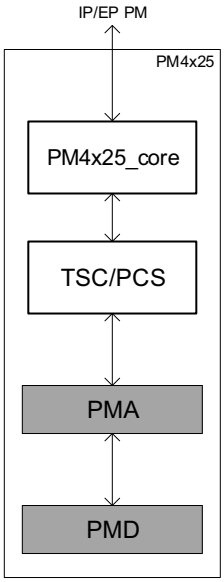
Figure 5: Typical Merlin (TSC4-MC) Connection Diagram (QMODE = 0)



2.1.2 Falcon SerDes Core

The BCM56070 includes four Falcon SerDes core instances. The following diagram shows a basic block diagram.

Figure 6: Falcon Basic Block Diagram



2.1.2.1 Falcon Modes of Operation

The operating port speed for a single Falcon SerDes core ranges from 10.3125 Gbaud to 27.3438 Gbaud. Falcon can be configured in any of the following modes:

- One-lane mode with each Falcon supporting up to four independent lanes (ports)
- Two-lane mode with each Falcon supporting up to two dual lanes (ports)
- Four-lane mode with each Falcon supporting a single port spanning four lanes

The BCM56070 Falcon interface has programmable transmit amplitude and preemphasis control. This feature is ideal for backplane and cable applications that may require the interface to drive long trace or cable lengths. The proper setting must be empirically verified to achieve the best performance for a given layout. For additional information, refer to the *TSC SerDes Debugging Guide* (TSC-E_TSC-F-AN1xx).

2.1.2.1.1 Single-Lane Configuration

In single-lane configurations, each Falcon core supports up to four independent ports. Refer to the data sheet for a list of supported single-lane port speeds for the Falcon core.

2.1.2.1.2 Two-Lane Configuration

In two-lane configurations, each Falcon supports up to two independent two-lane ports. Refer to the data sheet for a list of supported two-lane port speeds for the Falcon core.

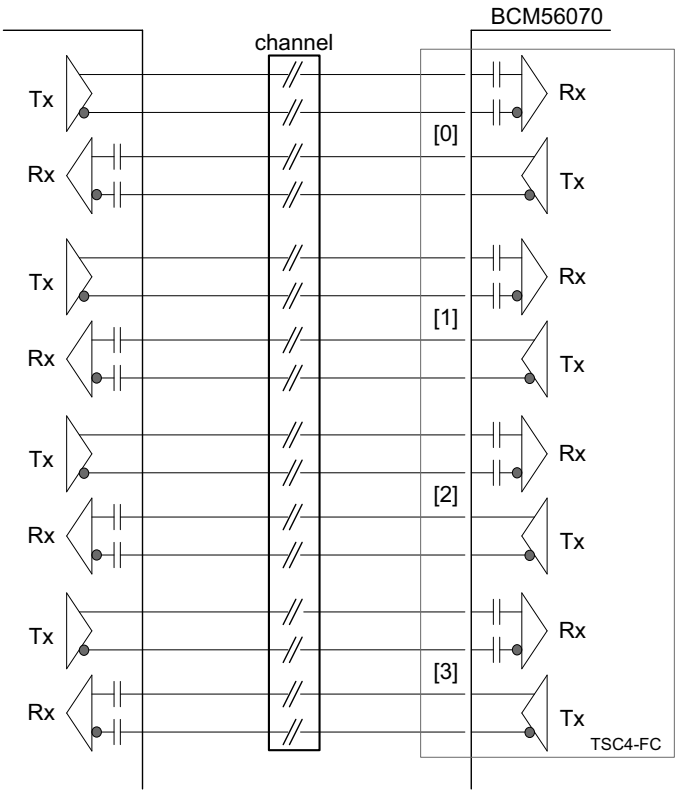
2.1.2.1.3 Four-Lane Configuration

In four-lane configurations, a Falcon can support a single port spanning all four lanes of the module. Refer to the data sheet for a list of supported four-lane port speeds for the Falcon core.

2.1.2.2 Falcon Connection Diagram

In all configurations, PCB design rules are restrictive, and simulations are required. For details, see Section 11, Falcon and Merlin Modeling and Simulations and Section 7.1, 25G PCB Layout Guidelines.

Figure 7: Typical Falcon (TSC4-FC) Connection Diagram



2.1.3 Falcon and Merlin PLL VCO Frequency Limitation

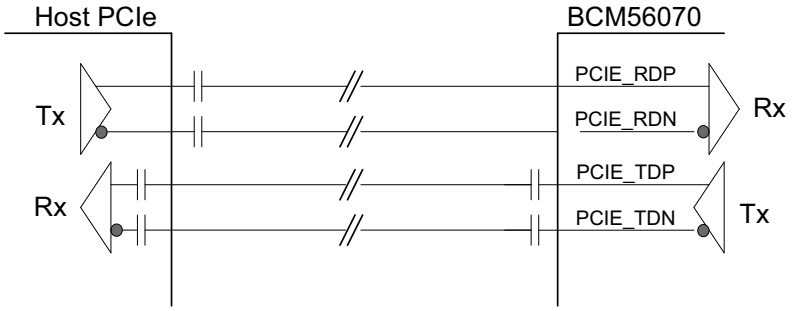
Each TSC core has a single PLL that is shared across all four SerDes lanes. The operating speed for each port within a TSC must be derived from this common PLL VCO frequency. The per-lane oversample (OSx) controls effectively reduce the PLL VCO frequency to the target frequency based on the port or lane speed.

For example, a Falcon core can be configured as a 1 × 20G (two-lane) port and 2 × 10G ports. In this configuration, the PLL is configured for 20G. The port operating at 10G will be configured in OSx2 mode, resulting in a 10G lane speed with an aggregate port speed of 20G. In this configuration, the 1 × 20G port and the 2 × 10G ports may coexist within a Falcon core.

2.2 PCIe SerDes (CPU Interface)

The BCM56070 is a x1 PCIe Gen3-capable device, and the BCM56070 PCIe interface conforms to the PCIe version 3.0 specification. The BCM56070 supports a single lane of PCIe (8 Gb/s in each direction). No external glue logic is required to support this interface. The protocols and electrical requirements of the PCIe specifications are strictly implemented. Unlike the PCI local bus interface, which is a parallel bus using reflected wave switching, the PCIe interface consists of a serial point-to-point interface that propagates data through differential pairs.

Figure 8: PCIe Interface Connection



2.2.1 PCIe Gen3 and QSPI Flash

PCIe Gen3 requires microcode to be loaded into the PCIe SerDes during initialization. This is achieved by using mHost0 to fetch microcode from an external flash memory (EEPROM) and push it into the PCIe SerDes.

This Quad Serial Peripheral Interface (QSPI) flash device is connected to the IP_QSPI interface and must be strapped so the device will download from this memory. The firmware configures the PCIe interface into a functionally compliant Gen3 mode.

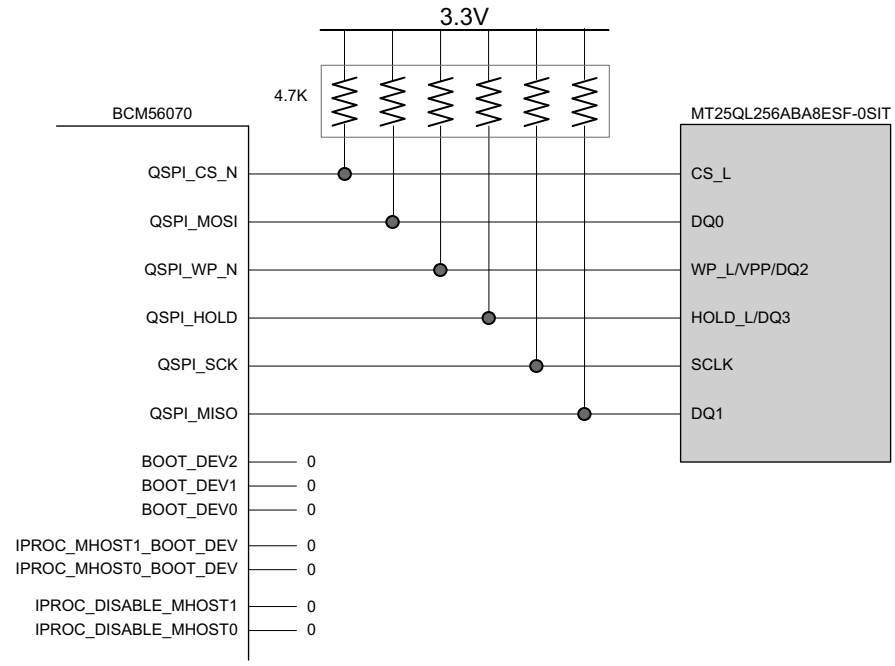
The strap settings are as follows:

- BOOT_DEV[2:0] = 3’b000.
- IPROC_MHOST[1:0]_BOOT_DEV = 2'B00.
- PCIE_FORCE_GEN[1:0] = 2’b00.
- QSPI flash memory is programmed with firmware provided by Broadcom®.
- QSPI flash memory is connected to IP_QSPI interface.

All designs should include an EEPROM device connected using the QSPI interface for PCIe Gen1, Gen2, and Gen3 operation. If the device is strapped to operate at Gen1 or Gen2 speeds, it is still required to populate and connect the QSPI flash device because this is used if any hard-reset register settings need to be tuned for optimal PCIe Gen2/Gen1 operation.

NOTE: Include a QSPI flash memory containing the Broadcom-provided PCIe firmware. Strap the device to download and execute the code from this flash memory for the PCIe interface to be functional. Refer to the *BCM56070 A0 K Version SVK Schematics* file for the connection circuit and example part number.

Figure 9: PCIe QSPI EEPROM Interface



2.2.2 PCIe PCB Routing and AC-Coupling

PCIe Gen3 supports speeds of 8 Gb/s, so follow routing guidelines for speeds of up to 10 Gb/s. For more information, see Section 7.2, 10G PCB Layout Guidelines. Refer to the *PCI Express Base Specification Revision 1.0a* for additional information related to routing and AC-coupling.

Series AC-coupling capacitors are required in the data path. The PCIe specification (version 3.1) recommends capacitor values in the range of 176 nF to 265 nF, with 220 nF as the typical value. The PCIe specification (version 2.0) recommends typical capacitor values in the range of 75 nF to 200 nF. All PCIe differential pairs must be routed as a closely coupled pair with a differential impedance of 100Ω. Place the AC-coupling capacitors as close to the transmitter buffer as practical. This ensures that the DC bias levels of the transmitted signal do not adversely affect the receiver.

The within-pair trace lengths must be length-matched within 5 mils to minimize skew.

Route all PCIe differential pairs as a closely coupled pair with a differential impedance of 100Ω. To minimize skew, match the length of the within-pair trace lengths to within 5 mils.

Minimize the number of vias in the trace path. Vias must always match in number on each differential pair and be collocated whenever possible.

2.2.3 PCIe Active-State Power Management

Disable active-state power management (ASPM) in the system for normal operation. The device does not support this feature. If this feature is enabled, the device may not initialize properly.

2.2.4 PCIe Reset

The device supports the following three reset modes per PCIe standards:

- Cold Reset: Applying the fundamental reset mechanism by toggling the PCIE_PERST_L signal following the application of power to the component.
- Warm Reset: Applying the fundamental reset mechanism by toggling the PCIE_PERST_L signal without the removal and application of power to the component. The timing requirements must be similar to that of Cold Reset, except that there are no changes in power events.
- Hot Reset: An inband mechanism where a reset is propagated across the link by software. The inband mechanism forces a link into the electrical idle state and going through a hot reset.

When the switch device operates as an End Point (EP), the Root Complex (RC/CPU) issues either a Warm Reset or Hot Reset. Regardless of any reset modes, it is a requirement to connect the PCIE_PERST_L signal directly from the switch to the CPU.

NOTE: Although the PCIe standards do not require toggling the PCIE_PERST_L signal during Hot Reset, it is a Broadcom requirement to support the Hot-Swap requirements. Failure to toggle PCIE_PERST_L will not reset the PCIe core within the switch.

All power-up and reset sequences must adhere to the timing diagram specified in the data sheet. Refer to the data sheet for timing on VDDC, SYS_RST_L, PCIE_PERST_L, PCIE_REFCLK, and XTAL.

Chapter 3: Clock Requirements

The BCM56070 requires the clocks and PLL sources shown in the following table. Refer to the BCM56070 data sheet (56070-DS1xx) for the clock input electrical requirements.

Table 1: BCM56070 Clock Requirements

Clock Input	Clock Requirement	Description
XTAL	Input type = Differential Frequency = 50 MHz	Generates a reference clock for the digital core logic.
PCIe_REFCLK	Input type = Differential Frequency = 100 MHz	PCIe SerDes reference clock. Includes on-chip AC-coupling capacitors. Requires an external 100Ω termination resistor.
TS_PLL_FREF	Input type = Differential Frequency = 50 MHz	TimeSync reference clock input. Requires external series AC-coupling 0.01-µF capacitors. Includes on-chip 100Ω differential termination resistors.
BSPLL[1:0]_FREF	Input type = Differential Frequency = 50 MHz	BroadSync® reference clock input. Requires external series AC-coupling 0.01-µF capacitors. Includes on-chip 100Ω differential termination resistors.
LCPLL0_FREF	Input type = Differential Frequency = 50 MHz, 156.25 MHz	Reference clock for SerDes. The required input for most applications, including IEEE 1588, is 156.25 MHz. For applications that require a minimum jitter single-source input to BSPLL, TS_PLL, and LCPLL0 (such as the telecom DPLL implementation), provide a 50-MHz OCXO high accuracy clock input. Requires external series AC-coupling 0.01-µF capacitors. Includes on-chip 100Ω differential termination resistors.

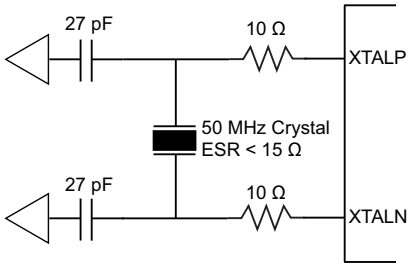
NOTE: The TS_PLL_FREF and BSPLL[1:0]_FREF are optional inputs if the TimeSync (TS) and BroadSync (BS) features are not used.

3.1 Chip Reference Clock (XTALP/XTALN)

To support a low retail bill of materials (RBOM) cost solution, the BCM56070 requires only one 50-MHz fundamental mode crystal device for the entire device. This information is for a solution without TimeSync applications. Optional clock sources are required for TimeSync applications. When a crystal is used, the external load capacitors are required and two series resistors should be reserved on the XTALP/N pins. The capacitor and resistor values can be changed upon PCB design and crystal selection.

For 50-MHz operation, use a crystal of ESR ≤ 15Ω and CL ≥ 18 pF with C1 and C2 of 27 pF. The component that meets this specification is 7M50070012 from TXC. A component with these requirements might not be necessary for 50-MHz operation. Tune the frequency to center at ±10 ppm during crystal performance verification. To measure the resonating frequency accurately, reserve test points of XTAL_ON_CML and XTAL_OP_CML. This is the buffered output of XTALP/N.

Figure 10: XTALP/N Reference Circuit



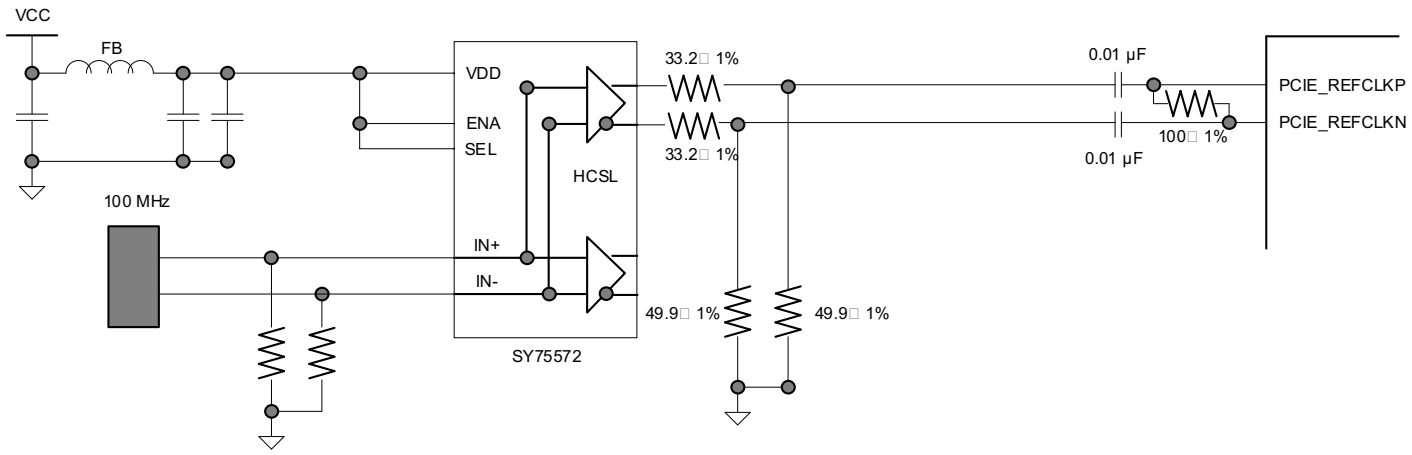
3.2 PCIE_REFCLK Clock Connection

This is a differential 100-MHz HCSL clock that drives the PCIe interface. Refer to the data sheet (56070-DS1xx) for the electrical requirements.

The following are example components:

- Oscillator: Microchip MX555ABD100M000
- Clock buffer: Microchip SY75572

Figure 11: PCIE_REFCLK Clock Connection

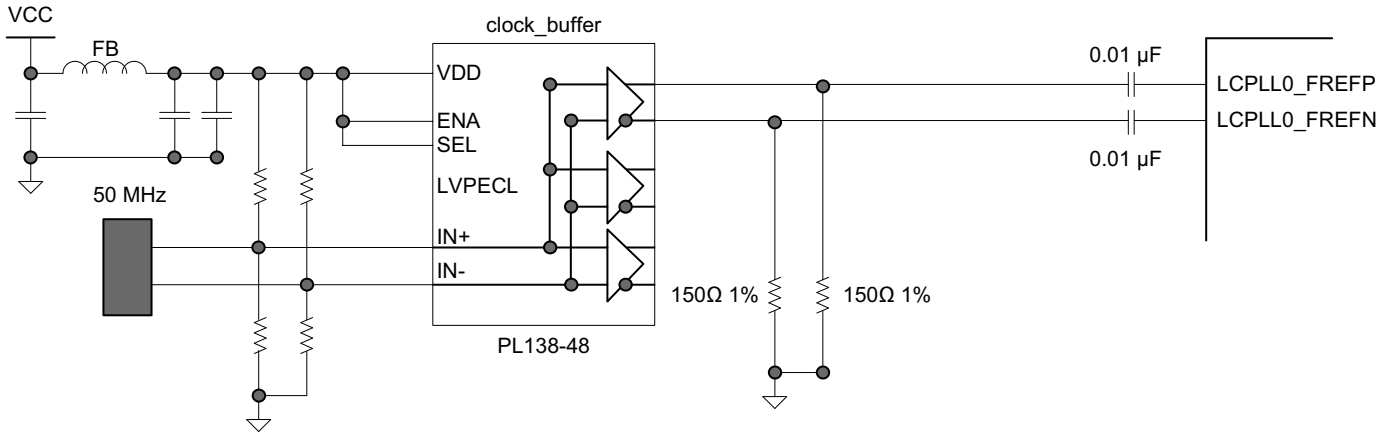


NOTE: All components shown in the connection diagrams are example components.

3.3 LCPLL0_FREF Connection

The iProc reference clock is a differential clock required to drive the iProc/CMIC logic. Its voltage swing cannot exceed the values specified in the data sheet. It must be routed with controlled impedance. The following figure shows an example using a single oscillator with a clock buffer to drive the LCPLL0_FREF input. See Table 1, BCM56070 Clock Requirements, for information related to this input, and refer to the data sheet for the LCPLL0_FREF electrical requirements.

Figure 12: LCPLL0_FREF Connection



NOTE: All components shown in the connection diagrams are example components.

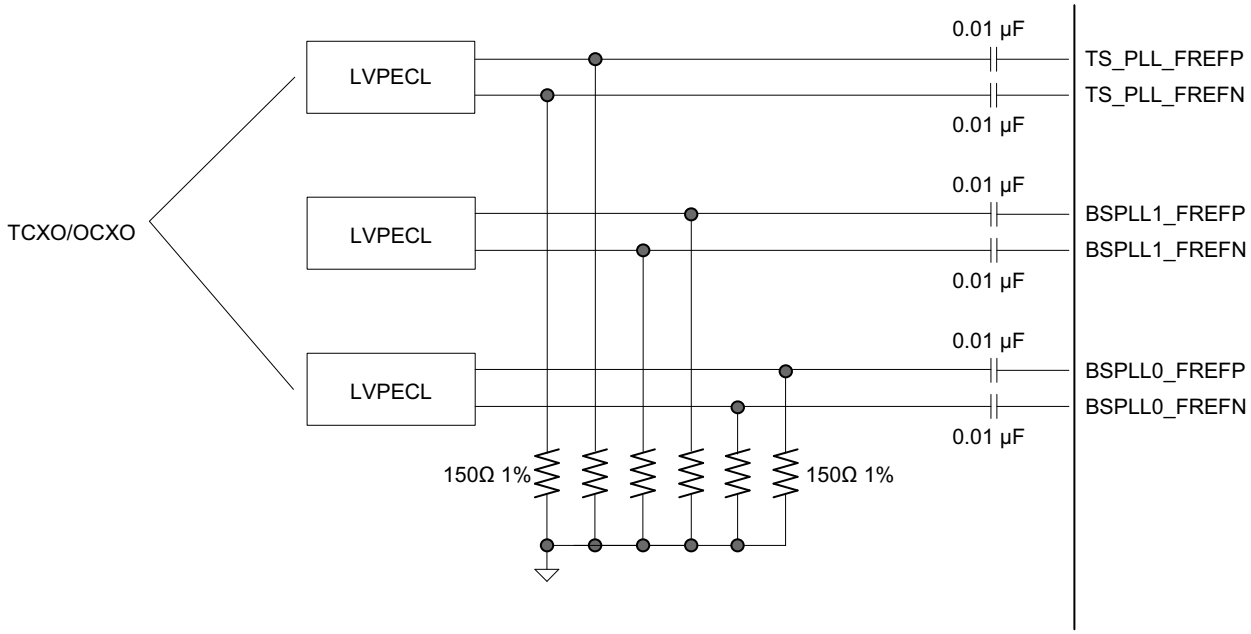
3.4 TimeSync and BroadSync Reference Clock Information

The following figure shows clock input circuit examples for the TimeSync (TS) and BroadSync reference clocks. These reference clocks have an internal termination and require external series AC-coupling capacitors (0.01 µF) on the board. Because they have internal DC biasing, they do not require external biasing resistors.

For unused TS_PLL_FREF and BSPLL[1:0]_FREF, see Section 3.5, Termination Schemes for Unused Differential Clock Inputs.

For timing-over-packet (ToP) and boundary clock applications, it is critical to have a stable crystal oscillator output. For these applications, a mini-oven-controlled crystal oscillator (OCXO) is required. A typical connection diagram is shown in the following figure.

Figure 13: TS_PLL and BSPLL Reference Clock Circuit Diagram



3.4.1 Mini OCXO Requirements

Broadcom recommends the Rakon M5948LF (RFPO40 Mercury OCXO, 50 MHz, 9 mm × 7 mm), the Rakon U6850LF (ROM1490 Mercury+ OCXO, 50 MHz, 14 mm × 9 mm), or the Rakon STP3088LF (ROX2522S4 OCXO, 50 MHz, 25 mm × 22 mm) as sources for TS_PLL_FREF and BSPLL_FREF. The M5948LF, U6850LF, and STP3088LF have been tested by Broadcom in the IEEE-1588 clock-recovery application.

When the OCXO is used either in a Timing-over-Packet (ToP) client or in a boundary clock application to provide the reference clock, it is critical to have a stable crystal oscillator output. The designs (power supply, layout, and thermals) around the OCXO must be optimized to provide the most stable conditions for the OCXO.

The output behavior of the OCXO can be altered by external conditions, such as temperature variation, reference voltage, and electrical noise. The following recommendations minimize the external influences as much as possible, given that there are other devices and signals that can create disturbances.

NOTE: The propagation delay of the buffers for frame sync and 4-kHz outputs must be less than 1 ns.

3.4.2 OCXO Power Supply and Voltage

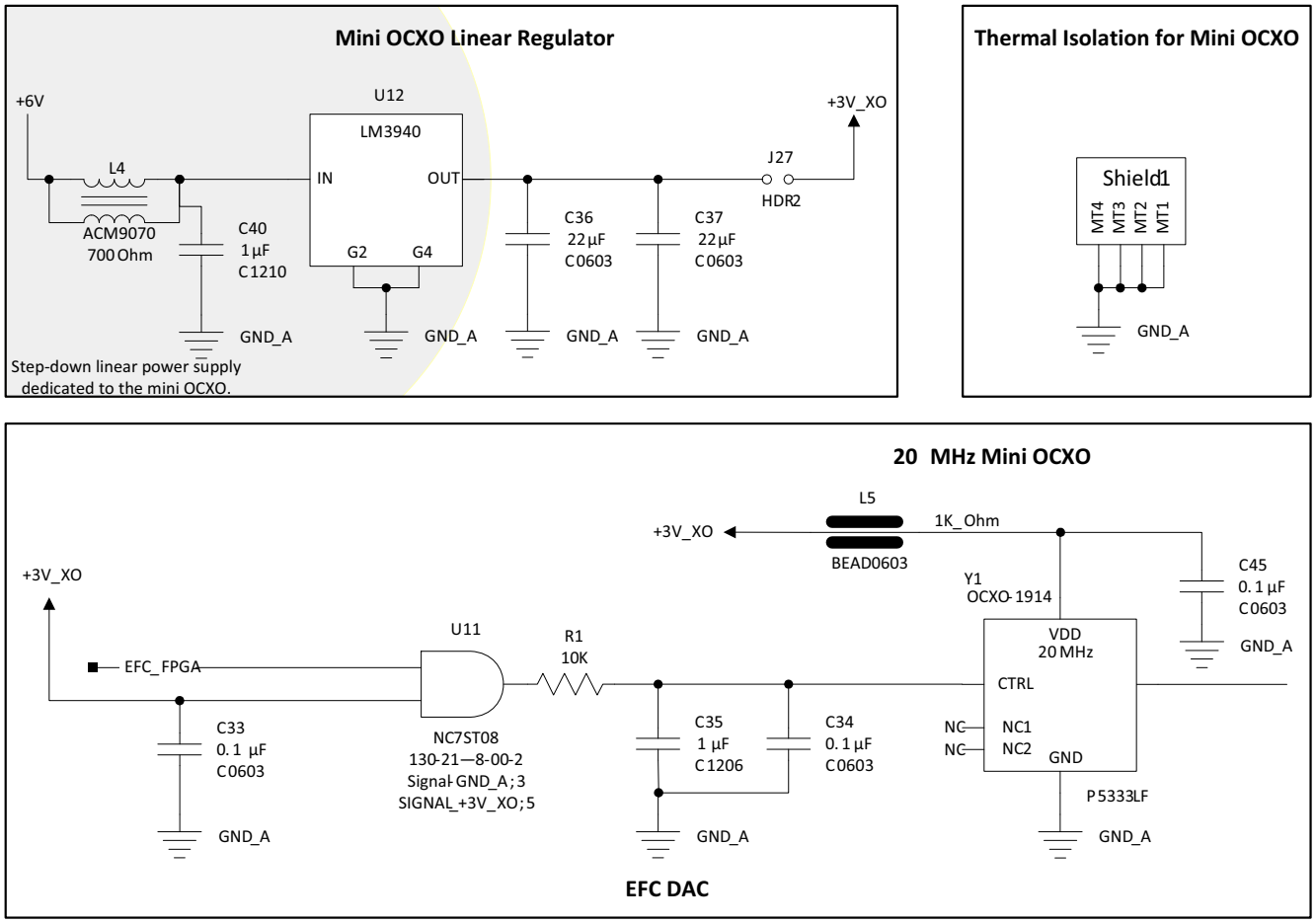
The power supply rail for the OCXO must be isolated from the power rails of all other devices. The recommended circuit is shown in the following diagram.

When a 3.3V supply is shared with other devices, filtering is critical to minimize noise and load variation.

Use a dedicated step-down linear supply using a 5V-to-12V input supply rather than inductor isolation from an existing 3.3V supply rail. Use good RF design practices when designing the circuit board, and place the OCXO close to the destination clock input to minimize noise injection across the long trace length.

The OCXO can have an initial voltage anywhere within the typical operating voltage range of ± 5% of the 3.3V supply. However, deviation from the initial voltage level during normal operation will adversely affect the stability of the output frequency. For example, the M5948LF and the STP3088LF both specify an operating voltage range of 3.3V ± 5%. If the operating voltage changes by ± 2%, the output frequency will typically change by ± 10 ppb.

Figure 14: Recommended Isolation Circuit



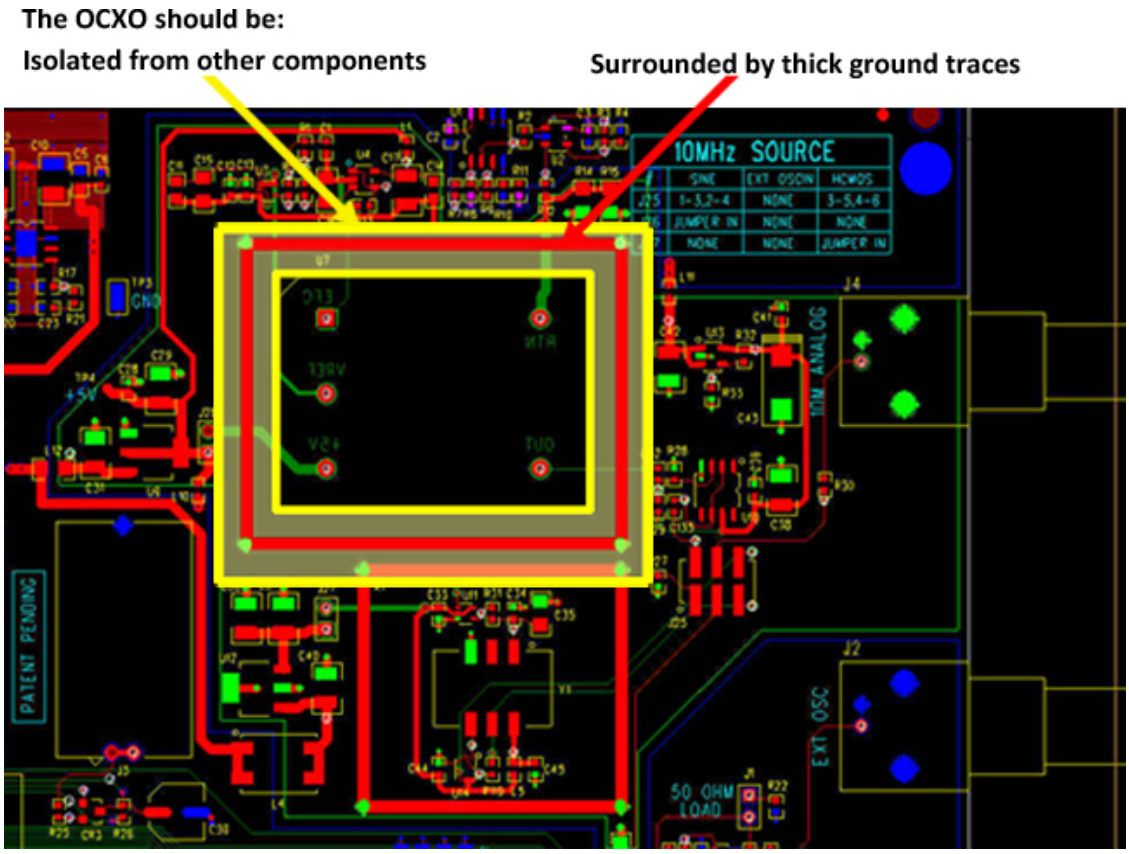
3.4.3 Mini OCXO PCB Layout Guidelines

Place the OCXO device as far from noise sources as possible. For example, avoid placement near fans, clock runs, other power supply rails, and devices that emit high temperatures.

The following figure is a layout example that illustrates how the OCXO must be isolated from the surrounding circuits.

NOTE: The device shown in the figure is not the actual part.

Figure 15: OCXO Placement on PCB

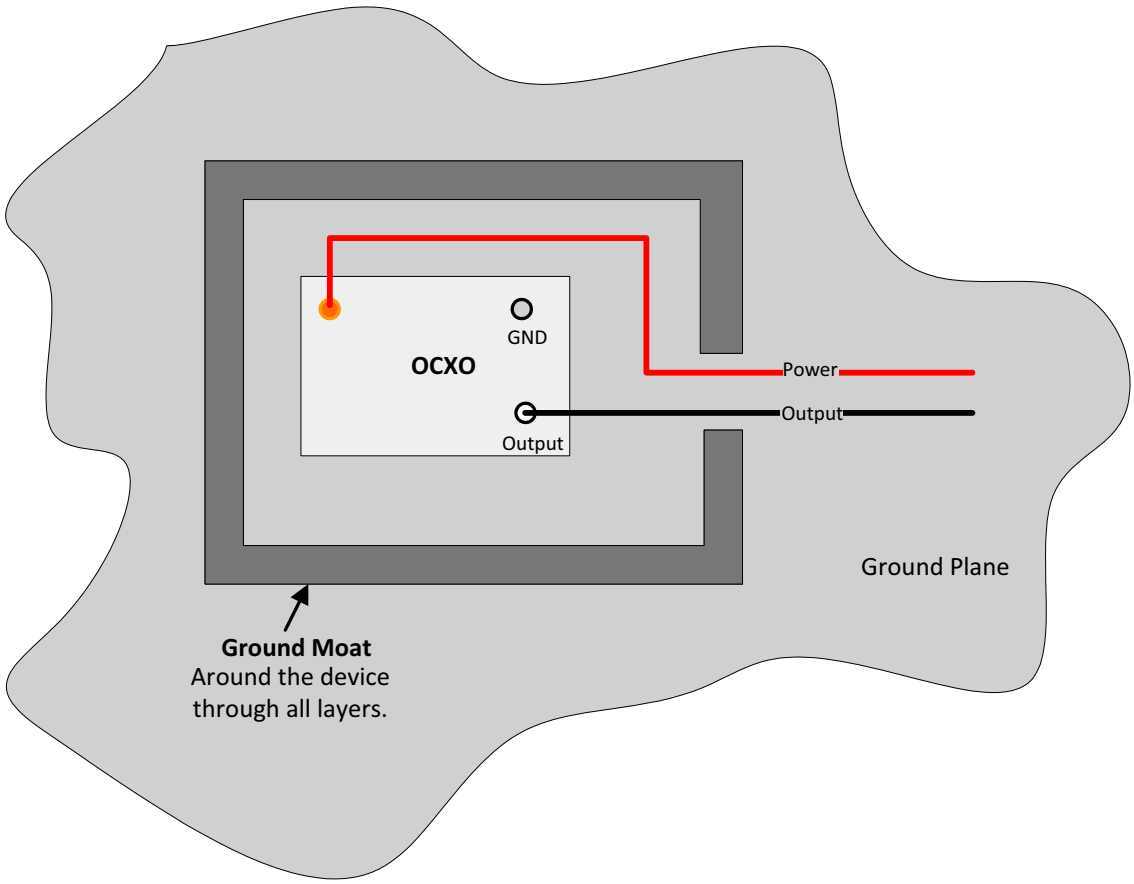


3.4.4 Alternative Mini OCXO PCB Layout

An alternative layout can be used to isolate the OCXO from the balance of the circuits. The OCXO must be separated from all noise sources. A ground moat (on all layers) must be created around the OCXO. In addition, void the ground connection only on the layer where the clock output path exists. No signal, power, or ground must go over the moat area on any layer.

The following figure illustrates this approach.

Figure 16: Alternative PCB Layout



3.4.5 OCXO Temperature Sensitivity

Temperature variation is a major factor that can impact the output frequency of the OCXO resulting in phase and frequency variations (wander). The following recommendations can minimize the temperature variation on the OCXO. In general, place the OCXO where the least temperature variation is anticipated, such as the following locations:

- Away from air vents and fans.
- Where airflow is low.
- In a location where the OCXO is fitted with an environmental cover to help isolate it from external influences (see Section 3.4.6, Environmental Protection Cover).

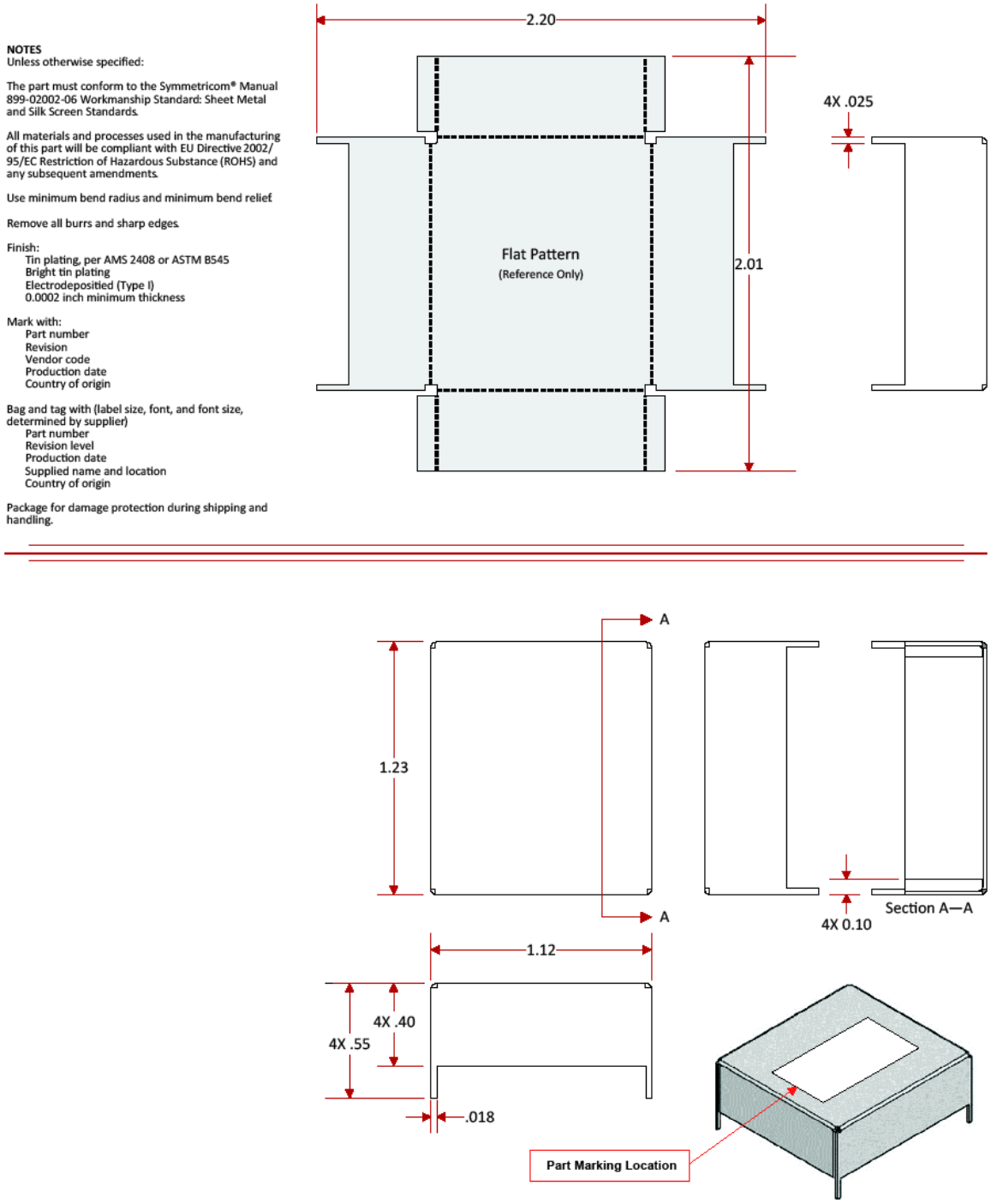
NOTE: Ensure the internal temperature of the cover does not exceed the maximum operating temperature of the OCXO.

3.4.6 Environmental Protection Cover

To shield the OCXO from potential thermal variations and changes to airflow, enclose the device in a metal cover. Connect the cover to the ground plane to avoid any electrical charge buildup.

The following figure is a mechanical drawing of a recommended cover.

Figure 17: Recommended Environmental Protection Cover

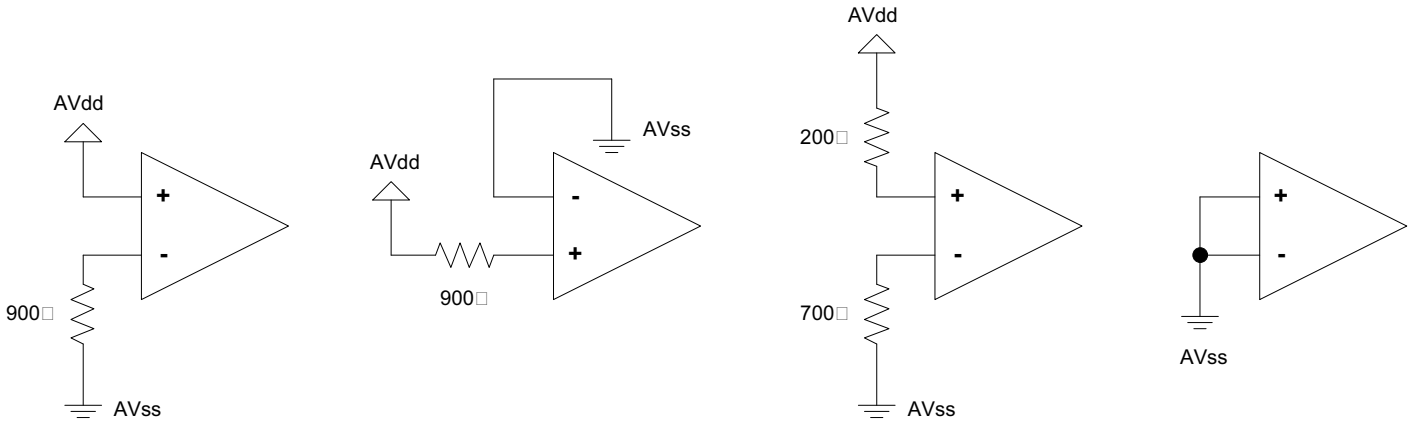


3.5 Termination Schemes for Unused Differential Clock Inputs

Recommendations for termination schemes are as follows:

- The use of any of the four termination schemes is permitted. Keep all etch as short as possible to eliminate the pickup of noise.
- The three schemes on the left provide for ~100 mV of differential potential between the P and N inputs so as to minimize the possibility of false switching. Net input current in these configurations is limited to ~1 mA.
- The simplest scheme, shorting both the P and N legs to AVss, works because the inputs are disabled when not in use.

Figure 18: Termination Schemes for Unused Differential Clock Inputs



Chapter 4: Power Supply Filtering Information

Use individual bypass or decoupling capacitors on each VDD pin whenever possible. Place these capacitors as close to the power pins as is practical. This placement may be achieved by using 0402 capacitors placed in the ball field of the device.

Use filter circuits for analog supplies. These filter circuits attenuate noise on the power supply at frequencies where analog circuits are most sensitive. The power supply requirements are listed in the following table.

Do not exceed the overall noise ripple values listed in the table. The filter must have adequate noise suppression such that a frequency from 50 kHz to 20 MHz meets the maximum allowable noise swing as described in the table. Select the DCR of the ferrite bead to minimize the voltage drop associated with the filter circuit.

Consider the voltage drop due to any filter components such that the voltage specification (as measured at the device pins) is not exceeded. This consideration implies that the power supply provided by the system must be rated better than the tolerance specified in the data sheet (56070-DS1xx) to compensate for the voltage drop across any filter circuit. Ensure that the current rating of the ferrite bead is at least twice the expected current for the supply.

Table 2: Power Supply

Pin Name	Nominal Voltage	Comments
Analog Power		
AVDD_1P8 AVDD_1P8_1	1.8V	Temperature monitor block power supply. Filter required. OTPC block. Noise < 10 mVp-p, 50 kHz to 20 MHz.
AVS_VTMON_VDDV1P8	1.8V	AVS VT monitor voltage. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
BSPLL[1:0]_AVDD1P8	1.8V	BroadSync PLL0 voltage. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
CORE_PLL_VDD1P8	1.8V	Core PLL voltage. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
GEN_PLL_VDD1P8	1.8V	iProc PLL power. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
LCPLL0_AVDD1P8	1.8V	LCPLL0 voltage. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
PCIE_PVDD_0P8	0.8V	PCIe PLL voltage. Filter required. Noise < 30 mVp-p, 50 kHz to 20 MHz.
PCIE_RTVDD_0P8	0.8V	PCIe transmitter and receiver voltage. Filter required. Noise < 30 mVp-p, 50 kHz to 20 MHz.
PGW_PLL_AVDD1P8	1.8V	Packet gateway PLL power. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
RESCAL[1:0]_AVDD0P8	0.8V	TSC calibration resistor power supply. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
TS_PLL_VDD1P8	1.8V	TimeSync PLL voltage. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
TSCF[3:0]_PVDD0P8	0.8V	Falcon PLL voltage. Filter required. Noise < 3 mVp-p, 50 kHz to 20 MHz.

Table 2: Power Supply (Continued)

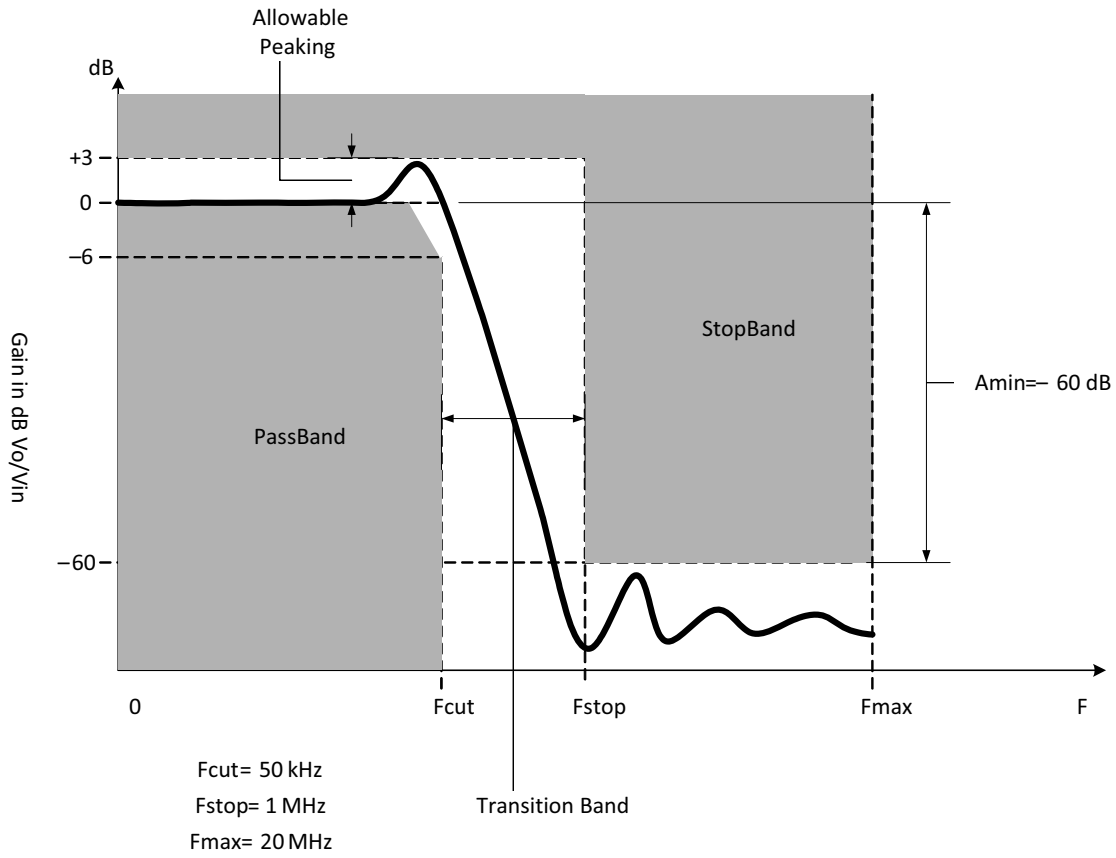
Pin Name	Nominal Voltage	Comments
TSCF_PVDD1P8	1.8V	Falcon PLL voltage. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
TSCF_RTVDD0P8	0.8V	Falcon transmitter/receiver voltage. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
TSCF_TVDD1P2	1.20V	Falcon transmitter voltage. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
TSCQ[2:0]_PVDD_0P8	0.8V	Merlin PLL voltage. Filter required. Noise < 3 mVp-p, 50 kHz to 20 MHz.
TSCQ_RTVDD_0P8	0.8V	Merlin transmitter and receiver voltage. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
XTAL_AVDD1P8	1.8V	XTAL PLL Voltage. Filter required. Noise < 10 mVp-p, 50 kHz to 20 MHz.
Digital Power		
OTPC_VDD1P8	1.8V	OTPC power supply. Filter not required.
VDDC	0.88V	Switch digital core voltage. Filter not required.
VDDO_3P3	3.3V	Digital I/O voltage. Filter not required. Noise < 100 mVp-p.

NOTE: Refer to the BCM56070 data sheet (56070-DS1xx) for detailed electrical requirements.

4.1 Analog Filter Requirements

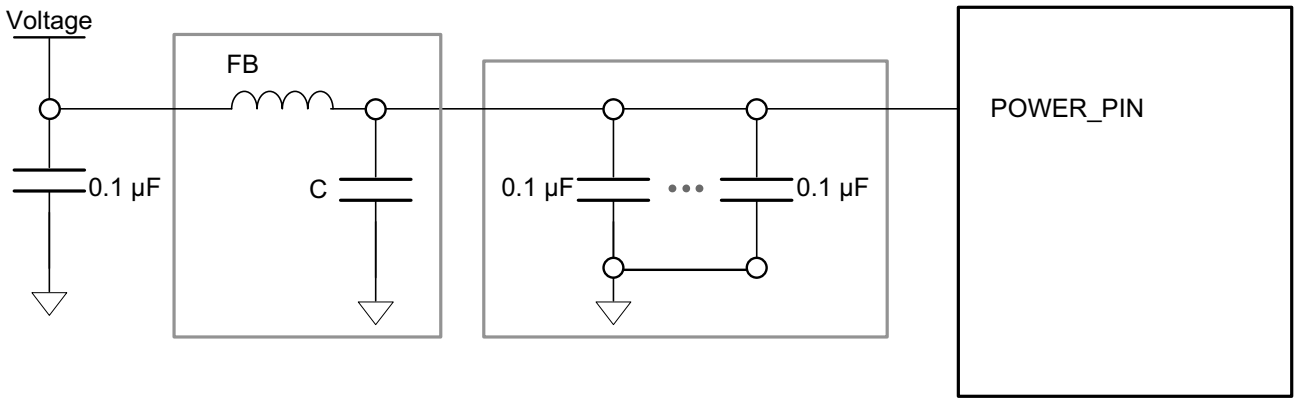
The following figure provides the AC requirements for the low-pass analog power filters along with all the PLL input pins on the device. This specification is designed to cover all of the analog power filters on Falcon and Merlin and all individual PLL filtering requirements using external filter components.

Figure 19: AC Requirements for Analog Power Filters



A reference power supply filter circuit with decoupling capacitors are shown in the following figure.

Figure 20: Power Supply Filter Circuit Diagram



4.1.1 Power Supply Filter Component Examples

The following table lists examples of components that can be used for power-supply filtering.

Table 3: SVK Power Supply Filter Components

Power_Pin Name	Nominal Voltage	Value of Capacitor C	Quantity 0.1 µF Capacitors per Filter Circuit	Ferrite Bead (FB) Example Component	Number of Filter Circuits
AVDD_1P8 AVDD_1P8_1	1.8V	22 µF	2	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	1
AVS_VTMON_VDDV1P8	1.8V	22 µF	1	Vishay ILHB0805ER601V Z = 600Ω, DCR = 100 mΩ, i = 2.0A, 0805	1
BSPLL[1:0]_AVDD1P8	1.8V	22 µF	2	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	2
CORE_PLL_VDD1P8	1.8V	22 µF	2	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	1
GEN_PLL_VDD1P8	1.8V	22 µF	2	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	1
LCPLL0_AVDD1P8	1.8V	22 µF	2	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	1
PCIE_PVDD_0P8	0.8V	22 µF	2	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	1
PCIE_RTVDD_0P8	0.8V	22 µF	2	TDK MPZ2012S101AT Z = 100Ω, DCR = 20 mΩ, i = 4.0A, 0805	1
PGW_PLL_AVDD1P8	1.8V	22 µF	1	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	1
RESCAL[1:0]_AVDD0P8	0.8V	22 µF	2	TDK MMZ1608R601AT Z = 600Ω, DCR = 400 mΩ, i = 500 mA, 0603	1
TSCF[3:0]_PVDD0P8	0.8V	47 µF	1	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	4
TSCF_PVDD1P8	1.8V	47 µF	4	TDK MMZ1608R601AT Z = 600Ω, DCR = 400 mΩ, i = 500 mA, 0603	1
TSCF_RTVDD0P8	0.8V	100 µF	5	Murata BLE32PN300SN1L Z = 30Ω, DCR = 1.6 mΩ, i = 10.0A, 1210	4[a]
TSCF_TVDD1P2	1.2V	47 µF	4	TDK MPZ2012S101AT Z = 100Ω, DCR = 20 mΩ, i = 4.0A, 0805	1
TSCQ[2:0]_PVDD_0P8	0.8V	47 µF	1	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	3
TSCQ_RTVDD_0P8	0.8V	47 µF	4	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	3[b]
TS_PLL_VDD1P8	1.8V	22 µF	2	TDK MMZ1608R601AT Z = 600Ω, DCR = 400 mΩ, i = 500 mA, 0603	1
XTAL_AVDD1P8	1.8V	22 µF	1	TDK MPZ2012S331AT Z = 330Ω, DCR = 50 mΩ, i = 2.5A, 0805	1

a. The four filters are connected in parallel to all 20 pins.

b. The three filters are connected in parallel to all 12 pins.

Chapter 5: Power Supply Information

Refer to the BCM56070 data sheet (56070-DS1xx) for power-up and power-down sequences.

5.1 Fail-Safe I/O Requirements

Refer to the BCM56070 data sheet (56070-DS1xx) for sequencing requirements for non-failsafe I/O signals.

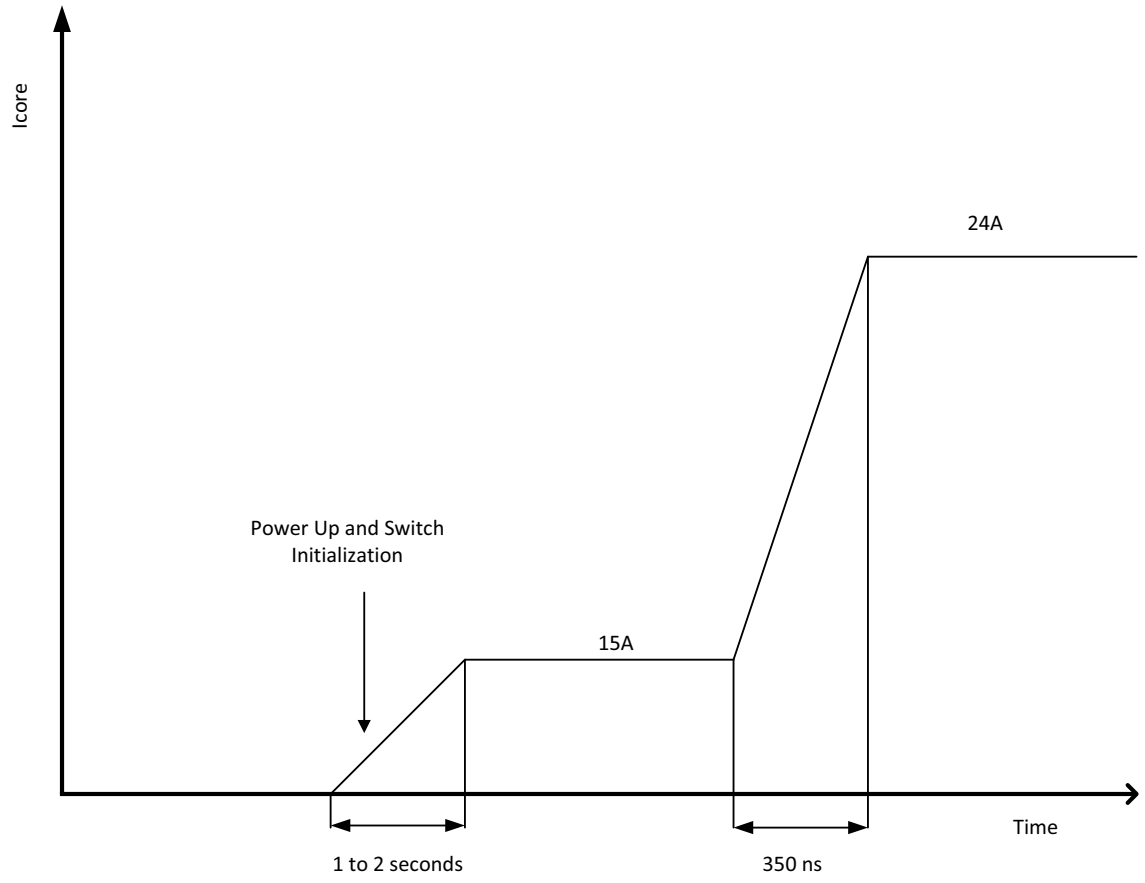
5.2 System Reset

Refer to the BCM56070 data sheet (56070-DS1xx) for power sequencing information, including system reset timing requirements.

5.3 Current Step

The following figure shows the expected transient current versus time. The worst-case condition may occur when the device has completed initialization with all features enabled and with all ports receiving maximum traffic at the same time. In this scenario, the worst-case condition for transient current is 9A over 350 ns.

Figure 21: Expected Transient Current versus Time



Chapter 6: Debug and Bring-up Recommendations

Make certain that signals accessible in the design help with system bring up and lab debug. The following table provides a list of signals that may be useful if you experience bring-up problems and require debugging.

Table 4: Signals for Debug

Pin Name	Purpose
MHOST[1:0]_BOOT_DEV BOOT_DEV[2:0]	Allows the Arm boot process to be modified.
IP_QSPI_*	Allows the QSPI operating mode to be configured.
PCIE_FORCE_GEN[1:0]	Allows the PCIe mode to be changed.
I2C[1:0]_SDA I2C[1:0]_SCL I2C2_SA[1:0]	Allows low-level access to PCIe and iProc subsystems[a].
GPIO[15:0]	Exposes one GPIO, which may allow status to be output.
JTAG*	Allows for production testing and lab debug.
TSCF_TEST[3:0] TSCQ_TEST[2:0]	Exposes one differential pair for each core type. This may allow direct visibility into PLL jitter in Falcon and Merlin cores.

a. Only members of the Broadcom Applications Engineering team should access these subsystems.

Chapter 7: PCB Layout Guidelines

The following sections provide guidance for routing the high-speed SerDes signals on a PCB. Validate any routing scheme through IBIS-AMI simulations.

7.1 25G PCB Layout Guidelines

This section describes the general PCB layout guidelines for Falcon applications for speeds up to 25 Gb/s. For any additional PCB instructions, see Chapter 2, High-Speed SerDes Cores.

High-speed signal routing techniques are necessary when planning system layout and trace routing. The guidelines and recommendations are as follows:

- Use a PCB substrate of Megtron6 or equivalent material.
- Select a PCB glass to minimize the effects of the fiber weave, such as 3313.
- Use hyper very low profile (HVLP) copper profile.
- Route high-speed signals as strip line.
- Ensure that the maximum intra-pair signal length mismatch is 2 mils.
- Ensure that the Falcon SerDes differential impedance target impedance is 95Ω ± 10%.
- Determine trace width and intra-pair spacing by the impedance target and board stack-up.
- Use wider traces to reduce copper loss but should be < 10 mils.
- Optimize all signal via (pad, antipad) dimensions for 95Ω impedance through simulation.
- Include the GND stitching vias in the simulation.
- Use a 3D electromagnetic simulation tool, such as HFSS.
- Vias for different layer transitions require separate optimization (in other words, vias for L1 to L4 transition may be different than vias for L1 to L18 transition).
- Use blind vias, which have no via stubs.
- Remove via stubs by back-drilling. The remaining stub must be less than 6 mils. Include the worst-case via stub length in the AMI simulation.
- Ensure that the package ball grid array (BGA) pads, connector surface-mount technology (SMT) pads, and AC-coupling capacitors have a cutout in the GND reference plane, immediately under the component. Determine the depth and dimension of the cutout by simulation to achieve optimal performance.
- Reference all differential signals to a GND plane.
- Stitch all GND islands along differential pairs with a maximum spacing of 40 mils.
- Do not overlap digital VDD and PVDD on adjacent PCB layers.
- Ensure that digital VDD and PVDD on the same PCB layer have a minimum spacing of five times the PCB dielectric layer thickness.
- Use high-performance connectors that are certified for 25G.
- Keep the trace breakout length as short as possible to minimize impedance discontinuities.
- Route traces with 50Ω geometries in break-out areas where traces are not tightly coupled.
- Avoid sharp bends in the trace routing; instead, use radius bend segments.
- Use larger inter-pair spacing to reduce crosstalk. Use a minimum of four times the trace-width spacing.
- If guard trace or ground patch is used between signal pairs, it must be stitched to GND. Ensure the distance between stitching vias is less than 40 mils.
- Use a solid GND reference plane for signal traces. Splits or voids in the (GND) plane area under or above the signal trace are not allowed. Ensure that the edge of a split or void in the reference plane is at least three times the signal trace width from the signal trace.

- Match the differential pair per segment close to the location of mismatch.
- To minimize the coupling between serpentine legs, ensure that the spacing between serpentine legs is at least five times the trace width.
- Minimize the number of vias (layer transitions) in the signal path.
- Ensure that the number of vias within each leg of a differential pair is the same. In addition, ensure the via placement across the differential pair is symmetric.
- Use stitching vias at layer transitions.
- When placing series AC-coupling capacitors, maintain sufficient lane-to-lane spacing. Ensure that their placement in relation to those for an adjacent lane is not so close as to enable coupling between lanes. Determine the exact spacing through simulation.
- Simulate the full channel with a SerDes AMI model to validate the system performance for both 10G and 25G.
- Use an appropriate simulation tool, such as Agilent ADS. CSP LinkEye® is not available for this SerDes core.
- In ADS simulation, a 15-mV/15-ps (HeightAtBER/WidthAtBER) margin is required for 10G, and a 15-mV/6-ps (HeightAtBER/WidthAtBER) margin is required for 25G.

7.2 10G PCB Layout Guidelines

This section describes the general PCB layout guidelines for the SerDes core when operating up to 10 Gb/s. Refer to the specific SerDes configurations for any additional PCB instructions. High-speed signal routing techniques are necessary when planning system layout and trace routing.

The guidelines and recommendations are as follows:

- Route the PCB trace as a closely coupled differential pair (stripline or microstrip).
- Ensure that the PCB trace impedance has a nominal differential impedance of 95Ω ± 10%
- For noise immunity, common mode noise, and current return path reasons, reference the high-speed signal traces to the ground plane (if possible) for controlled characteristic impedance. At a minimum, use the same reference plane along the entire length of the trace path. Minimize the number of vias and avoid any discontinuities in the reference plane.
- Check trace width and intra-pair spacing in the impedance target and board stackup. Wider traces are preferred to reduce loss, but widths greater than 8 mils are not recommended.
- Use a narrow differential trace width or spacing to escape the ball field, and keep them as short as possible.
- Avoid tight bends.
- Maximize inter-pair spacing to reduce crosstalk. Use at least four times the trace width spacing.
- Use a solid or continuous reference plane (GND) for signal traces. Avoid splits or voids in the reference plane.
- Use blind or back-drilled vias (or both) to remove the via stubs. At high data rates, via stubs can adversely impact the return loss (RL).
- Minimize the number of vias in the high-speed path. Within the differential pair, use the same number of vias on the positive and negative signal traces with symmetrical via placement on the positive and negative signal trace.
- Use stitching vias for signal layer transitions.
- Minimize intra-differential pair length mismatch. The length mismatch target between positive and negative signal is 4 mils (for SFI). Match differential pairs per segment. Match near mismatches.
- Avoid overlapping VDD and GND islands and planes of different domains.
- Use guard trace to reduce crosstalk if board space is available. Connect guard trace to the ground plane through stitching vias. The distance between stitching vias must not be larger than 100 mils.
- When placing series AC-coupling capacitors, maintain sufficient lane-to-lane spacing. Their placement in relation to those for an adjacent lane must not be so close as to enable coupling between lanes. Determine the exact spacing through simulation. Proper spacing can be achieved by staggering capacitor placement.

7.3 PCIe PCB Layout Guidelines

The PCIe PCB layout guidelines are as follows:

- Ensure that all differential signals have a single-ended trace impedance of 50Ω and a differential impedance of 100Ω.
- Match the trace lengths of each differential pair within 5 mils (0.005 in.).
- Do not put 50Ω termination resistors at the receiver inputs PCIE_RXDP and PCIE_RXDN. The PCIe core has integrated 50Ω termination resistors.
- Each TXDP signal must implement an on-board AC-coupling capacitor. Comply with the requirement of 75 nF to 200 nF, as stated in the *PCI Express Base Specification Revision 1.0a*, Section 4.3.3, Table 4-5.
- The PCI Express Base Specification Revision 1.0a, Section 4.3.1.2, dictates AC coupling be placed as close to the transmitter as practical. This placement ensures that the DC bias levels of the transmitted signal do not adversely affect the receiver.
- Keep vias to a minimum because a single via can contribute up to 1.0 dB of loss to the overall loss budget, as specified in the *PCI Express Base Specification Revision 1.0a*, Section 4.3.2.1. Vias must always match in number on each differential pair.
- Vias must not have pads on unused layers when the differential signal must transition between layers of the PCB. The technique of removing all pads from unused layers helps prevent loss or helps reduce impedance discontinuities.

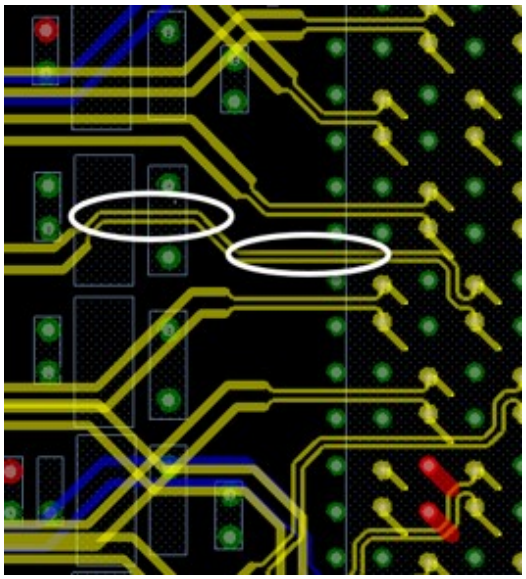
7.4 Escaping the Pad Field

For an example of the high-speed SerDes signals escaping the pad field, refer to the Allegro layout file for the SVK.

7.4.1 Minimize Neck-Down Length

Optimize neck-down lengths to have minimum trace length in the ball field. See the following figure for an example of excessive neck-down length.

Figure 22: Excessive Neck-Down Length



Chapter 8: Reference Clock Layout Guidelines

Take care when laying out the high-speed differential clocks for the device. Of critical importance is the LCPLL0_FREF differential pair, which clocks the Falcon and Merlin SerDes cores. Jitter on these reference clocks can significantly degrade the SerDes performance. Treat these clock nets as high-speed differential signals. As such, route these clocks as shielded differential pairs on an interior layer of the board. Additionally, back-drill all vias associated with these clocks to minimize reflections.

Chapter 9: HiGig Channel Requirements

The HiGig™ (HG) channel requirements are similar to the IEEE-complaint channel requirements. For example, if the HiGig interface is operating at HG[40] or HG[42] over a backplane, its channel requirement will be IEEE 40G-KR4 channel specification.

Chapter 10: Guidelines for Unused Pins

This section provides guidance for the proper termination of any unused device pins.

The following table provides the recommended connectivity for interfaces on the device that are not used.

Table 5: Unused Pin Connection

Unused Interface	Connection
IP_BSC_SCL/SDA	NC
LED	NC
IP_BS*_CLK	NC
IP_BS*_HB	NC
IP_BS*_TC	NC
L1_RCVRD_CLK	NC
L1_RCVRD_CLK_VALID	NC
L1_RCVRD_CLK_BKUP	NC
L1_RCVRD_CLK_BKUP_VALID	NC
IP_UART*_CTS_N	NC
IP_UART*_SIN	NC
IP_UART*_RTS	NC
IP_UART*_SOUT	NC
IP_MDC*	NC
IP_MDIO*	NC

10.1 Unused PCIe Pins

If some lanes of the PCIe interface are not used, leave the pins floating for RX or TX. The RX inputs use an internal 50Ω to ground, and the TX outputs have an internal 50Ω to VDD. Provide all the PCIe_RTVDD and PCIe_PVDD supplies to their specified voltage levels with the power supply.

10.2 Unused TSC Pins

All Falcon and Merlin cores must be powered, even if they are not used. All RVDD, TVDD, PVDD, and (TSC) VDD supplies must be provided to their specified voltage levels with the recommended power supply filtering. The unused RDP/N receiver input pins can be connected to GND, and the TDP/N transmitter output pins can be left NC.

Table 6: Unused TSC4-x Connection

Signal Name	Unused Connection
Receiver	
TSCQ_RDP[3:0]	GND
TSCQ_RDN[3:0]	GND
TSCF_RDP[3:0]	GND
TSCF_RDN[3:0]	GND
Transmitter	
TSCQ_TDP[3:0]	NC
TSCQ_TDN[3:0]	NC
TSCF_TDP[3:0]	NC
TSCF_TDN[3:0]	NC

Chapter 11: Falcon and Merlin Modeling and Simulations

For high-speed SerDes, such as Falcon and Merlin, use simulations to validate the system design and to provide performance estimations in the form of bit error rate (BER).

Include the worst-case channel simulations, and perform a detailed analysis of the system. Extract or include through-channel and crosstalk models for any mated connectors in the path.

11.1 Falcon and Merlin IBIS-AMI Models

The Falcon and Merlin IBIS-AMI models are available on the Broadcom Customer Support Portal (docSAFE) and include the following components:

- TX path:
  - Analog front end (AFE), modeled by a separate S-parameter.
  - TX pre-emphasis equalizer.
- RX path:
  - AFE, modeled by a separate S-parameter.
  - RX equalizer (peaking filter [PF], variable-gain amplifier [VGA], and decision-feedback equalizer [DFE]).

11.1.1 Device Package Model

Worst-case crosstalk and worst-insertion loss Falcon and Merlin SerDes models are available on docSAFE.

Chapter 12: EMI Considerations

For information on PCB stack-up selection, return current path continuity, and decoupling (low-inductance capacitor layout), refer to the *Design Recommendations for Best Performance, Guidelines for PCB Stackups, Layout, and Magnetics Selection* (EMC-AN1xx) and *Selected Methods for Low-Noise Printed Circuit Board Design* (EMC-TI1xx).

NOTE: Pins that are output, such as out-of-band flow control (OOBFC) or SyncE (RCVRD_CLK), must be terminated if they are not used.

Chapter 13: Heat Sink Selection and Attachment

13.1 Heat Sink Selection

In most applications, the BCM56070 device package requires a heat sink. The end-use thermal environment combined with the operating mode of the device dictates the required thermal characteristics (such as the size or thermal resistance) of the heat sink.

13.2 Heat Sink Attachment

The heat sink used with any device in the BCM56070 family must be mechanically mounted to the device. An adhesive-based or taped-based attachment scheme is not allowed. In a mechanically mounted configuration, contact between the heat sink and the package is maintained using an externally applied mechanical force. For best results, ensure that the heat sink is held in place by a clamp or fixture to the printed circuit board. The heat sink must not be clamped to the package (the package and heat sink combination must not be free-standing).

Use a non-adhesive thermal-interface material (that is, phase-change film or thermal grease) between the heat sink and the package top to maintain a low thermal resistance path between them. The applied operating force between the heat sink and the package should be sufficient to meet the thermal interface material manufacturer's recommendations.

The exact configuration of the mounting scheme and clamping mechanism is at the user's discretion, but consider the following:

- For the 25-mm package, a maximum-allowed force during heat sink attachment at room temperature is 47.4 lbf/21.5 kgf for maximum of 30 seconds.
- For the 25-mm package, a maximum-allowed sustained force during the device’s lifespan is 12.6 lbf/5.7 kgf.
- The applied operating force should be evenly distributed across the package top.
- Select tooling holes and clamp locations to minimize PCB warping.
- The clamping mechanism must not clamp to the package underside.
- The clamping structure must withstand the user's mechanical testing requirements, such as shock and vibration.
- To distribute the force uniformly, place a thermal pad between the external heat sink and the bare die.
- To avoid concentrated force on the exposed die, use a heat sink with a grooved base plate design.

NOTE: When attaching the heat sink, apply uniform force to the device surface. Concentrated force on the device surface can cause die or package damage. For optimized force, perform a heat sink assembly evaluation test, and reference the heat sink and thermal interface supplier's requirement.

Related Documents

The references in this section may be used with this document.

NOTE: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads and Support site.

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Data Sheet (Low-Power 440G Switch with MACsec Encryption)	56070-DS1xx	Broadcom CSP
Theory of Operation	56070-PG2xx	Broadcom CSP
Programmer's Register Reference Guide	BCM56070_A0-PRG*.zip	Broadcom CSP
Packaging Reflow Process Guidelines for Surface Mount Assemblies	PACKAGING-AN1xx	Broadcom CSP
TSC-F 1G Support on TSC-FalconCore	TSC-F-AN1xx	Broadcom CSP

Glossary

The following table lists the acronyms and abbreviations used in this document.

Table 7: Acronyms and Abbreviations

Acronym/Abbreviation	Description
AN	Auto-negotiation
ASPM	Active-state power management
BGA	Ball grid array
DCR	DC resistance
EEPROM	Electrically erasable programmable read-only memory
EMI	Electromagnetic interference
EP	Egress processor
ESD	Electrostatic discharge
HG	HiGig
HVLP	Hyper very low profile
I/O	Input/output
IP	Ingress processor
MMU	Memory management unit
OCXO	Oven-controlled crystal oscillator
OOBFC	Out-of-band flow control
OSx	Oversample
OTP	One-time programmable
PCB	Printed circuit board
PCIe	Peripheral component interconnect express
PLL	Phase locked loop
QSPI	Quad Serial Peripheral Interface
RF	Radio frequency
RX	Receive
SFI	SerDes Framer Interface
SMT	Surface-mount technology
SerDes	Serializer/deserializer
SyncE	Synchronous Ethernet
TDM	Time division multiplexing
TS	TimeSync
TSC	TDM-based SerDes Controller
TSC4-FC	Falcon SerDes core
TSC4-MC	Merlin SerDes core
TSC4-x	Falcon or Merlin SerDes core (or both)
ToP	Timing-over-Packet
USXGMII	Universal serial 10GbE media independent interface
VCO	Voltage-controlled oscillator