

AFBR-5972EZ

Compact 650-nm Transceiver with Compact Versatile-Link Connector for Fast Ethernet and up to 250 Mbaud over POF

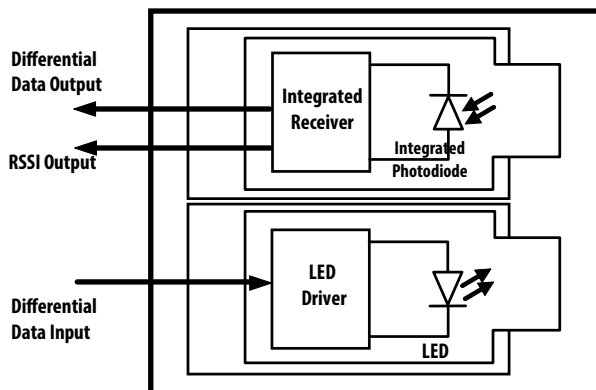


Description

The Broadcom® AFBR-5972EZ transceiver provides the system designer with the ability to implement Fast Ethernet (100 Mb/s) over standard bandwidth 0.5 ± 0.05 NA POF. This transceiver features a compact Versatile-Link duplex connector that is compatible with existing Versatile-Link simplex connectors, and it features a very compact design with a form factor similar to a UTP connector.

The AFBR-5972EZ transceiver is lead-free and compliant with RoHS.

Figure 1: Block Diagram



Features

- Fast Ethernet communications over POF
- Link lengths up to 50m POF (NA 0.5) or 70m POF (NA 0.3)
- Compact footprint
- 3.3V operation
- Data rates up to 250 Mbaud
- LVDS input and output data connections
- Analog RSSI (receiver signal strength) monitor output
- Temperature range -40°C to 85°C

Applications

- Factory automation at Fast Ethernet speeds
- Fast Ethernet networking over POF
- Proprietary communication over POF up to 250 Mbaud

Transmitter

The transmitter contains a 650-nm LED with a driver IC. The LED driver operates at 3.3V. It receives an LVDS electrical input and converts it into a modulated current driving the LED. The IC and LED are packaged in an optical subassembly integrating the transmitter section. The optical subassembly couples the output optical power efficiently into POF fiber.

Receiver

The receiver IC integrates a double photodiode with the amplifier and quantizer function. The IC is packaged in an optical subassembly integrating the receiver section. This optical subassembly couples the optical power efficiently from POF fiber to the receiving photodiode. The integrated IC operates at 3.3V and converts the photocurrent into a LVDS electrical output signal.

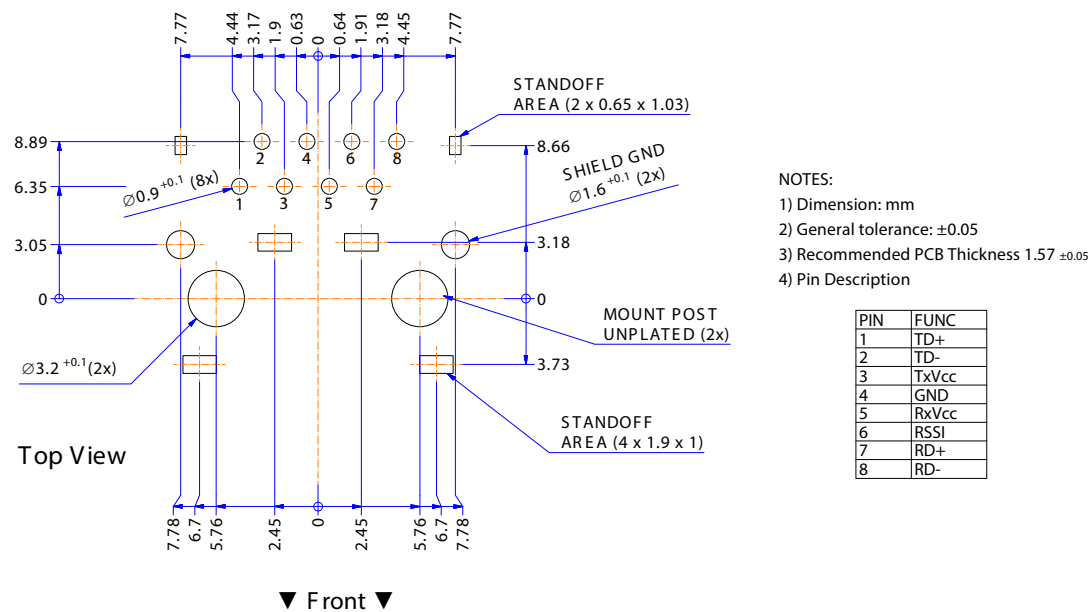
Package

The transceiver package consists of three basic elements: two opto-electrical subassemblies and the housing, as shown in the block diagram in Figure 1. The package outline drawing and pinouts are shown in Figure 2 and Figure 7.

The opto-electrical subassemblies use a high-volume assembly process together with low-cost lens elements that result in a cost-effective building block. They consist of the active III-V devices, IC chips, and various surface-mounted passive components.

There are eight signal pins, four EMI shield solder posts, and two mounting posts, which exit the bottom of the housing. The solder posts are isolated from the internal circuit of the transceiver and are to be connected to chassis ground. The mounting posts are to provide mechanical strength to hold the transceiver to the application board.

Figure 2: PCB Footprint and Pinout Diagram



Pin Descriptions

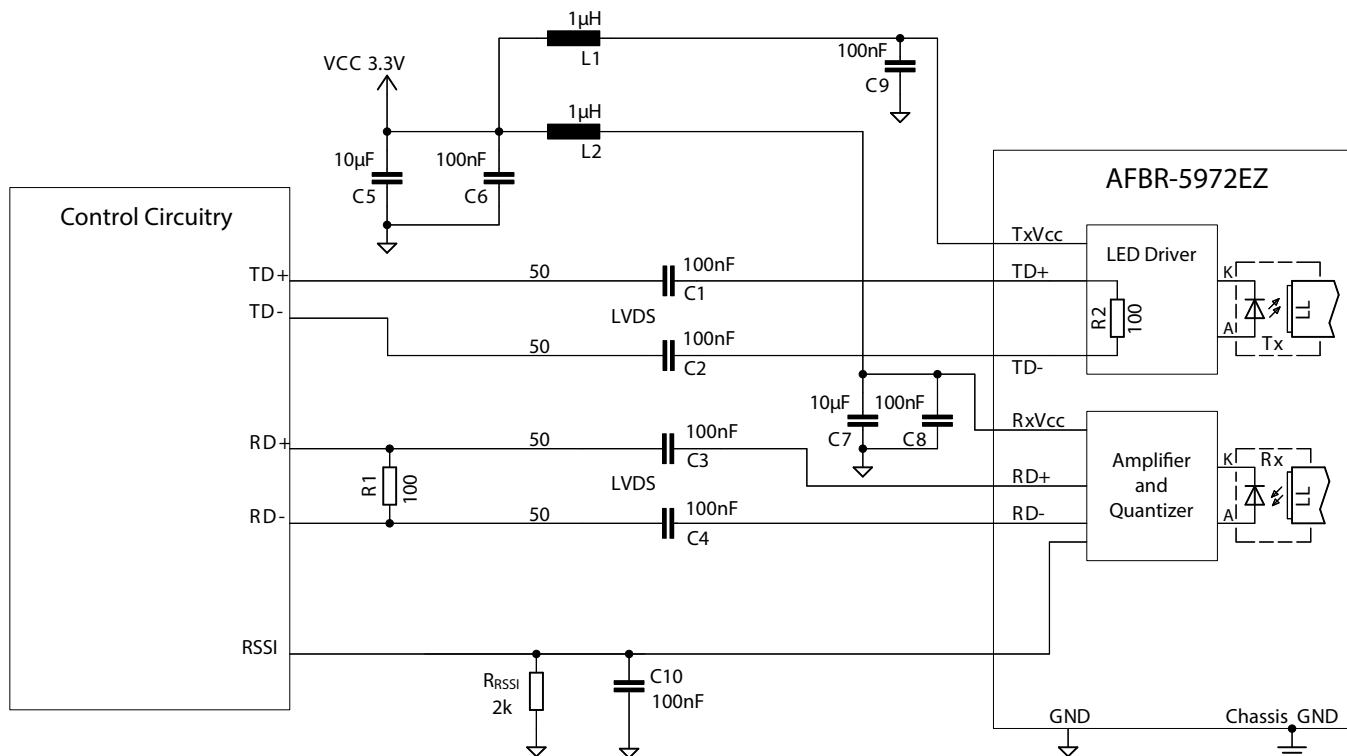
Table 1: Pin Descriptions

Pin Number	Name	Description
1	TDData+	Transmitter data in positive. This input is an LVDS compatible differential line.
2	TDData-	Transmitter data in negative. This input is an LVDS compatible differential line.
3	TxVCC	Transmitter power supply pin. Provides +3.3V DC via a transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the TxVCC pin.
4	GND	Common ground pin. Directly connect this pin to the signal ground plane of the host board.
5	RxVCC	Receiver power supply pin. Provides +3.3V DC via a receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the RxVCC pin.
6	RSSI	Receiver signal strength pin. Delivers a DC output current proportional to the average incoming light power.
7	RData+	Receiver data out positive. This data line is an LVDS-compatible differential output line that should be properly terminated. In absence of an optical input signal, this line is squelched.
8	RData-	Receiver data out negative. This data line is an LVDS-compatible differential output line that should be properly terminated. In absence of an optical input signal, this line (same as RData+) is squelched.
Shield	Shield	This is to be connected to the equipment chassis ground.

Application Circuit

The recommended application circuit is shown in [Figure 3](#).

Figure 3: Recommended Application Circuit



Board Layout – Decoupling Circuit and Ground Planes

The layout of the application circuitry is important to achieve optimum performance of the transceiver. Designers should use the following guidelines:

- Use a power-supply decoupling circuit to filter out noise and ensure optimal product performance.
- Provide a contiguous signal ground plane in the circuit board directly under the transceiver to provide a low-inductance ground for signal return current.
- Connect the shield posts to the chassis ground to provide optimum EMI, ESD, and EMS performance, which is in keeping with good high-frequency board layout practices.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic discharge (ESD) to the electrical pins	ESD22-A114	Withstands up to 2000V HBM applied between the electrical pins.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 15V/m field swept from 80 MHz to 1 GHz applied to the transceiver when mounted on a circuit board without chassis enclosure.
Eye safety	EN 60825-1:52007	Laser class 1 product (LED radiation only). TÜV certificate: R 50483935. CAUTION: Use of controls or adjustments of performance or procedures other than those specified herein can result in hazardous radiation exposure.
Component recognition	Underwriter Laboratories	UL File #: E173874.

Transceiver Diagnostics Timing Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Time to Initialize	t_init	—	5	ms	Note ^a , Figure 4
Assert Time	t_ass	—	100	μs	Note ^{b,c}
Deassert Time	t_deass	—	100	μs	Note ^{c,d}

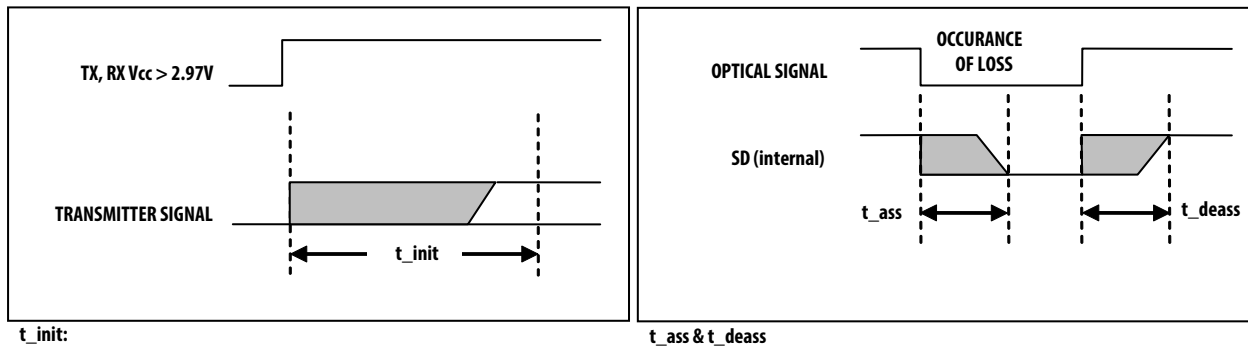
a. Time from power-on to when the modulated optical output rises above 90% of nominal.

b. Time from valid optical signal to assertion.

c. There is an internal signal detect (SD) signal that is directly related to assert (PA) and deassert (PD) levels as specified in [Receiver Optical Characteristics](#). There is no direct access to the SD signal; however, the Rx data outputs will squelch and the RSSI will switch off once the optical input power falls below PD. Furthermore, the Rx data and RSSI outputs will be activated once the optical input power exceeds PA.

d. Time from loss of optical signal to deassertion.

Figure 4: Transceiver Timing Diagrams



Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operation conditions. It should not be assumed that limiting values of more than one parameter can be applied to the products at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+100	°C	—
Case Operating Temperature	T_C	-40	+85	°C	Notes ^{a, b}
Lead Soldering Temperature	T_{sold}	—	260	°C	Note ^c
Lead Soldering Time	t_{sold}	—	10	s	Note ^c
Supply Voltage	V_{CC}	-0.5	4.0	V	—
Data Input Voltage	V_I	-0.5	V_{CC}	V	—

- Operating the product outside the maximum-rated case operating temperature range will compromise its reliability and can damage the product.
- The temperature is measured using a thermocouple connected to the hottest position of the housing.
- The transceiver is Pb-free wave solderable.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Case Operating Temperature	T_C	-40	—	+85	°C	Notes ^{a, b}
Supply Voltage	V_{CC}	2.97	3.30	3.63	V	—
Receiver Output Termination Impedance	R_L	—	100	—	Ω	—
Signaling Rate (Fast Ethernet)	B_{FE}	—	125	—	Mbaud	4B/5B; Note ^c
Signaling Rate (General)	B_G	10	—	250	Mbaud	Note ^d

- The temperature is measured using a thermocouple connected to the housing.
- Electrical and optical specifications of the product are guaranteed across the recommended case operating temperature range only.
- Ethernet autonegotiation pulses are not supported.
- Minimum signaling rate for bi-phase coded signal. Maximum signaling rate for 8B/10B coded signal (verified by the PRBS $2^7 - 1$ test pattern).

Transceiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Current	I_{CC}	—	45	55	mA	—
Power Dissipation	P_{DISS}	—	150	200	mW	—
Power Supply Noise Immunity	PS_{NI}	50	—	—	mV	Peak to peak; Note ^a
Tx Differential Input Voltage (pk-pk)	V_{DII}	200	—	1800	mV	—
Tx Input Voltage Range to Circuit Common	V_I	0	—	2.4	V	—

a. Frequencies from 0.1 MHz to 100 MHz.

Transmitter Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Average Launched Power (1-mm POF; NA = 0.5)	P_{O-POF}	−10	−6.5	−3.0	dBm	Note ^a
Extinction Ratio	EXT	10	—	—	dB	Note ^a
Central Wavelength	λ_C	635	650	675	nm	Notes ^{a, b}
Spectral RMS	$\Delta\lambda$	—	—	17	nm	Notes ^{b, c}
Optical Rise Time (10% to 90%)	t_r	—	1.7	2	ns	Note ^a
Optical Fall Time (90% to 10%)	t_f	—	1.6	2	ns	Note ^a
Duty Cycle Distortion Contributed by the Transmitter	DCD	—	—	1	ns	Peak to peak; Note ^a
Data-Dependent Jitter	J_{DD}	—	—	0.6	ns	Note ^a
Random Jitter Contributed by the Transmitter	J_R	—	—	0.76	ns	Peak to peak; Notes ^{a, d}
Overshoot	OS	—	7	25	%	Note ^a

a. Measured at the end of 1-meter plastic optical fiber with a PRBS 2^7-1 sequence, running at 250 Mbaud data rate.

b. Central wavelength is defined as: (Ref: EIA/TIA standard FOTP-127/6.1, 1991)

$$\lambda_c = \frac{\sum_{i=1}^N P_i \lambda_i}{\sum_{i=1}^N P_i}$$

c. Spectrum RMS is defined as: (Ref: EIA/TIA standard FOTP-127/6.3, 1991)

$$\Delta\lambda = \left[\left(\frac{\sum_{i=1}^N P_i \lambda_i^2}{\sum_{i=1}^N P_i} \right) - \lambda_c^2 \right]^{\frac{1}{2}}$$

d. Based on BER = 2.5×10^{-10} .

Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Differential Output Voltage (pk-pk)	V_{DO}	500	—	900	mV	Note ^a
Output Common Mode Voltage	V_{OCM}	—	1.2	—	V	Note ^a
Data Output Rise Time (10% to 90%)	t_r	—	0.8	1.5	ns	Note ^a
Data Output Fall Time (90% to 10%)	t_f	—	0.8	1.5	ns	Note ^a
Duty Cycle Distortion	DCD	—	—	1.0	ns	Note ^{a, b}
Data Dependent Jitter	J_{DD}	—	—	1.2	ns	Note ^{a, b}
Random Jitter	J_R	—	—	2.14	ns	Peak to peak; Notes ^{a, b, c}
RSSI Output Responsivity	I_{RSSI}/P_{IN}	—	0.55	—	A/W	See Figures 5 and 6.
Voltage at RSSI Output	V_{RSSI}	0	—	$V_{CC} - 1.5$	V	—

a. Characterized with LVDS termination (100Ω).

b. Contributed by Rx only.

c. Based on BER = 2.5×10^{-10} .

Figure 5: Typical RSSI Output Voltage across $R_{RSSI} = 2\text{ k}\Omega$

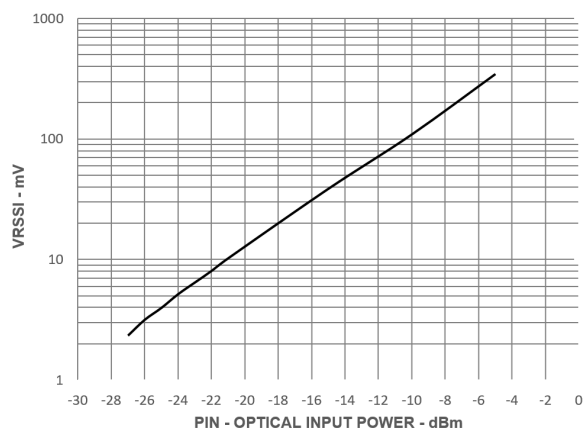
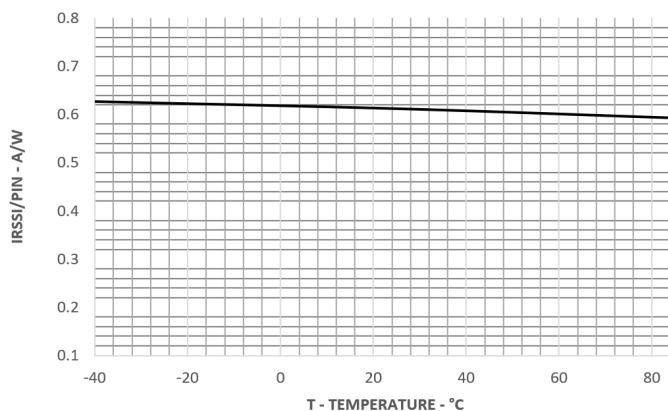


Figure 6: Typical Responsivity vs. Temperature



Receiver Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Unstressed Receiver Sensitivity (POF) for Fast Ethernet Data Rate (125 Mbaud)	CSEN ₁₂₅	-26	—	—	dBm	Note ^a
Unstressed Receiver Sensitivity (POF) for Data Rate 250 Mbaud	CSEN ₂₅₀	-22	—	—	dBm	Note ^b
Input Optical Power Maximum (POF)	P _{IN-MAX}	—	—	-3.0	dBm	Notes ^{a, c}
Operating Wavelength	λ_C	635	650	675	nm	—
Assert Input Power Level	PA	—	-31	—	dBm	Notes ^{d, e}
Deassert Input Power Level	PD	—	-32.5	—	dBm	Notes ^{d, e}
Hysteresis between Assert and Deassert	PA-PD	—	2	—	dB	Note ^e

a. Measured with a PRBS 2⁷-1 sequence at 125 Mbaud. BER < 2.5 × 10⁻¹⁰.

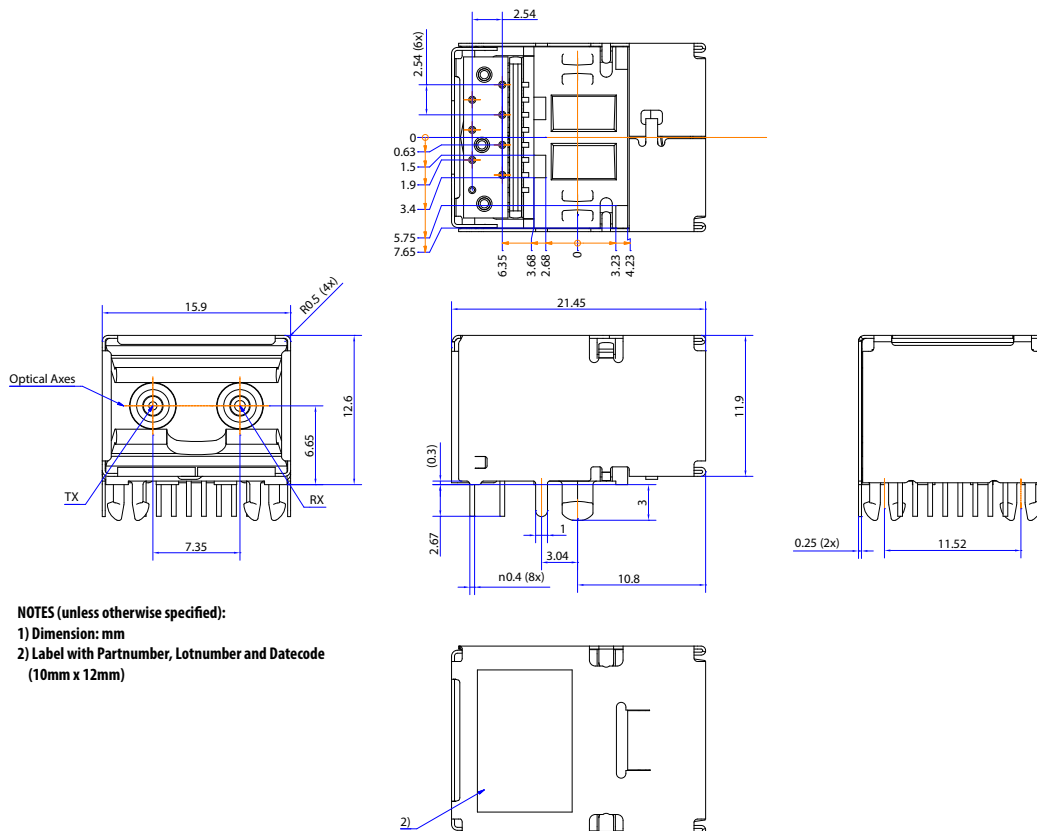
b. Measured with a PRBS 2⁷-1 sequence at 250 Mbaud. BER < 2.5 × 10⁻¹⁰.

c. Input Optical Power Maximum is defined as the maximum optical average amplitude where the receiver duty cycle distortion reaches ±1 ns.

d. Asserted and deasserted levels are indicated as dB below the unstressed receiver sensitivity level for POF.

e. There is an internal signal detect (SD) signal that is directly related to assert (PA) and deassert (PD) levels. There is no direct access to the SD signal; however, the Rx data outputs will squelch and the RSSI will switch off once the optical input power falls below PD. Furthermore, the Rx data and RSSI outputs will be activated once the optical input power exceeds PA.

Figure 7: Package Outline Drawing



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