BROADCOM®

Data Sheet

ACPL-K33T

Automotive 2.5A Peak High-Output Current SiC MOSFET and IGBT Gate Drive Optocoupler with Rail-to-Rail Output Voltage in Stretched SO-8

Description

The Broadcom® 2.5-Amp Automotive R^{2}Coupler™ Gate Drive Optocoupler contains an AlGaAs LED that is optically coupled to an integrated circuit with a power output stage. The ACPL-K33T features a fast propagation delay and tight timing skew and is ideally designed for driving SiC MOSFETs and IGBTs used in AC-DC and DC-DC converters. The high operating voltage range of the output stage provides the drive voltages required by gate-controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct-driving SiC MOSFETs and IGBTs at high frequency for high-efficiency conversion.

Broadcom R^{2}Coupler isolation products provide reinforced insulation and reliability that deliver safe signal isolation that is critical in automotive and high-temperature industrial applications.

Features

- Qualified to AEC-Q100 Grade 1 test guidelines
- Automotive temperature range: –40°C to +125°C
- Peak output current: 2.0A minimum
- Rail-to-rail output voltage
- Propagation delay: 120 ns maximum
- Dead time distortion: +50 ns/–40 ns
- LED input threshold current hysteresis
- Common mode rejection (CMR): 50 kV/µs minimum at V_{CM} = 1500V
- Low supply current allows a bootstrap half-bridge topology: ICC = 4.2 mA maximum
- Under-voltage lockout (UVLO) protection with hysteresis for SiC MOSFETs and IGBTs
- Wide operating V_{CC} range: 15V to 30V
- Safety approvals:
  - UL recognized 5000 V_{RMS} for 1 minute
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1140 V_{peak}

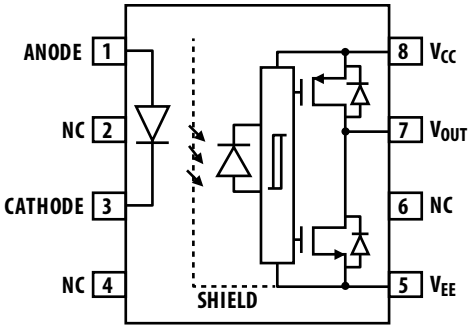
Applications

- Hybrid power train DC/DC converters
- EV/PHEV chargers
- Automotive isolated IGBT gate drives
- AC and brushless DC motor drives

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage and degradation that might be induced by electrostatic discharge (ESD). The component featured in this data sheet is not recommended to be used in military or aerospace applications or environments.

Functional Diagram

Figure 1: ACPL-K33T Functional Diagram



NOTE: A minimum 1-µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Truth Table

LED	$V_{CC} - V_{EE}$	V_{OUT}
OFF	0V – 30V	LOW
ON	< V_{UVLO-}	LOW
ON	> V_{UVLO+}	HIGH

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	UL 5000-V_{RMS}/ 1-Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-K33T	-000E	Stretched SO-8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

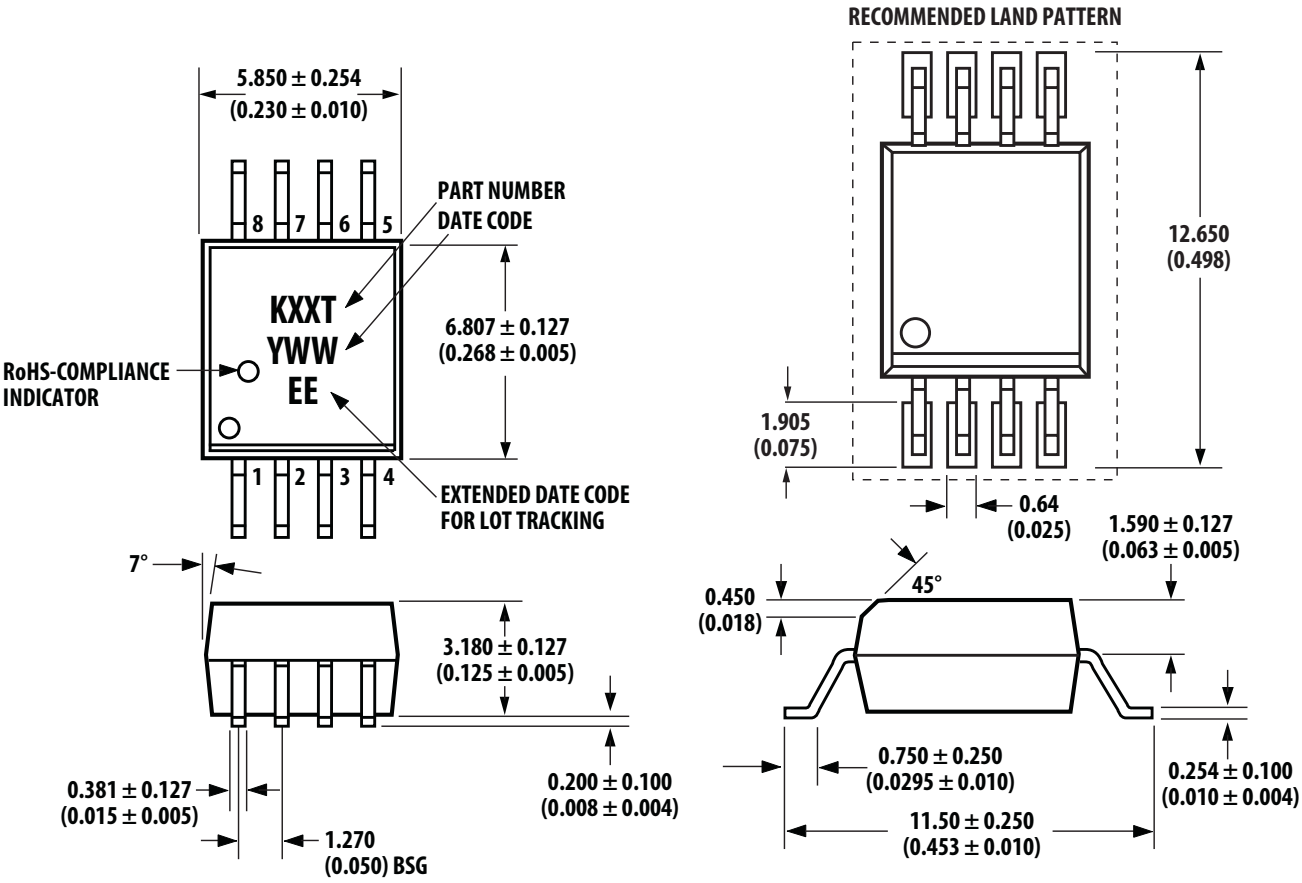
To form an order entry, choose a part number from the Part Number column and combine it with the desired option from the Option column.

Example 1:

Use ACPL-K33T-560E to order the product with an SSO-8 surface-mount package in tape and reel packaging with IEC/EN/DIN EN 60747-5-5 safety approval and RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawings (Stretched SO-8)



Dimensions in millimeters (inches).

Notes:
1. Lead coplanarity = 0.1 mm (0.004 inches).
2. Floating lead protrusion = 0.25 mm (10 mils) max.

Recommended Pb-Free IR Profile

Recommended reflow condition is as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Non-halide flux should be used.

Regulatory Information

The ACPL-K33T is approved by the following organizations.

UL	UL 1577, component recognition program up to V_{ISO} = 5 kV_{RMS}
CSA	CSA Component Acceptance Notice #5
IEC/EN/DIN EN 60747-5-5	IEC/EN/DIN EN 60747-5-5

IEC/EN/DIN EN 60747-5-5 Insulation-Related Characteristics (Option 060 and 560 Only)

Description	Symbol	Option 060 and 560	Units
Installation classification per DIN VDE 0110/1.89, Table 1 For rated mains voltage < 600 V_{RMS} For rated mains voltage < 1000 V_{RMS}	—	 I - IV I - III	—
Climatic Classification[a]	—	40/125/21	—
Pollution Degree (DIN VDE 0110/1.89)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{peak}
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial discharge < 5 pC	V_{PR}	2137	V_{peak}
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test with t_m = 10 seconds, Partial discharge < 5 pC	V_{PR}	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 seconds)	V_{IOTM}	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure Case Temperature Input Current Output Power	 Ts $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_s, V_{IO} = 500V	Rs	> 10^9	Ω

a. Climatic classification denotes <Minimum ambient temperature of operation>/<Maximum ambient temperature of operation>/<Number of days of the damp heat, steady state test>.

Insulation and Safety-Related Specifications

Parameter	Symbol	ACPL-K33T	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8	mm	Measured from input terminals to output terminals, shortest distance through the air.
Minimum External Tracking (Creepage)	L(102)	8	mm	Measured from input terminals to output terminals, shortest distance path along the body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and the detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group (DIN VDE0109)	—	IIIa	—	Material Group (DIN VDE 0109).

Absolute Maximum Ratings

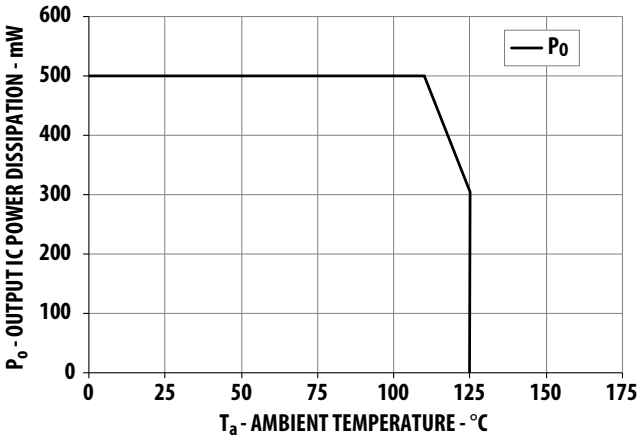
Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	150	°C
Operating Temperature	T_A	–40	125	°C
IC Junction Temperature[a]	T_J	—	150	°C
Average Input Current	$I_{F(AVG)}$	—	20	mA
Peak Input Current (50% duty cycle, < 1 ms pulse width)	$I_{F(PEAK)}$	—	40	mA
Peak Transient Input Current (< 1 µs pulse width, 300 pps)	$I_{F(TRAN)}$	—	1	A
Reverse Input Voltage	V_R	—	6	V
“High” Peak Output Current[b]	$I_{OH(PEAK)}$	—	2.5	A
“Low” Peak Output Current[b]	$I_{OL(PEAK)}$	—	2.5	A
Total Output Supply Voltage	$(V_{CC} – V_{EE})$	0	35	V
Output Voltage	$V_{O(PEAK)}$	–0.5	V_{CC}	V
Output IC Power Dissipation[c]	P_O	—	500	mW
Total Power Dissipation[a]	P_T	—	550	mW

a. The total power dissipation is derated linearly above a 110°C free-air temperature at a rate of 13 mW/°C. The maximum LED and IC junction temperature should not exceed 150°C.

b. The maximum pulse width = 100 ns, duty cycle = 2%.

c. Derate linearly above a 110°C free-air temperature at a rate of 13 mW/°C. See Figure 2.

Figure 2: Output IC Power Dissipation Derating Chart



Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Operating Temperature	T_A	–40	125	°C
Output Supply Voltage	$(V_{CC} – V_{EE})$	15	30	V
Input Current (ON)	$I_{F(ON)}$	7	13	mA
Input Voltage (OFF)	$V_{F(OFF)}$	–5.5	0.8	V

Electrical Specifications (DC)

Unless otherwise noted, all minimum/maximum specifications are at recommended operating conditions. All typical values are at T_A = 25°C, $V_{CC} – V_{EE}$ = 15V, V_{EE} = Ground.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure
High Level Peak Output Current	I_{OH}	—	–3.5	–2.0	A	$V_{CC} – V_O$ = 15V	3
Low Level Peak Output Current	I_{OL}	2.0	4	—	A	$V_O – V_{EE}$ = 15V	4
High Output Transistor RDS(ON)[a]	$R_{DS,OH}$	—	2.2	4.0	Ω	I_{OH} = –2.0A	
Low Output Transistor RDS(ON)[a]	$R_{DS,OL}$	—	1.0	2.0	Ω	I_{OL} = 2.0A	
High Level Output Voltage[b, c]	V_{OH}	V_{CC} – 0.45	V_{CC} – 0.2	—	V	I_F = 10 mA I_O = –100 mA	
Low Level Output Voltage	V_{OL}	—	0.1	0.25	V	I_O = 100 mA	
High Level Supply Current	I_{CCH}	—	2.65	4.2	mA	I_F = 10 mA	5
Low Level Supply Current	I_{CCL}	—	2.55	4.2	mA	V_F = 0V	6
Threshold Input Current Low to High	I_{FLH}	—	2.6	5.5	mA	V_O > 5V	7
Threshold Input Voltage High to Low	V_{FHL}	0.8	—	—	V		
Input Forward Voltage	V_F	1.25	1.5	1.85	V	I_F = 10 mA	7
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.5	—	mV/°C		
Input Reverse Breakdown Voltage	BV_R	6	—	—	V	I_R = 100 µA	
Input Capacitance	C_{IN}	—	90	—	pF	f = 1 MHz V_F = 0V	
UVLO Threshold	V_{UVLO+}	12.1	13	13.9	V	V_O > 5V I_F = 10 mA	8
	V_{UVLO-}	11.1	12	12.9			8
UVLO Hysteresis	$UVLO_{HYS}$	0.5	1.0	—	V	—	

a. The output is sourced at –2.0A or 2.0A with a maximum pulse width of 10 µs.

b. In this test, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero amperes.

c. The maximum pulse width = 1 ms.

Switching Specifications (AC)

Unless otherwise noted, all minimum/maximum specifications are at recommended operating conditions. All typical values are at T_A = 25°C, $V_{CC} – V_{EE}$ = 15V, V_{EE} = Ground.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure
Propagation Delay Time to High Output Level[a]	t_{PLH}	30	65	120	ns	V_{CC} = 15V R_G = 7.5Ω C_L = 10 nF f = 20 kH Duty Cycle = 50% V_{in} = 4.5V to 5.5V R_{in} = 350Ω	9, 12, 14
Propagation Delay Time to Low Output Level	t_{PHL}	30	65	120	ns		10, 12, 14
Pulse Width Distortion ($t_{PHL} – t_{PLH}$)[b]	PWD	–40	0	40	ns		11
Dead Time Distortion Caused by Any Two Parts ($t_{PLH} – t_{PHL}$)[c]	DTD	–40	—	50	ns		
Rise Time	t_R	—	15	—	ns	V_{CC} = 15V C_L = 1 nF f = 20 kHz Duty Cycle = 50% V_{in} = 4.5V to 5.5V R_{in} = 350Ω	13, 14
Fall Time	t_F	—	15	—	ns		
Output High Level Common Mode Transient Immunity[d, e]	$\|CM_H\|$	50	>75	—	kV/µs	T_A = 25°C V_{CC} = 30V V_{CM} = 1500V with split resistors	15
Output Low Level Common Mode Transient Immunity[d, f]	$\|CM_L\|$	50	>75	—	kV/µs		

a. This load condition approximates the gate load of 600V/50A power devices.

b. Pulse width distortion (PWD) is defined as $t_{PHL} – t_{PLH}$ for any given device.

c. Dead time distortion (DTD) is defined as $t_{PLH} – t_{PHL}$ between any two parts under the same test condition. A negative DTD reduces the original system dead time; whereas a positive DTD increases the original system dead time.

d. Pin 2 and Pin 4 must be connected to LED common.

e. Common mode transient immunity in a high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output remains in the high state, (V_O > 15V).

f. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output remains in the low state (V_O < 1.0V).

Package Characteristics

Unless otherwise noted, all minimum/maximum specifications are at recommended operating conditions. All typical values are at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage[a, b, c]	V_{ISO}	5000	—	—	V_{RMS}	RH < 50%, t = 1 minute T_A = 25°C
Input-Output Resistance[c]	R_{I-O}	109	1014	—	Ω	V_{I-O} = 500 V_{DC}
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz

a. The input-output momentary withstand voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.

b. In accordance with UL1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second.

c. The device is considered a two-terminal device: pins 1, 2, 3, and 4 are shorted together, and pins 5, 6, 7, and 8 are shorted together.

Typical Performance Plots

Figure 3: I_{OH} vs. (V_{CC} –V_{OH})

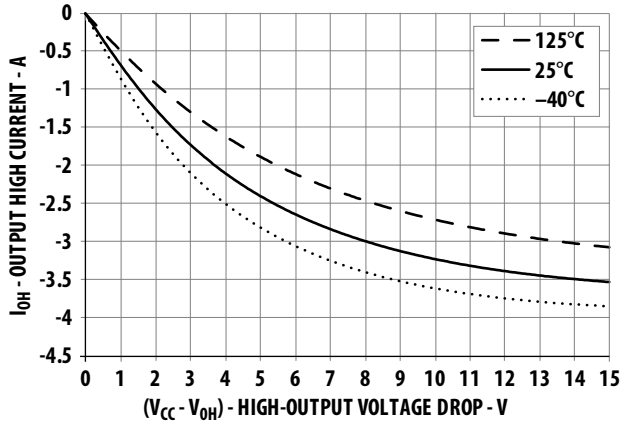


Figure 4: I_{OL} vs. V_{OL}

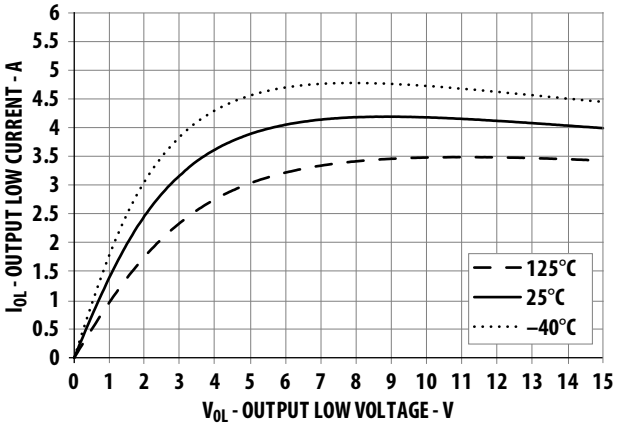


Figure 5: I_{CCH} vs. Temperature

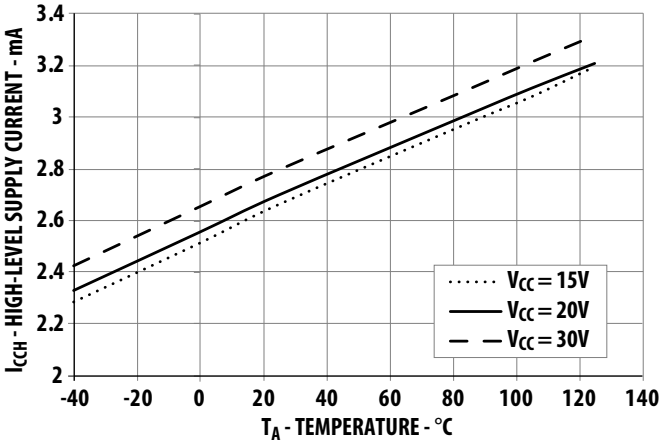


Figure 6: I_{CCL} vs. Temperature

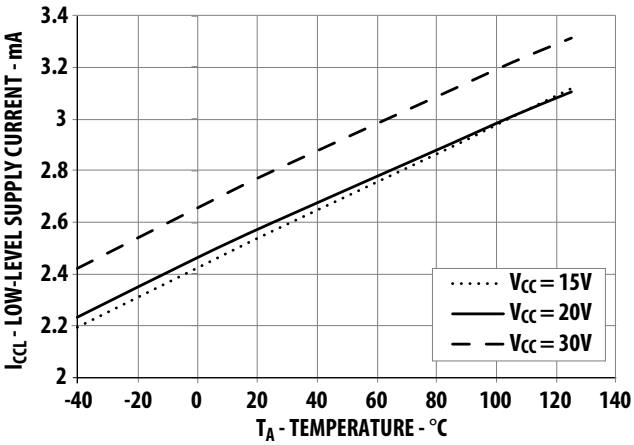


Figure 7: V_F vs. Temperature

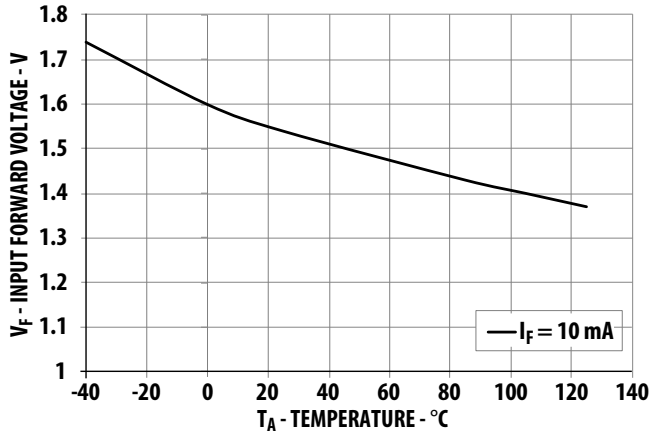


Figure 8: I_F vs. V_F

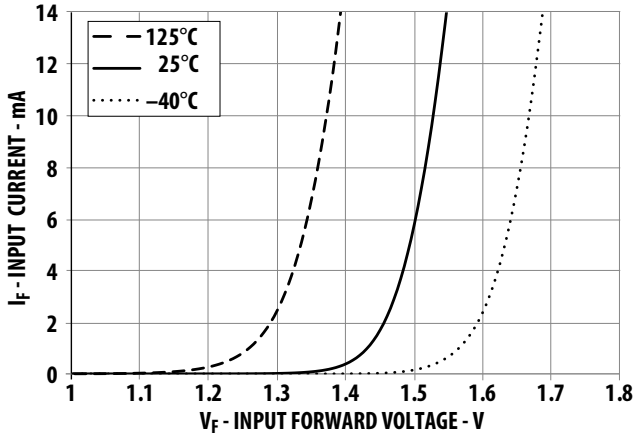


Figure 9: t_{PLH} vs. Temperature

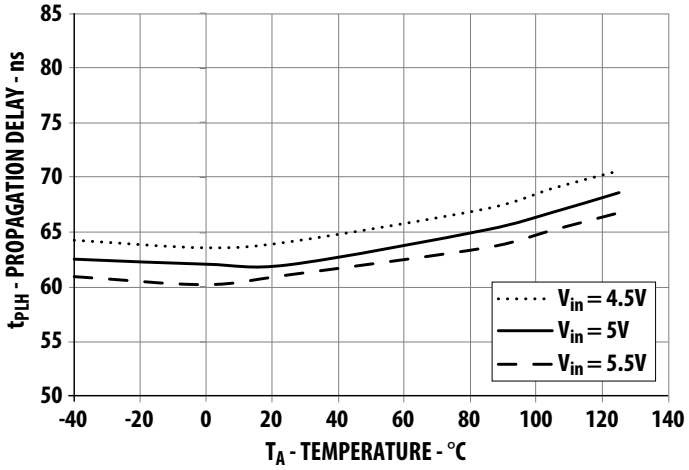


Figure 10: t_{PHL} vs. Temperature

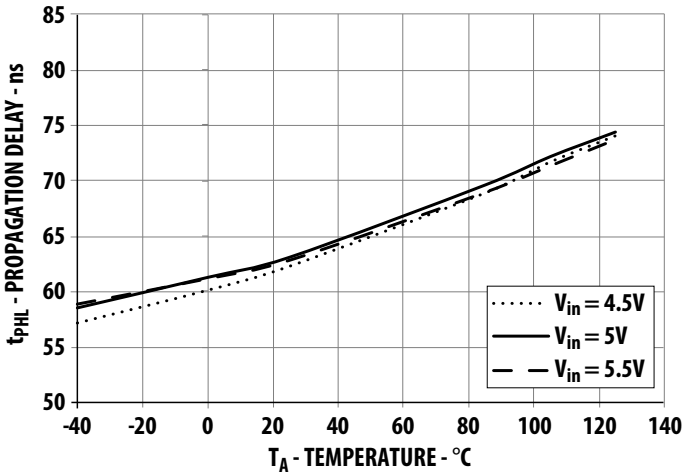


Figure 11: PWD vs. Temperature

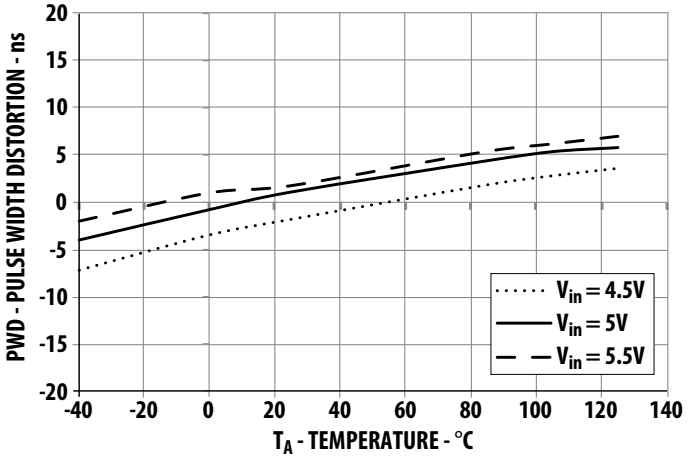


Figure 12: t_{PLH} and t_{PHL} Test Circuit

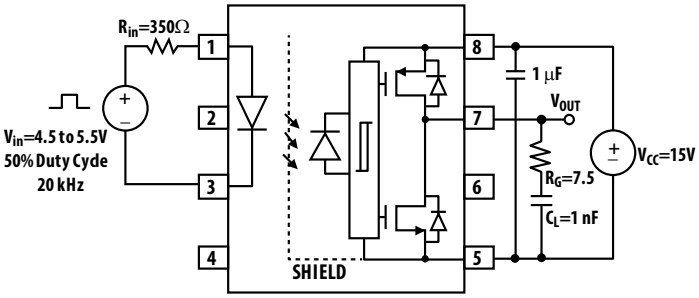


Figure 13: t_r and t_f Test Circuit

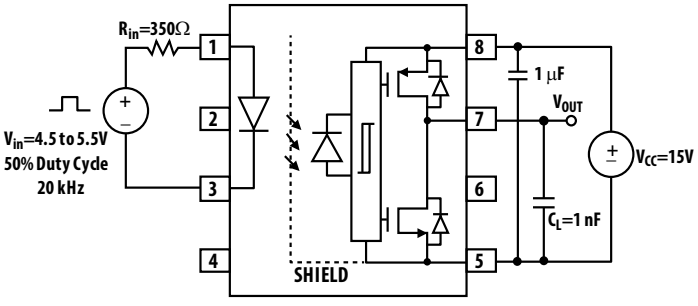


Figure 14: t_{PLH}, t_{PHL}, t_r, and t_f Reference Waveforms

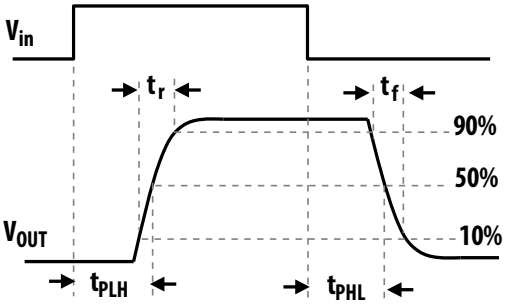


Figure 15: CMR Test Circuit

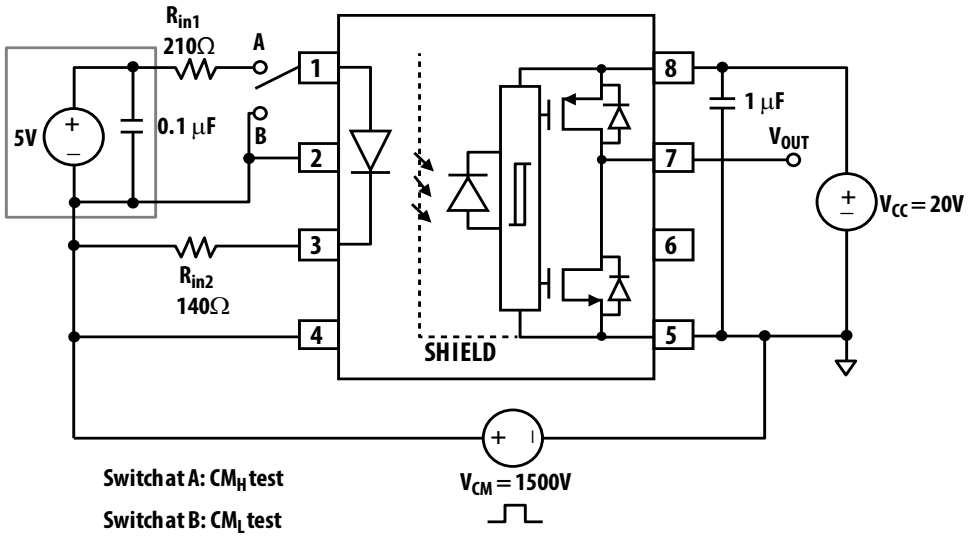
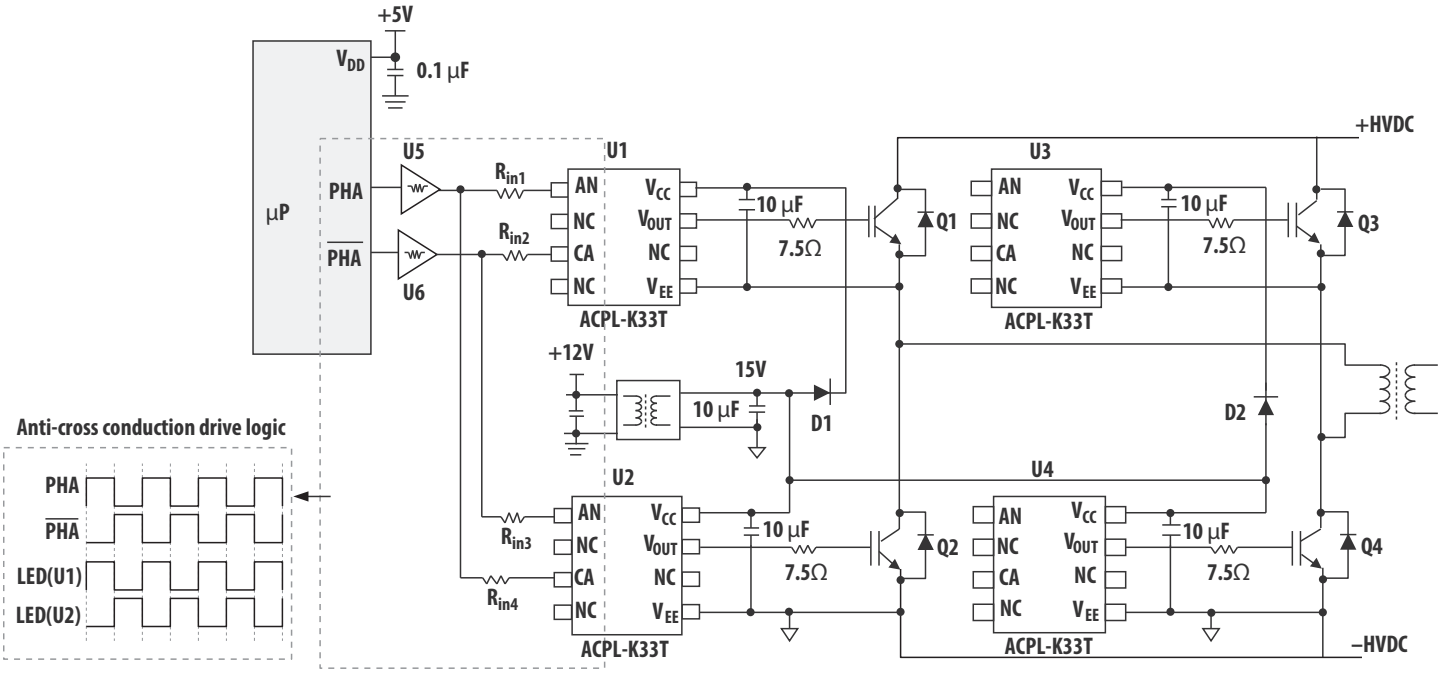


Figure 16: Typical High-Speed SiC MOSFET/IGBT Gate Drive Circuit



Anti-Cross Conduction Drive

One of the many benefits of using the ACPL-K33T is the ease of implementing an anti-cross conduction drive between the high-side and the low-side gate drivers to prevent a shoot-through event. This safety interlock drive can be realized by interlocking the output of buffer U5 and U6 to both the high-side and the low-side gate drivers, as shown in Figure 16. Due to the difference in propagation delay between optocouplers, however, a certain amount of dead time must be added to ensure sufficient dead time at the MOSFET gate. For more details, see Dead Time and Propagation Delay Waveforms.

Recommended LED Drive Circuits

There will be common mode noise whenever the ground level of the optocoupler's input control circuitry differs from the output control circuitry. Figure 17 and Figure 18 show the recommended LED drive circuits that use a logic gate (CMOS buffer) for high common mode rejection (CMR) performance of the optocoupler gate driver. Split limiting resistors are used to balance the impedance at both the anode and the cathode of the input LED for high common mode noise rejection. The output impedance of the CMOS buffer (shown as R_O in Figure 17 and Figure 18) must be included in the calculation for LED drive current.

On the other hand, Figure 19 and Figure 20 show the recommended LED drive circuits that use a single transistor. During the LED off state, M1 and Q1 in Figure 19 and Figure 20 will shunt the current, which results in greater power consumption. It is not recommended to have open-drain and open-collector drive circuits, as shown in Figure 21 and Figure 22. This is because during the off state of the MOSFET/transistor, the cathode of the input LED sees high impedance and becomes sensitive to noise.

Drive Power

If a CMOS buffer is used to drive the LED, it is recommended that you connect the CMOS buffer at the LED cathode. This is because the sinking capability of the NMOS is usually greater than the driving capability of the PMOS in a CMOS buffer.

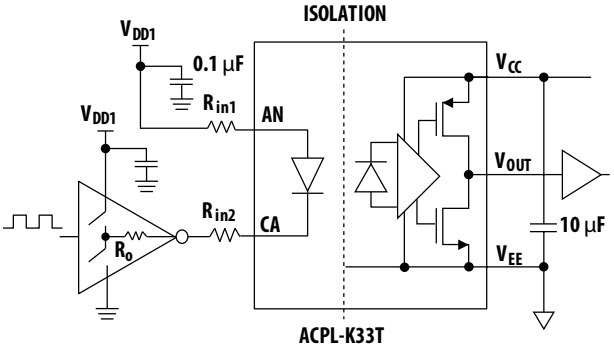
Drive Logic

The designer can configure LED drive circuits for non-inverting and inverting logic as recommended in Figure 17 and Figure 18. For the inverting and non-inverting logic to work, the external power supply V_{DD1} must be connected to the CMOS buffer. If the V_{DD1} supply is lost, the LED will be permanently off and output will be low.

Bypass and Reservoir Capacitors

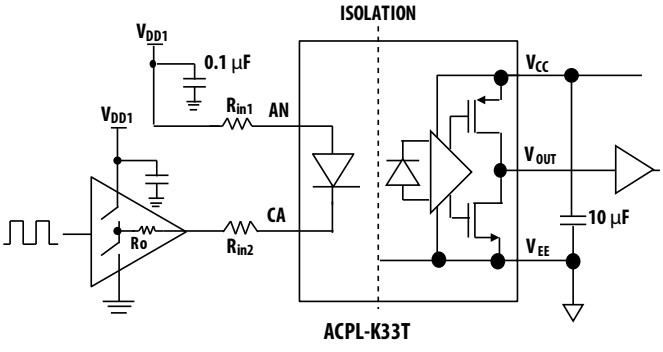
Supply bypass capacitors are necessary at the input buffer and the ACPL-K33T output supply pin. A ceramic capacitor with a value of 0.1 µF is recommended at the input buffer to provide high-frequency bypass, which also helps to improve CMR performance. At the output supply pin ($V_{CC} – V_{EE}$), it is recommended to use a 10-µF, low-ESR, and low-ESL capacitor as a charge reservoir to supply instant driving current to the IGBT at V_{OUT} during switching.

Figure 17: Recommended Non-Inverting Logic Gate Drive Circuit



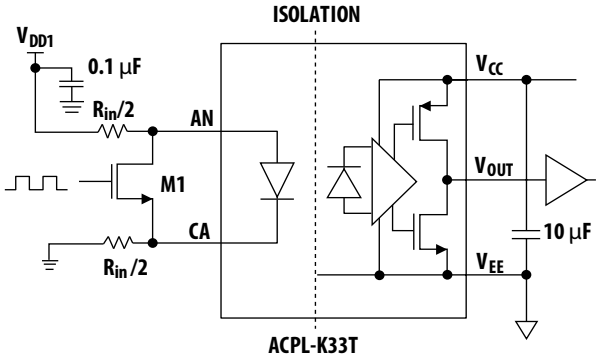
V_{DD1} = 5V ± 10%
Ratio R_{in1}: (R_{in2} + R_o) = 1.5:1
Recommended R_o + R_{in1} + R_{in2} = 350Ω

Figure 18: Recommended Inverting Logic Gate Drive Circuit



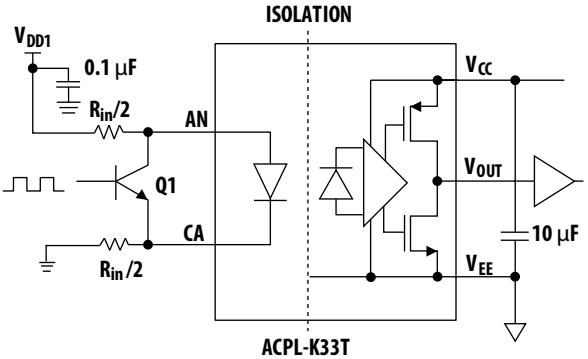
V_{DD1} = 5V ± 10%
Ratio R_{in1}: (R_{in2} + R_o) = 1.5:1
Recommended R_o + R_{in1} + R_{in2} = 350Ω

Figure 19: Recommended Single-Transistor Drive Circuit



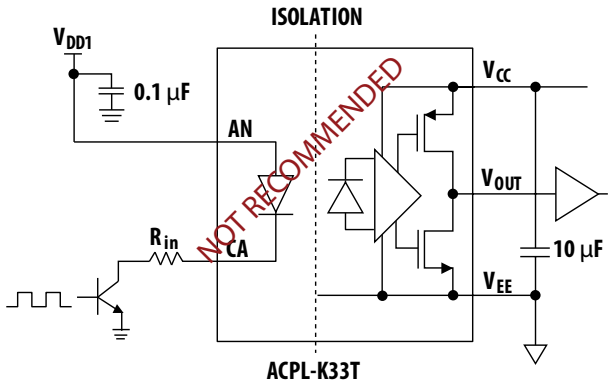
V_{DD1} = 5V ± 10%
Ratio R_{in1}: R_{in2} = 1.5:1
Recommended R_{in1} + R_{in2} = 350Ω

Figure 20: Recommended Single-Transistor Drive Circuit



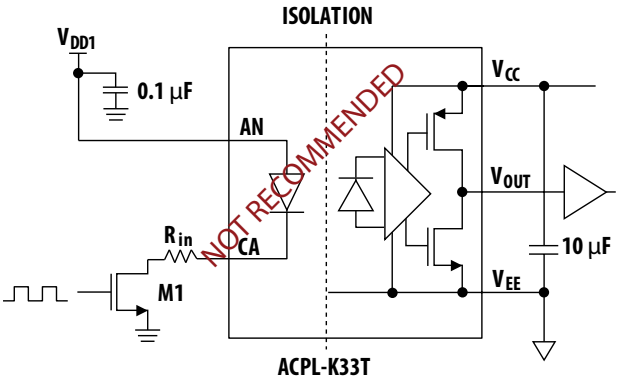
V_{DD1} = 5V ± 10%
Ratio R_{in1}: R_{in2} = 1.5:1
Recommended R_{in1} + R_{in2} = 350Ω

Figure 21: Not Recommended – Open-Drain/Open-Collector Drive Circuit (1)



NOTE: Not recommended.

Figure 22: Not Recommended – Open-Drain/Open-Collector Drive Circuit (2)

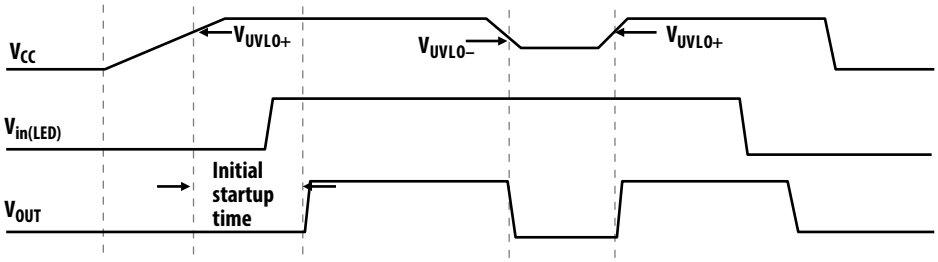


NOTE: Not recommended.

Initial Power-Up and UVLO Operation

Insufficient gate voltage to the IGBT can increase IGBT turn-on resistance, resulting in a large power loss and damage to the IGBT due to high heat dissipation. The ACPL-K33T constantly monitors the output power supply. During initial power-up, the ACPL-K33T requires a maximum of 50 µs initial startup time for the internal bias and circuitry to get ready. The gate driver output (V_{OUT}) is held at the off state during the initial startup time. Thereafter, when the output power supply is lower than the under-voltage lockout (V_{UVLO-}) threshold, the gate driver output will shut off to protect the IGBT from low-voltage bias. When the output power supply is more than the V_{UVLO+} threshold, V_{OUT} is released from the low state and it follows the input LED drive signal, as shown in Figure 23.

Figure 23: ACPL-K33T Initial Power-Up and UVLO Operation



Dead Time Distortion and Propagation Delay

Dead time is the period of time during which both high-side and low-side power transistors (shown as Q1 and Q2 in Figure 16) are off. Originally, the system is required to design in some amount of dead time to compensate for the turn-off delay needed for the MOSFET to discharge the input capacitance after the gate is switched off. This amount of dead time is called the system original dead time. When an optocoupler is used, the designer must consider the effect of the optocoupler's dead time distortion (DTD) toward the system original dead time. The optocoupler's negative DTD decreases the system original dead time; on the other hand, the optocoupler's positive DTD increases the system original dead time. Therefore, the designer must add extra dead time to the system original dead time to compensate for the optocoupler's negative DTD. Figure 24 and Figure 25 illustrate the effect of the optocoupler's DTD to the system original dead time.

Dead Time and Propagation Delay Waveforms

Figure 24: Negative DTD Reduces the Original DT

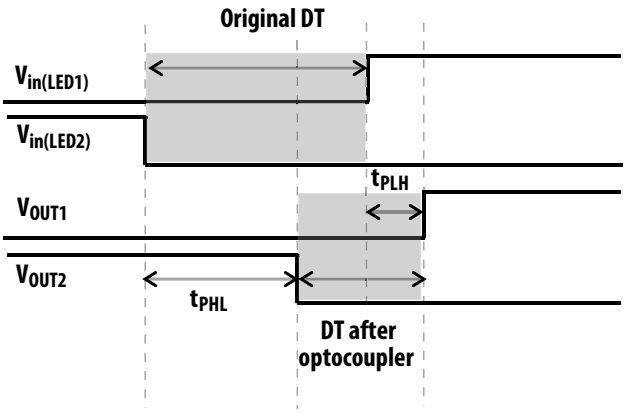
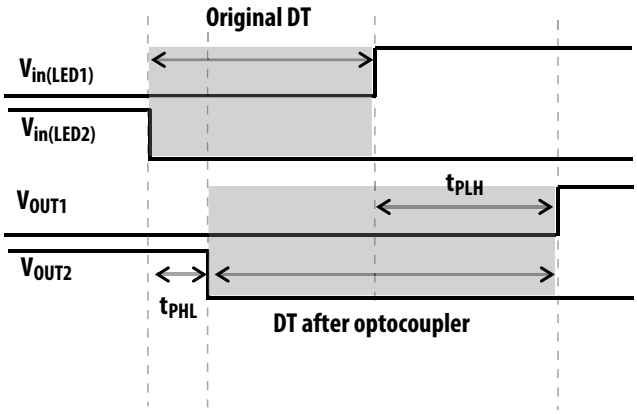


Figure 25: Positive DTD Increases the Original DT



Here is an example of the total dead time calculation for a typical optocoupler circuit for MOSFET driving.

Total dead time required = System original dead time + |optocoupler's negative DTD|

= System original dead time + |40 ns|

Where system original dead time = MOSFET turn-off delay

NOTE: The propagation delays used to calculate the dead time distortion (DTD) are taken at equal temperatures and test conditions because the optocouplers (used under consideration) are typically mounted in close proximity to each other and are switching the same type of MOSFETs.

Programmable Dead Time

The programmable dead time can be introduced to an optocoupler gate driver by adding an external capacitor (C_{DT}) across the input LED (anode and cathode) as shown in Figure 26. This simple circuitry offers you the flexibility to optimize gate drive switching timing for various MOSFETs and applications through hardware configuration.

The value of the external capacitor (C_{DT}) can be calculated based on the minimum dead time requirement for the system, as shown in the following equation. The added dead time will delay the turn-on timing of the gate signal, as shown in Figure 27.

$$C_{DT(min)} = - \frac{DT_{(min)}}{R_{in(min)} \ln\left(1 - \frac{V_{F(min)} - V_{in(off)}}{V_{in(on)} - V_{in(off)}}\right)}$$

Where:

DT: The total dead time required for a system, including the original dead time and the optocoupler's negative DTD

R_{in}: The total input LED current-limiting resistor

C_{DT}: The external dead time programming capacitor

V_F: The input LED forward voltage

V_{in}: The input PWM voltage

Figure 26: Add C_{DT} for Dead Time Programming

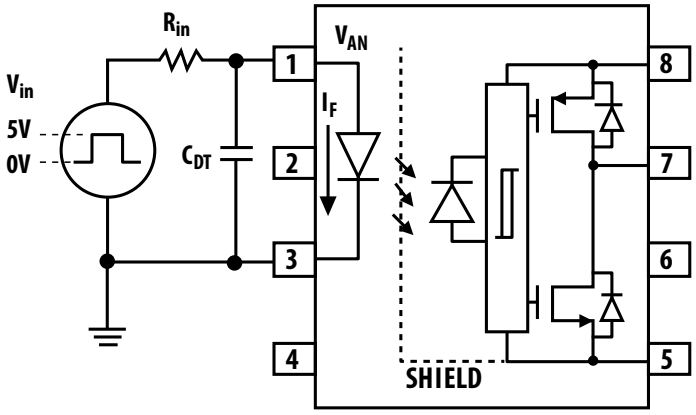
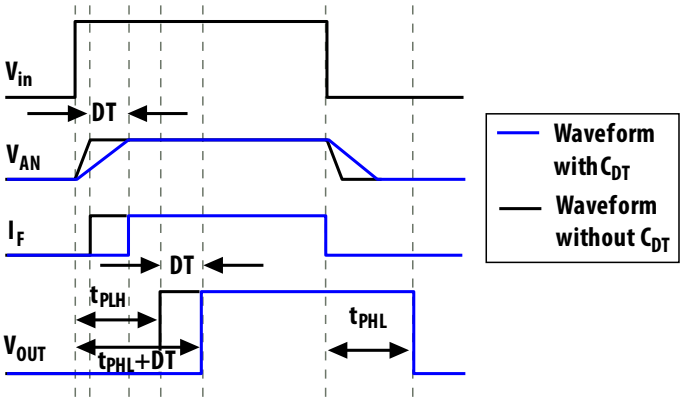


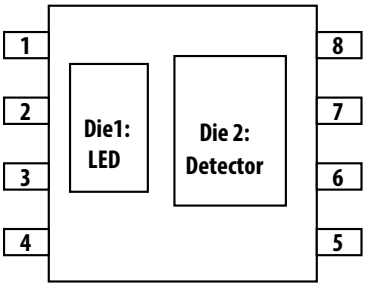
Figure 27: Timing Diagram with and without C_{DT}



Thermal Resistance Model for the ACPL-K33T

Figure 28 shows the diagram for measurement. Here, one die is first heated, and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated, and all the dice temperatures are recorded. With the known ambient temperature, die junction temperature, and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 2-by-2 matrix for our case of two heat sources.

Figure 28: Diagram of the ACPL-K33T for Measurement



$$\begin{vmatrix} R11 & R12 \\ R21 & R22 \end{vmatrix} \cdot \begin{vmatrix} P1 \\ P2 \end{vmatrix} = \begin{vmatrix} \Delta T1 \\ \Delta T2 \end{vmatrix}$$

R11: Thermal resistance of Die1 due to heating of Die1 (°C/W)

R12: Thermal resistance of Die1 due to heating of Die2 (°C/W)

R21: Thermal resistance of Die2 due to heating of Die1 (°C/W)

R22: Thermal resistance of Die2 due to heating of Die2 (°C/W)

P1: Power dissipation of Die1 (W)

P2: Power dissipation of Die2 (W)

T1: Junction temperature of Die1 due to heat from all dice (°C)

T2: Junction temperature of Die2 due to heat from all dice (°C)

Ta: Ambient temperature (°C)

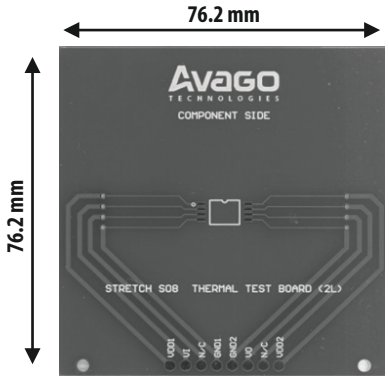
ΔT1: Temperature difference between Die1 junction and ambient (°C)

ΔT2: Temperature deference between Die2 junction and ambient (°C)

T1 = (R11 × P1 + R12 × P2) + Ta ----------(1)

T2 = (R21 × P1 + R22 × P2) + Ta ----------(2)

Measurement is done on both low-conductivity and high-conductivity boards as shown in the following table.

Layout	Measurement Data	
	Low-conductivity board per JEDEC 51-3: R11 = 191°C/W R12 = R21 = 68.5°C/W R22 = 77°C/W	High-conductivity board per JEDEC 51-7: R11 = 155°C/W R12 = R21 = 64°C/W R22 = 41°C/W

NOTE: These thermal resistances R11, R12, R21, and R22 can be improved by increasing the ground plane/copper area.

The application and environment design for the ACPL-K33T must ensure that the junction temperature of the internal IC and LED within the gate drive optocoupler does not exceed 150°C. Use equation (1) and equation (2) to estimate the junction temperatures. For example:

Calculation of the LED and Output IC Power Dissipation:

LED Power Dissipation, $P_E = I_{F(LED)}$ (Recommended Max.) × $V_{F(LED)}$ (at 125°C) × Duty Cycle
= 13 mA × 1.25V × 50%
= 8.125 mW

Output IC Power Dissipation, $P_O = V_{CC}$ (Recommended Max.) × I_{CC} (Max.) + P_{HS} + P_{LS}
= 30V × 4.2 mA + 60 mW + 34.3 mW
= 220.3 mW

Where:

P_{HS} = High-side switching power dissipation
= $(V_{CC} \times Q_G \times f_{PWM}) \times R_{DS,OH(MAX)}/(R_{DS,OH(MAX)} + R_{GH})/2$
= (30V × 80 nC × 200 kHz) × 4Ω/(4Ω +12Ω)/2
= 60 mW

P_{LS} = Low-side switching power dissipation
= $(V_{CC} \times Q_G \times f_{PWM}) \times R_{DS,OL(MAX)}/(R_{DS,OL(MAX)} + R_{GL})/2$
= (30V × 80 nC × 200 kHz) × 2Ω/(2Ω +12Ω)/2
= 34.3 mW

Q_G = Gate charge at supply voltage

f_{PWM} = LED switching frequency

R_{GH} = Gate charging resistance

R_{GL} = Gate discharging resistance

Calculation of the LED Junction Temperature and Output IC Junction Temperature at T_a=125°C Based on a High-Conductivity Board Thermal Resistance Model:

LED Junction Temperature, T1 = $(R11 \times P_E + R12 \times P_O) + T_a$
= (155°C/W × 8.125 mW + 64°C/W × 220.3 mW) + 125°C
= 140°C < T_J(absolute max.) of 150°C

Output IC Junction Temperature, T2 = $(R21 \times P_E + R22 \times P_O) + T_a$
= (64°C/W × 8.125 mW + 41°C/W × 220.3 mW) + 125°C
= 135°C < T_J(absolute max.) of 150°C

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