AFBR-59E4APZ, AFBR-5803x, AFBR-5972Z, AFBR-59F1Z, HFBR-57E5APZ, AFBR-57E6APZ

Interfacing Avago Technologies Fast Ethernet Optical Transceivers with Various PHY ICs

Application Note 5582

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Introduction

This application note discusses the terminations required at both ends of the transmitter (Tx) and receiver (Rx) transmission lines for proper interconnection of different Avago Technologies Fast Ethernet Optical Transceivers with various PHY ICs from several selected manufacturers.

AC-coupling has been chosen as the general interfacing option in all cases presented in this application note due to its simplicity, compared to DC-coupling. For AC-coupling, a designer does not have to look out for common mode voltage compatibility between the output of the PHY IC and the input of the optical transceiver and vice versa, because the common mode voltage of the output signal is removed by the de-coupling capacitors and then fixed on the input side to the required level.

Avago Fast Ethernet Optical Transceivers covered in this document are:

- AFBR-59E4APZ
- AFBR-5803x
- AFBR-5972Z
- AFBR-59F1Z
- HFBR-57E5APZ
- AFBR-57E6APZ

The following PHY IC devices are considered:

- Broadcom BCM54618SE
- IC+ IP101G
- Micrel KSZ8041FTL

Some similar PHY ICs are available from Broadcom and IC+ that feature a Fast Ethernet Optical Transceiver interface matching with BCM54618SE and IP101G mentioned earlier. As such, the terminations described in this application note should work as well with those other PHY ICs. For more details, see Compatible PHY ICs on page 13.

The interfaces (terminations) defined in this application note have been evaluated at room temperature using Spirent Fast Ethernet traffic generator and analyzer. For a PRBS7 payload of the Ethernet frames, it has been confirmed a 0% frame loss in a communication held for 30 seconds between the PHY IC and the Avago Fast Ethernet Optical Transceiver. The interfaces proposed here, however, have not been verified over voltage, temperature and other parameter shifts.

Therefore the schematics shown in this application note are recommendations and Avago cannot guarantee full function and performance. The designer should perform his own verification.

AFBR-59E4APZ

This optical transceiver has LVPECL input/outputs. The device already includes de-coupling capacitors for an AC-coupled interface; therefore, the only issue the circuit designer has to consider is the voltage swing of the signal supplied by the output of the PHY to the input of the optical transceiver and vice versa.

Figure 1 shows the internal configuration of AFBR-59E4APZ.

Figure 1 Internal Structure of AFBR-59E4APZ

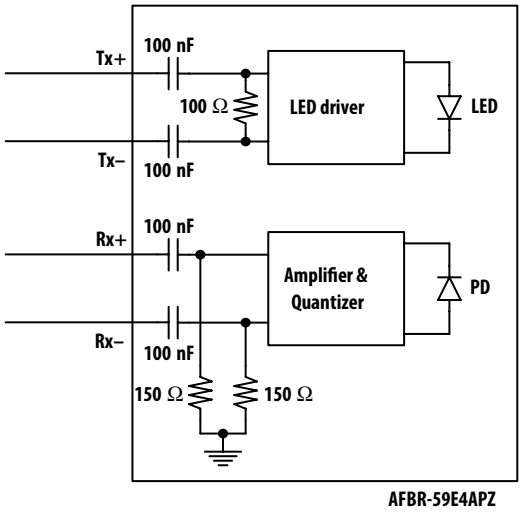


Table 1 shows the Signal Detect (SD) voltage levels supplied by the optical Rx of AFBR-59E4APZ.

Table 1 Signal Detect Voltage Levels Supplied by AFBR-59E4APZ

	Min.	Max.
Invalid data signal	V_{dd} – 1.81 V	V_{dd} – 1.62 V
Valid data signal	V_{dd} – 1.02 V	V_{dd} – 0.88 V

The parameter V_{dd} shown in Table 1 has a typical value of 3.3 V.

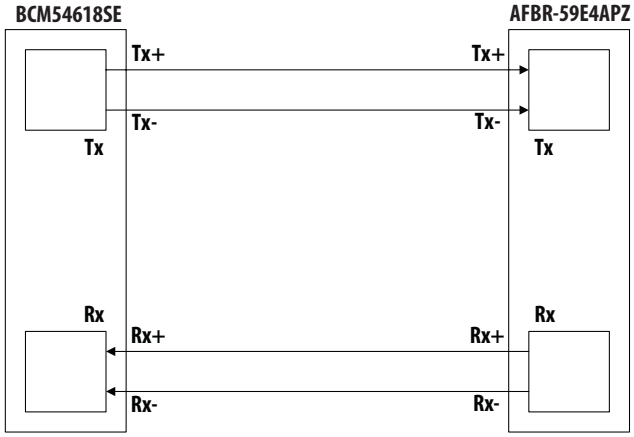
Broadcom BCM54618SE

This PHY requires an AC-coupled interface for the communication with an external 100BASE-FX optical transceiver.

The terminations for 50 Ω impedance matching and common mode level adjustment at the PHY inputs are included in the device; therefore, no external termination is needed. The PHY outputs do not necessitate any external termination either. On the other hand, BCM54618SE does not need the SD output of the Fast Ethernet optical transceiver to be connected to the PHY. These features lower the complexity of the design.

Figure 2 shows the interconnection between AFBR-59E4APZ and BCM54618SE.

Figure 2 Interconnection between AFBR-59E4APZ and BCM54618SE



IC+ IP101G

This PHY IC has LVPECL inputs/outputs for communication with an external 100Base-FX optical transceiver.

The output stage of LVPECL requires to source current to ground. This is usually achieved by placing two 150 Ω resistors between ground and Tx+/Tx-, respectively. For IP101G, these resistors are included in the PHY IC, and so layout of the terminations is simplified, making it easier for the circuit designer to connect IP101G to an optical transceiver. On the other hand, the resistors required for the 50 Ω impedance matching of the input stage are also built-in within the PHY IC. Therefore, the only terminations required by this PHY are the resistors that provide the correct common mode level to the input stage.

As the common mode level required by LVPECL is 2.0 V, the resistors shown in Figure 3 are a good combination. The high values of these resistors ensure low current through them, which translates into low power consumption.

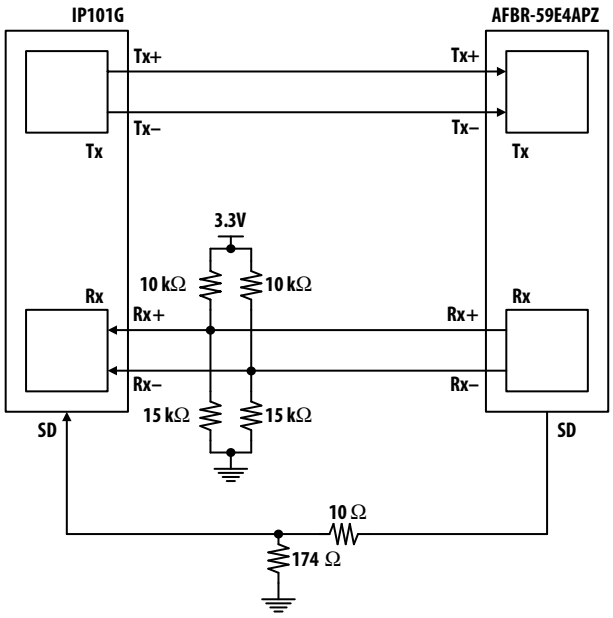
Table 2 shows the SD input voltage levels required by IP101G. The values shown in Table 1 and Table 2 allow setting the correct voltage divider for the connection of SD.

Table 2 Signal Detect Voltage Levels Required by IP101G

	Min.	Max.
Invalid data signal	1.3 V	1.7 V
Valid data signal	2.0 V	3.3 V + 0.5 V

Figure 3 shows the interconnection of AFBR-59E4APZ and IP101G.

Figure 3 Interconnection between AFBR-59E4APZ and IP101G



Micrel KSZ8041FTL

This PHY IC has CML inputs/outputs for communication with an external 100Base-FX optical transceiver.

The output stage of CML is based on an open-drain differential pair, which sinks current that must be supplied from outside. This current is usually provided by connecting 50 Ω resistors between V_{CC} and Tx+/Tx-. At the input stage, a common mode level of around 3.3 V is required by KSZ8041FTL. This common mode level is achieved by connecting 50 Ω resistors between Vcc and Rx+/Rx-.

AFBR-59E4APZ has LVPECL input/outputs. The voltage swing of the signal at the outputs Tx+/Tx- of the PHY IC is compatible with the voltage swing expected by the optical module at its inputs Tx+/Tx-. Also the voltage swing of the signal at the outputs Rx+/Rx- of the optical module is compatible with the voltage swing expected by the PHY IC at its inputs Rx+/Rx-. As

such, both devices. optical module and PHY IC can directly be connected to each other, because AFBR-59E4APZ is AC-coupled and it includes the correct terminations inside the housing (see Figure 1).

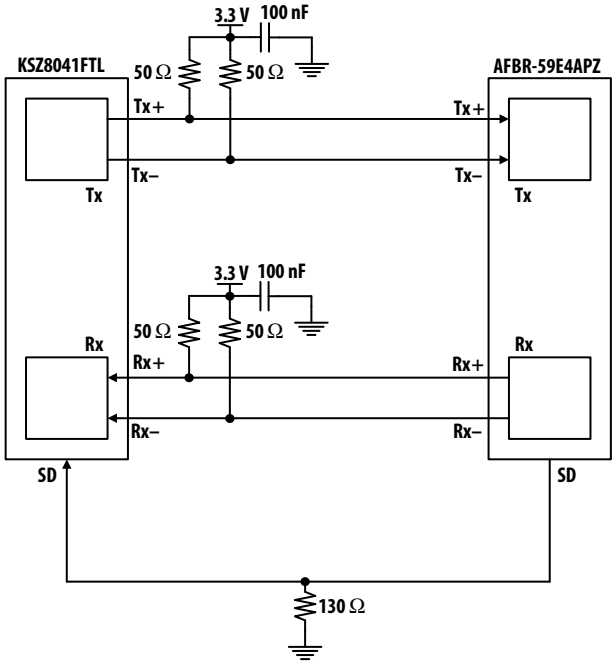
Table 3 shows the SD input voltage levels required by KSZ8041FTL. The values shown in Table 1 and Table 3 allow the correct voltage divider to be set for the connection of SD.

Table 3 Signal Detect Voltage Levels Required by KSZ8041FTL

	Min.	Max.
Invalid data signal	1.0 V	1.8 V
Valid data signal	2.2 V	—

Figure 4 shows the schematic of the interconnection between KSZ8041FTL and AFBR-59E4APZ.

Figure 4 Interconnection between AFBR-59E4APZ and KSZ8041FTL

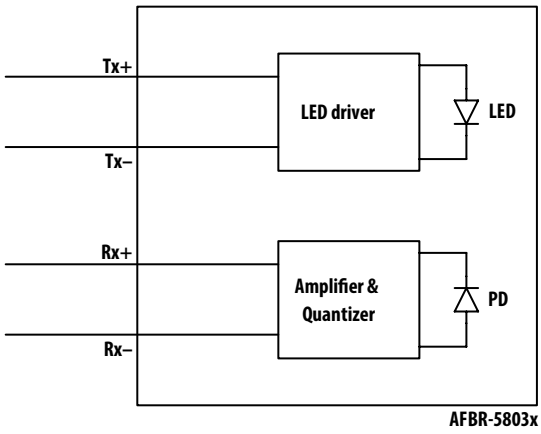


AFBR-5803x

This optical transceiver also features LVPECL inputs/outputs. In opposition to AFBR-59E4APZ, AFBR-5803Z does not include built-in de-coupling capacitors or adaptation resistors.

Figure 5 shows the internal structure of AFBR-5803x.

Figure 5 Internal Structure of AFBR-5803x



Since AFBR-5803x does not include any built-in adaptation resistors, an 82 Ω/130 Ω voltage divider is required at the Tx+/Tx- inputs to provide 50 Ω impedance matching, as well as to fix the common mode level to 2.0 V, which is the level required by these LVPECL inputs. On the other hand, 150 Ω resistors connected to ground are required at the Rx+/Rx- outputs to provide a path to ground for the emitter current of the output stage.

Table 4 shows the SD voltage levels supplied by the optical Rx of AFBR-5803x.

Table 4 Signal Detect voltage levels supplied by AFBR-5803Z

	Min.	Max.
Invalid data signal	V_{dd} – 1.83 V	V_{dd} –1.55 V
Valid data signal	V_{dd} – 1.085 V	V_{dd} – 0.88 V

The AFBR-5803x can be operated at a nominal voltage of either 3.3 V or 5 V. Only the 3.3 V supply option will be considered for AFBR-5803x here, as the tested PHY ICs work at this supply voltage.

Broadcom BCM54618SE

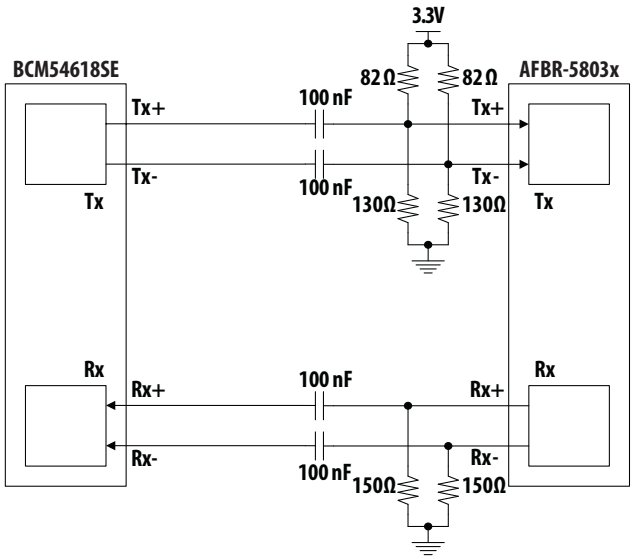
This PHY includes the terminations for 50-Ω impedance matching and common mode level adjustment at its inputs (Rx+/Rx-) and does not need any external termination at its outputs (Tx+/Tx-).

BCM54618SE does not require as an input the SD output of the optical transceiver.

BCM54618SE requires AC-coupling for the connection to any Fast Ethernet optical transceiver.

Figure 6 shows the interconnection between AFBR-5803x and BCM54618SE.

Figure 6 Interconnection between AFBR-5803 and BCM54618SE



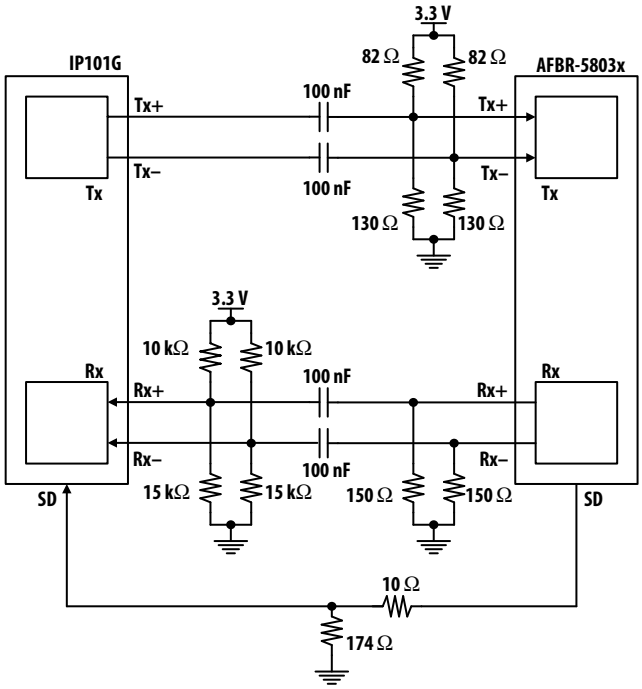
IC+ IP101G

A 10 kΩ/15 kΩ voltage divider at both Rx+/Rx- is the only adaptation network required by IP101G. This voltage divider fixes the common mode level at 2.0 V and ensures a low current flow through it at the same time.

Table 2 and Table 4 show that a 10 Ω/174 Ω voltage divider is a good option to fix the proper voltage levels at the SD input of the PHY IC.

Figure 7 shows the schematic of the interconnection between IP101G and AFBR-5803x.

Figure 7 Interconnection between AFBR-5803x and IP101G



Micrel KSZ8041FTL

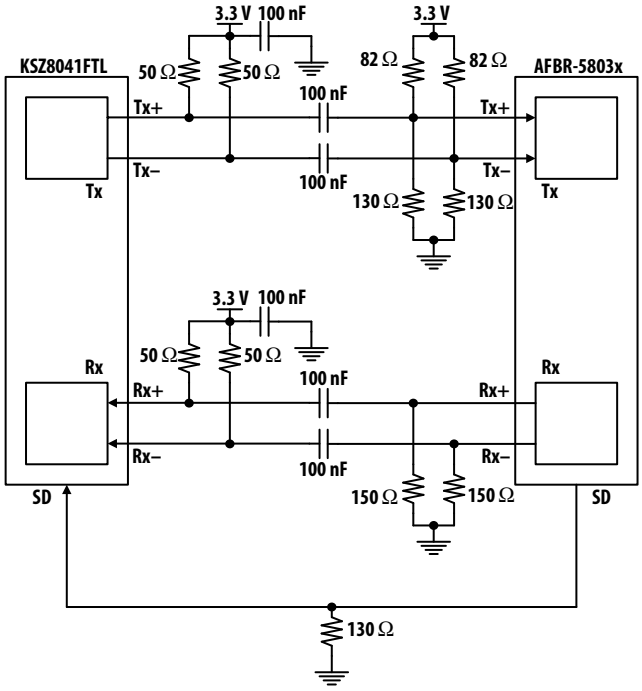
This PHY IC has CML inputs/outputs for communication with an external 100Base-FX optical transceiver.

It requires 50 Ω resistors between V_{cc} and Tx+/Tx- to source current to the open-drain output stage, and 50 Ω resistors between V_{cc} and Rx+/Rx- to fix the common mode level at the Rx+/Rx- inputs to 3.3 V as well as to provide 50 Ω impedance matching.

Table 3 and Table 4 show that a 130 Ω resistor between the SD trace and ground is enough to fix the voltage to the correct levels at the SD input of the PHY IC.

Figure 8 shows the schematic of the interconnection between KSZ8041FTL and AFBR-5803x.

Figure 8 Interconnection between AFBR-5803x and KSZ8041FTL



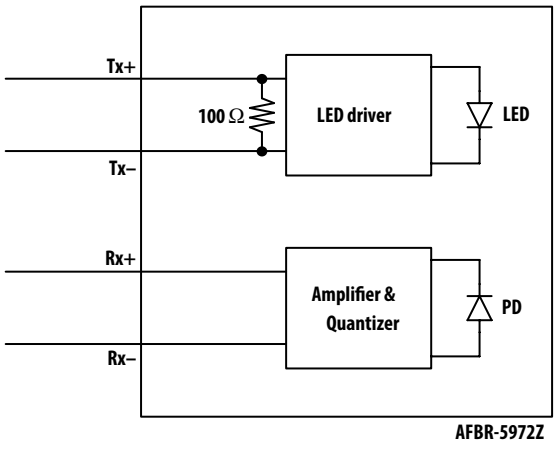
AFBR-5972Z

This optical transceiver accepts LVDS/LVPECL signals at the Tx+/Tx- inputs and delivers LVPECL signals at the Rx+/Rx- outputs.

LVDS is the standard used in this application note for the evaluation of AFBR-5972Z.

Figure 9 shows the internal configuration of AFBR-5972Z.

Figure 9 Internal structure of AFBR-5972Z



As AFBR-5972Z will be AC-coupled to the PHY IC, the terminations required by the optical transceiver are the ones needed to establish the common mode level at the Tx+/Tx- inputs and to source current to ground at the Rx+/Rx- outputs. The 50 Ω impedance matching at the Tx lines is provided by the internal 100 Ω resistor between Tx+ and Tx-. The common mode level at the Tx+/Tx- inputs will be fixed at 1.65 V, which is within the range defined for an LVDS differential input. This level is achieved by connecting a 10 kΩ pull-up resistor and a 10 kΩ pull-down resistor to Tx+/Tx-.

Table 5 shows the SD voltage levels supplied by the optical Rx of AFBR-5972Z.

Table 5 Signal Detect Voltage Levels Supplied by AFBR-5972Z

	Min.	Max.
Invalid data signal	V_{dd} – 1.83 V	V_{dd} – 1.50 V
Valid data signal	V_{dd} – 1.16 V	V_{dd} – 0.88 V

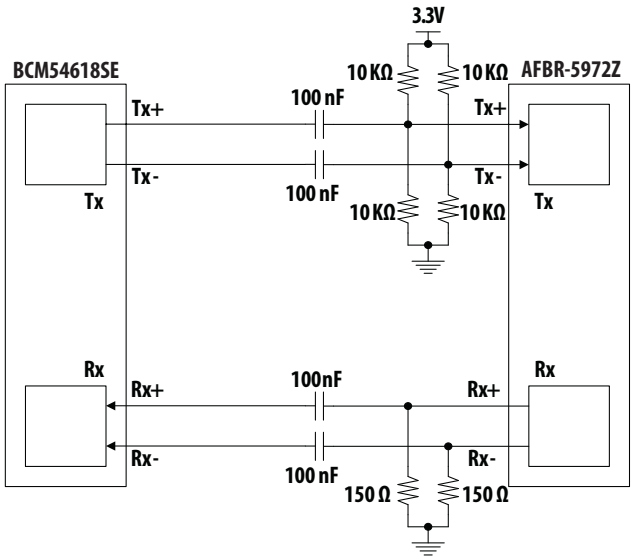
The parameter V_{dd} shown in Table 1 has a typical value of 3.3 V.

Broadcom BCM54618SE

This PHY requires de-coupling capacitors for the connection to any Fast Ethernet optical transceiver. No termination is needed at its inputs or at its outputs. Also, there is no need to connect the SD output of the Fast Ethernet optical transceiver to the PHY.

Figure 10 shows the interconnection between AFBR-5972Z and BCM54618SE.

Figure 10 Interconnection between AFBR-5972Z and BCM54618SE

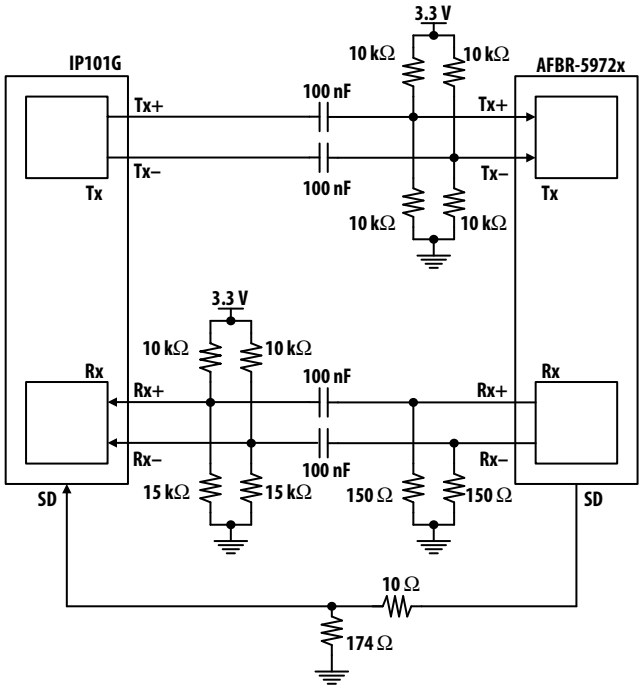


IC+ IP101G

Figure 11 shows the schematic of the interconnection between IP101G and AFBR-5972Z.

Table 2 and Table 5 show that a 10 Ω/174 Ω voltage divider is a good option to fix the proper voltage levels at the SD input of the PHY IC.

Figure 11 Interconnection between AFBR-5972Z and IP101G



The 10 kΩ/15 kΩ voltage divider placed at both Rx+/Rx- is the only adaptation network required by IP101G. This voltage divider fixes the common mode level at 2.0 V and ensures a low current flow through it at the same time.

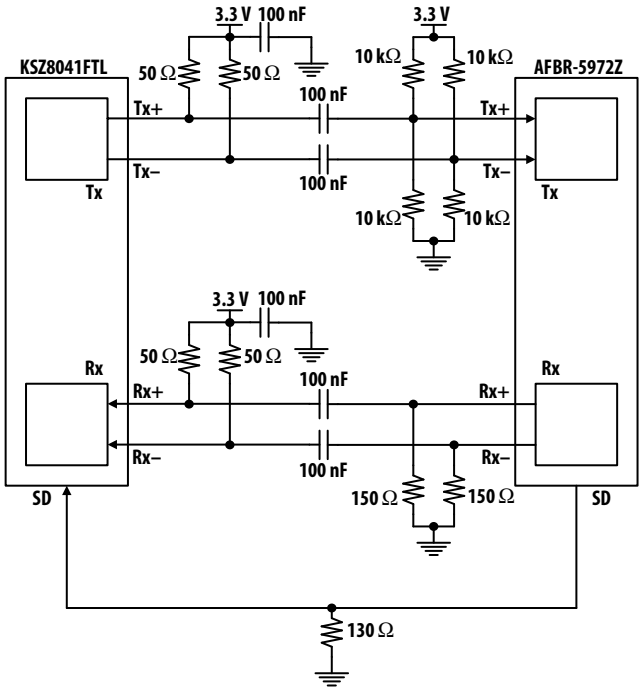
Micrel KSZ8041FTL

The KSZ8041FTL PHY IC requires 50 Ω resistors between V_{CC} and Tx+/Tx- to source current to the open-drain output stage, and also 50 Ω resistors between V_{CC} and Rx+/Rx- to fix the common mode level at the Rx+/Rx- inputs at 3.3 V as well as to provide 50 Ω impedance matching.

Table 3 and Table 5 show that a 130 Ω resistor between the SD trace and ground is enough to fix the voltage at the correct levels at the SD input of the PHY IC.

Figure 12 shows the schematic of the interconnection between KSZ8041FTL and AFBR-5972Z.

Figure 12 Interconnection between AFBR-5972Z and KSZ8041FTL

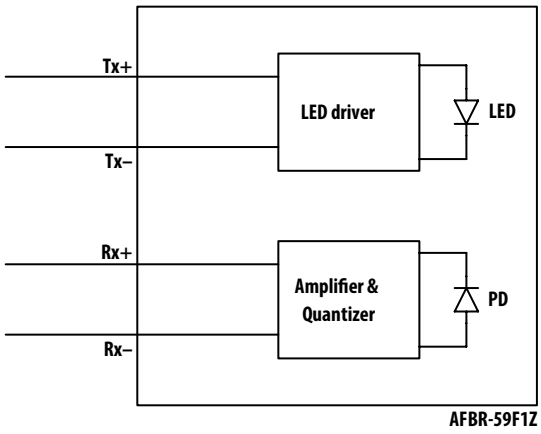


AFBR-59F1Z

This optical transceiver has LVPECL input/outputs. It does not include built-in de-coupling capacitors or adaptation resistors.

Figure 13 shows the internal structure of AFBR-59F1Z.

Figure 13 Internal Structure of AFBR-59F1Z



As AFBR-59F1Z does not include any built-in adaptation resistors, an 82 Ω/130 Ω voltage divider is required at the Tx+/Tx- inputs to provide 50 Ω impedance matching, as well as to fix the common mode level at 2.0 V. 150 Ω resistors connected to ground are needed at the Rx+/Rx- outputs to provide a path to ground to the emitter current of the output stage.

Table 6 shows the SD voltage levels supplied by the optical Rx of AFBR-59F1Z.

Table 6 Signal Detect Voltage Levels Supplied by AFBR-59F1Z

	Min.	Typ.	Max.
Invalid data signal	—	Vdd - 1.7 V	—
Valid data signal	—	Vdd - 0.8 V	—

Broadcom BCM54618SE

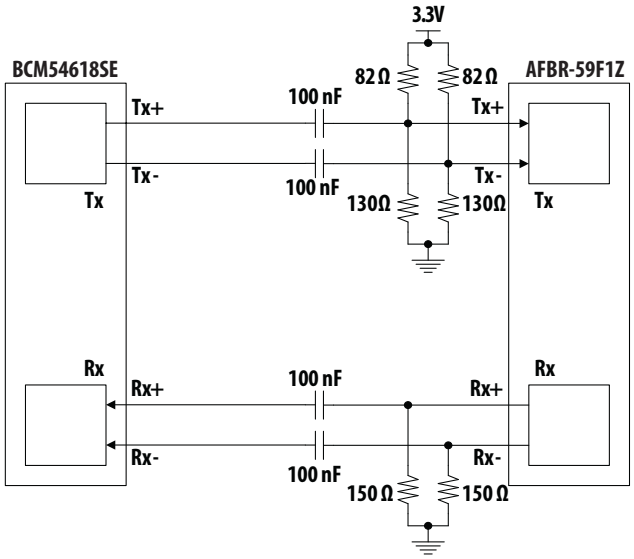
This PHY requires an AC-coupled interface for the communication with an external 100BASE-FX optical transceiver.

No termination is needed at the PHY inputs nor at its outputs, as these terminations are included in the package of the device.

BCM54618SE does not require as an input the SD output of the Fast Ethernet optical transceiver.

Figure 14 shows the interconnection between AFBR-59F1Z and BCM54618SE.

Figure 14 Interconnection between AFBR-59F1Z and BCM54618SE



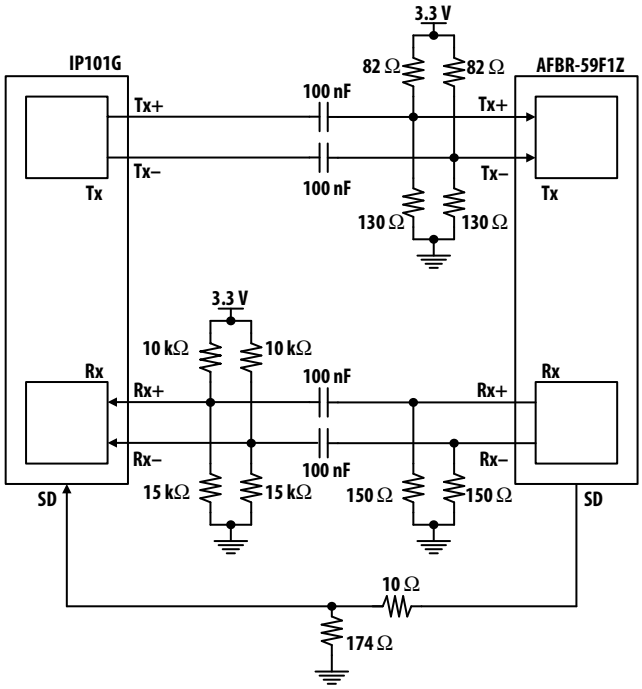
IC+ IP101G

A 10 kΩ/15 kΩ voltage divider at both Rx+/Rx- is the only adaptation network required by IP101G. This voltage divider fixes the common mode level at 2.0 V and ensures a low current flow through it at the same time.

Table 2 and Table 6 show that a 10 Ω/174 Ω voltage divider is a valid option to fix the proper voltage levels at the SD input of the PHY IC.

Figure 15 shows the schematic of the interconnection between IP101G and AFBR-59F1Z.

Figure 15 Interconnection between AFBR-59F1Z and IP101G



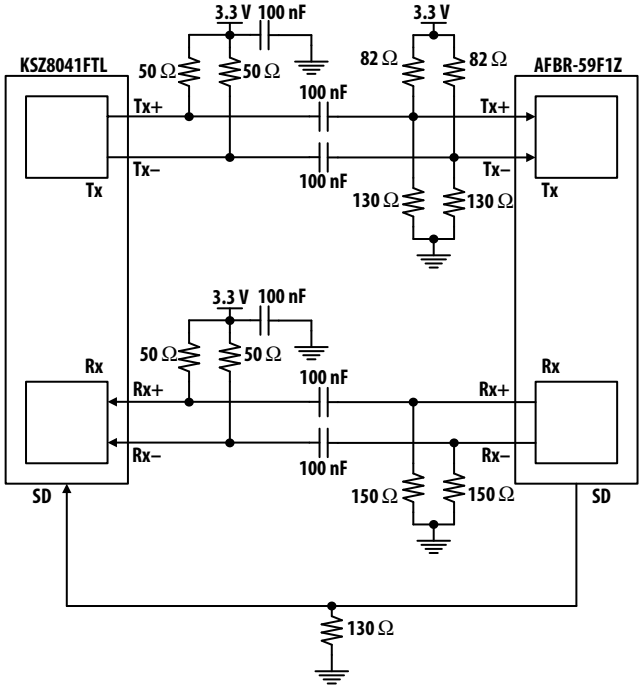
Micrel KSZ8041FTL

This PHY IC has CML inputs/outputs for communication with an external 100Base-FX optical transceiver; therefore, it requires 50 Ω resistors between V_{CC} and Tx+/Tx- to source current to its open-drain output stage and also 50 Ω resistors between V_{CC} and Rx+/Rx- to fix the common mode level at the Rx+/Rx- inputs to 3.3 V, as well as to provide 50 Ω impedance matching.

Table 3 and Table 6 show that a 130 v resistor between the SD trace and ground is enough to fix the voltage to the correct levels at the SD input of the PHY IC.

Figure 16 shows the schematic of the interconnection between KSZ8041FTL and AFBR-59F1Z.

Figure 16 Interconnection between AFBR-59F1Z and KSZ8041FTL



HFBR-57E5APZ/AFBR-57E6APZ

These optical transceivers have LVPECL input/outputs. The devices already include de-coupling capacitors for an AC-coupled interface; therefore, the only issue the circuit designer has to consider is the voltage swing of the signal supplied by the output of the PHY to the input of the optical transceiver and vice versa.

Figure 17 shows the internal configuration of HFBR-57E5APZ, while Figure 18 shows the internal configuration of AFBR-57E6APZ.

Figure 17 Internal Structure of HFBR-57E5APZ

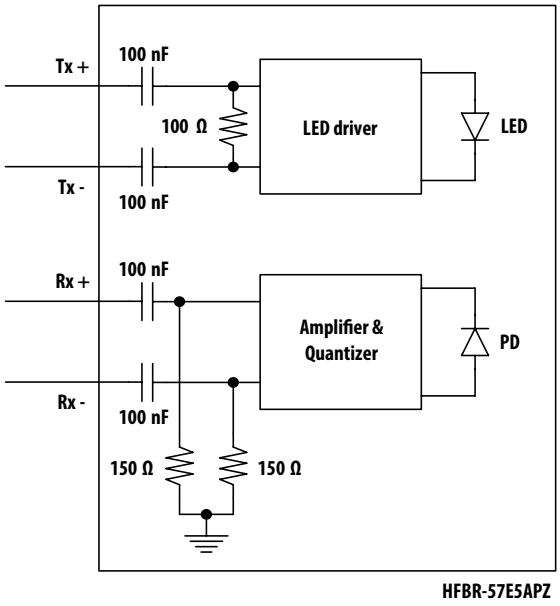
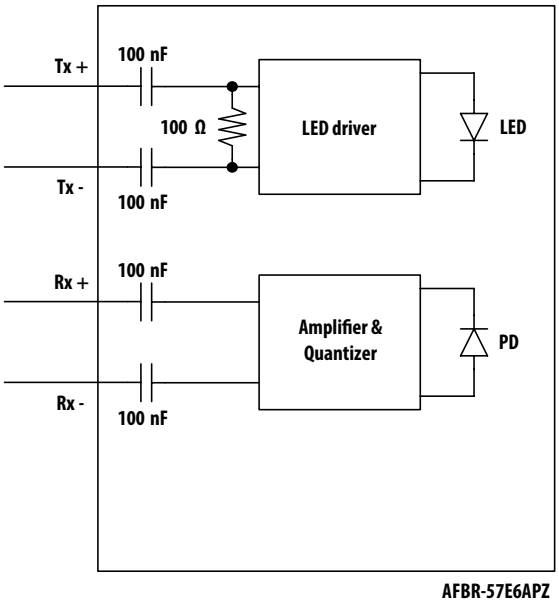


Figure 18 Internal Structure of AFBR-57E6APZ



In opposition to the optical transceivers previously introduced, HFBR-57E5APZ and AFBR-57E6APZ do not implement a SD output, but a Loss of Signal (LOS) output. The LOS output shows a high value when there is an invalid data signal at the input of the optical Rx and a low value when the data signal at the input of the optical Rx is valid.

Table 7 shows the LOS voltage levels supplied by the optical Rx of HFBR-57E5APZ and AFBR-57E6APZ.

Table 7 Loss of Signal Voltage Levels Supplied by HFBR-57E5APZ and AFBR-57E6APZ

	Min.	Max.
Invalid data signal	2.0 V	—
Valid data signal	—	0.8 V

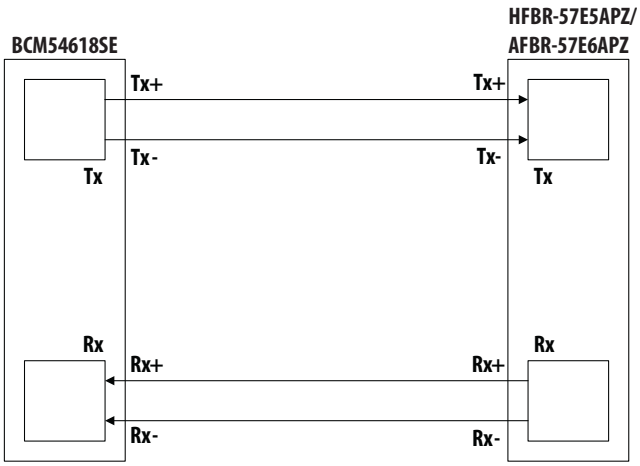
Broadcom BCM54618SE

This PHY includes the terminations for 50-Ω impedance matching and common mode level adjustment at its inputs (Rx+/Rx-) and does not need any external termination at its outputs (Tx+/Tx-). Also, there is no need to connect the SD output of the Fast Ethernet optical transceiver to the PHY.

BCM54618SE requires AC-coupling for the connection to any Fast Ethernet optical transceiver.

Figure 19 shows the interconnection between HFBR-57E5APZ/AFBR-57E6APZ and BCM54618SE.

Figure 19 Interconnection between HFBR-57E5APZ/AFBR-57E6APZ and BCM54618SE



IC+ IP101G

A 10KΩ/15KΩ voltage divider at both Rx+/Rx- is the only adaptation network required by IP101G. This voltage divider fixes the common mode level to 2.0V and assures a low current flow through it at the same time.

Since the voltage levels at the LOS output of the optical Rx of HFBR-57E5APZ and AFBR-57E6APZ are not compatible with the voltage levels expected by IP101G at its SD input (see Table 2), a voltage level conversion is required. This conversion is achieved by means of an LVTTL/LVCMOS to differential LVPECL translator. Specifically, the device MC10EPT20, from ON Semiconductor, has been used to evaluate the performance of HFBR-57E5APZ and AFBR-57E6APZ in combination with IC + IP101G, although similar voltage translators, such as SN65EPT22, from Texas Instruments, might also work.

Table 8 shows the voltage level conversion implemented by MC10EPT20. Due to the inverted behavior of an SD output with regards to a LOS output, the voltage levels shown in Table 8 are the ones available at the inverted output of MC10EPT 20. The inverted output of the voltage translator will be used to interconnect HFBR-57E5APZ/AFBR-57E6APZ to IP101G. The voltage levels shown in the column LVPECL inverted output of Table 8 are typical values, measured at 25 °C.

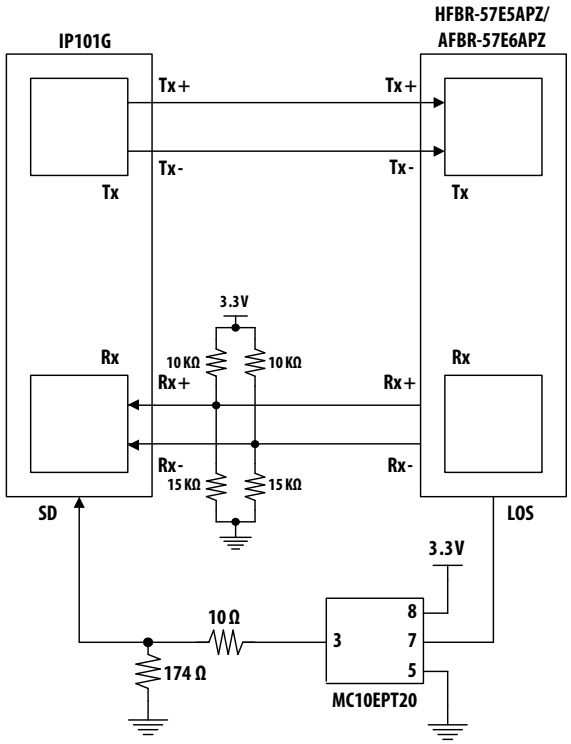
Table 8 Voltage Level Conversion Made by MC10EPT20

LVTTL/LVCMOS input	LVPECL Inverted Output
> 2.0 V	1.6 V
< 0.8 V	2.4 V

Table 2 and Table 8 allow setting the correct voltage divider for the interconnection of the LVPECL inverted output of MC10EPT20 and the SD input of IP101G.

Figure 20 shows the schematic of the interconnection between IP101G and HFBR-57E5APZ/AFBR-57E6APZ.

Figure 20 Interconnection between HFBR-57E5APZ/AFBR-57E6APZ and IP101G



Micrel KSZ8041FTL

This PHY IC has CML inputs/outputs for the communication with an external 100Base-FX optical transceiver.

It requires 50 Ω resistors between V_{CC} and Tx+/Tx- to source current to the open-drain output stage and also 50 Ω resistors between V_{CC} and Rx+/Rx- to fix the common mode level at the Rx+/Rx- inputs to 3.3V, as well as to provide 50 Ω impedance matching.

Since the voltage levels at the LOS output of the optical Rx of HFBR-57E5APZ and AFBR-57E6APZ are not compatible with the voltage levels expected by KSZ8041FTL at its SD input (see Table 3), a voltage level conversion is required. This conversion is achieved by means of an LVTTL/LVCMOS to differential LVPECL translator. Specifically, the device MC10EPT20, from ON Semiconductor, has been used to evaluate the performance of HFBR-57E5APZ and AFBR-57E6APZ in combination with Micrel KSZ8041FTL, although similar voltage translators, such as SN65EPT22, from Texas Instruments, might also work.

Table 9 shows the voltage level conversion implemented by MC10EPT20. Due to the inverted behavior of a SD output with regards to a LOS output, the voltage levels shown in Table 9 are the ones available at the inverted output of MC10EPT 20. The inverted output of the voltage translator will be used to interconnect HFBR-57E5APZ/AFBR-57E6APZ to KSZ8041FTL. The voltage levels shown in the column LVPECL inverted output of Table 9 are typical values, measured at 25°C.

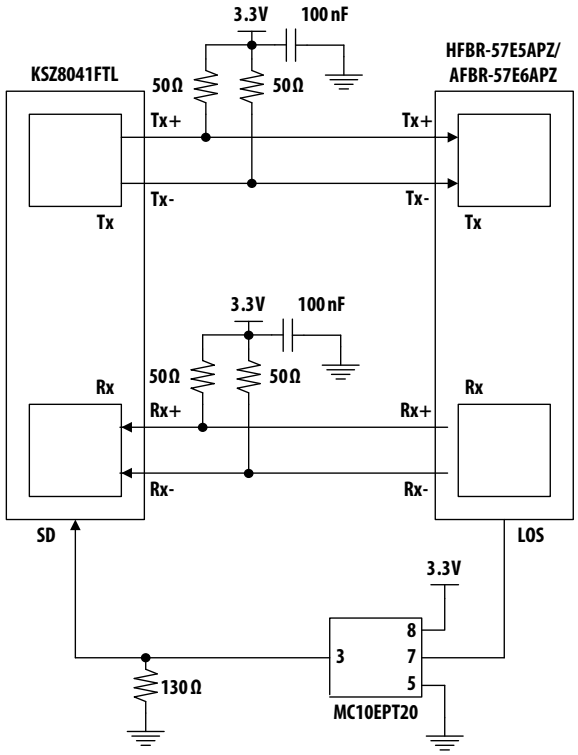
Table 9 Voltage Level Conversion Made by MC10EPT20

LVTTL/LVCMOS input	LVPECL inverted output
> 2.0 V	1.6 V
< 0.8 V	2.4 V

According to Table 3 and Table 9, a 130 Ω resistor between the SD trace and ground is enough to fix the correct voltage levels at the SD input of the PHY IC.

Figure 21 shows the schematic of the interconnection between KSZ8041FTL and HFBR-57E5APZ/AFBR-57E6APZ.

Figure 21 Interconnection between HFBR-57E5APZ/AFBR-57E6APZ and KSZ8041FTL



Compatible PHY ICs

In addition to Broadcom BCM54618SE and IC+ IP101G, there are similar PHY ICs from those manufacturers featuring the same interface for Fast Ethernet Optical Transceivers as the ones included in this document.

These other PHY ICs, which are listed as follows, should work perfectly with the terminations described in this application note. They, however, have not been tested; therefore, Avago cannot guarantee full function and performance. The designer should perform his own verification.

Broadcom

1. BCM54210S: This is a single-port 10/100/1000 PHY. The available port can be configured to work in 100BASE-FX mode.

The configurations shown in Figure 2, Figure 6, Figure 10, Figure 14, and Figure 19 should also be valid for BCM54210S.

IC+

1. IP175GH: This is a five-port embedded 10/100 PHY Switch Controller. It includes four 100Base-TX ports and one 100Base-FX port.
2. IP178G: This is an eight-port embedded 10/100 PHY Switch Controller. It includes six 100Base-TX ports and two 100Base-FX ports.

The configurations shown in Figure 3, Figure 7, Figure 11, Figure 15, and Figure 20 should also be valid for IP175GH and IP178G, as explained.

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