ACPL-302J

Isolated IGBT Gate Driver with Integrated DC/DC Controller evaluation board

User's Manual

Quick Start

Visual inspection is needed to ensure that the evaluation board is received in good condition.

Default connections of the evaluation board are as shown (see Figure 1):

1. The evaluation board is to be powered up by a +12V DC power supply (V_{in}) as shown to pins +12 V and GND1 of Connector P1. Through an internal DC/DC Controller plus an external Pulse Transformer (T1), a +20 V DC output supply (at V_{out}) is provided at pins V_{CC2} and V_{EE2} of Connector P2.
2. Pins AN and CA are provided at Connector P1 to allow for +5 V PWM input signals to be connected to drive the Gate Driver Optocoupler ACPL-302J's LED at 10 mA.
3. Gate (G) and Emitter (E) pins at P3, plus Collector (C) pin at P4 are provided to drive external IGBT (not provided) directly.
4. A 15 V Zener (D5) and 1 kΩ resistor (R30) are included in the eval board across V_{CC2} and V_E, and V_E and V_{EE2}, respectively, to have a 15V regulated V_{CC2} and -5V V_{EE2}, with respect to V_E.
5. Besides driving the external IGBT, the eval board provides feedback signals such as:
   a. An UnderVoltage LockOut Signal (/UVLO) – an active Low signal which is activated when V_{CC2} is lower than the turn-on threshold of ACPL-302J, and
   b. A Fault Signal (/Fault) – an active Low signal which is activated when external IGBT (it is driven) experiences an overcurrent or short circuit condition.

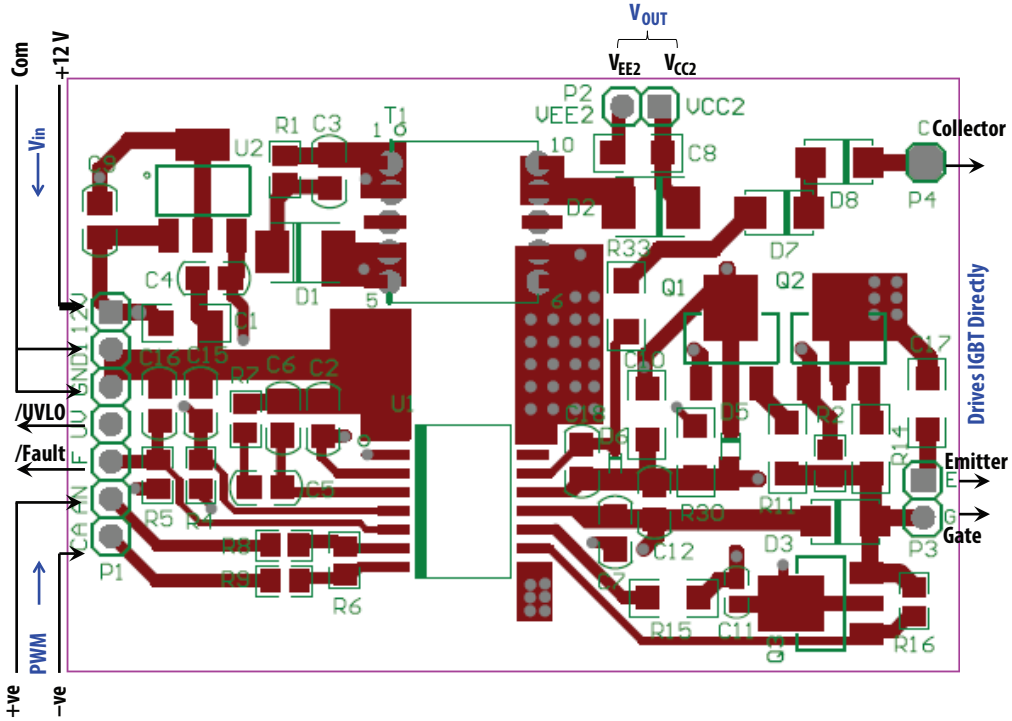

Figure 1. Actual ACPL-302J evaluation board showing default connections

Once physical inspection is complete, the evaluation board can be powered up in 4 simple steps according to Figure 2 as shown, in simulation mode without the need of actual IGBT.

Set Up IGBT Gate Driver (in Simulation Mode)

1. To simulate actual gate capacitance of an IGBT, solder a 10 nF capacitor across G (Gate) and E (Emitter) terminals at P3.
2. To simulate a turn-on saturated Collector voltage of IGBT, solder a jumper wire across the Collector at P4 to Emitter terminal at P3.
3. Connect a +12 V DC supply (PS1) across +12 V and GND1 terminals of P1.
4. To simulate microcontroller output to drive the IGBT, connect a 10 kHz 5 V PWM input signal (at about 50% duty) from a Signal Generator across AN and CA pins of P1.
5. To monitor the waveforms, use a multi-channel digital oscilloscope at the following points:
   a. Input PWM signal across AN and CA pins of P1.
   b. Input DC Supply Voltage PS1 across +12 V and GND1 terminals of P1.
   c. Output DC Voltage across V_{CC2} and V_{EE2} pins at P2; expect to see +20 V DC.
   d. V_G represents the gate drive output signal of ACPL-302J (U1) across Gate and Emitter pins of P3. Expect to see about 50% duty Gate Drive signals with peak-peak levels at -5 V and +15 V.
6. It is also good to check the status outputs of /UVLO and /Fault; use a multimeter to check that they are both High, for inactive status.

Note: The jumper wire connected during Step 2 must be removed before you proceed with the next steps.

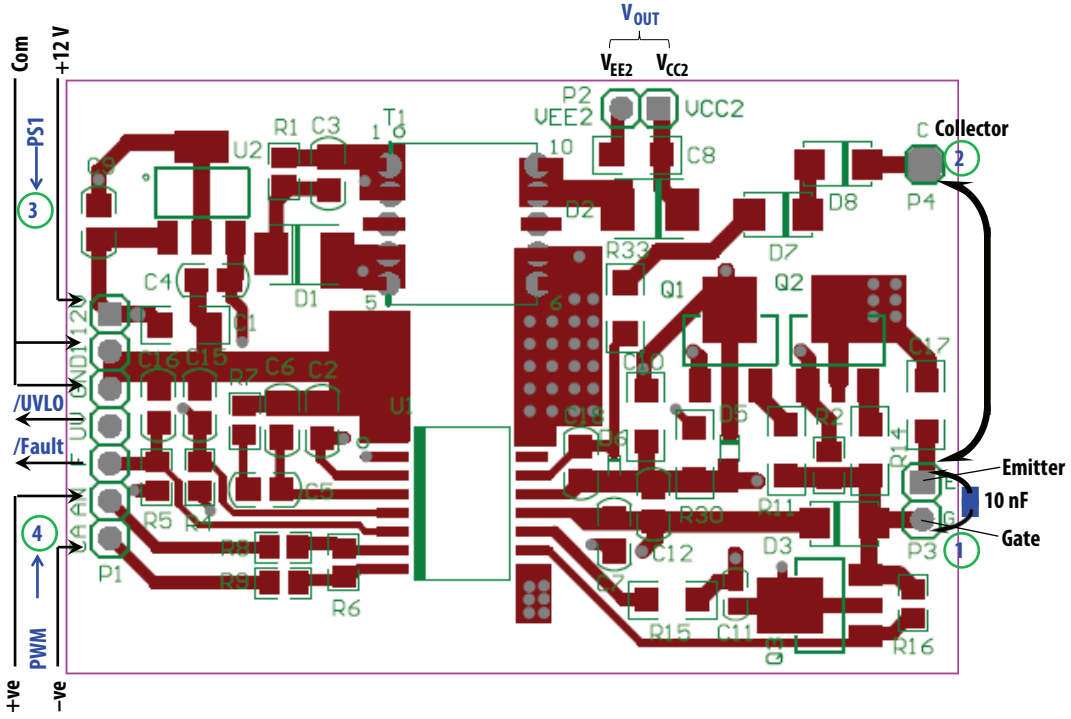

Figure 2. Simple Simulation Test Setup of Evaluation Board

Schematics

Figure 3 shows the schematics of the evaluation board.

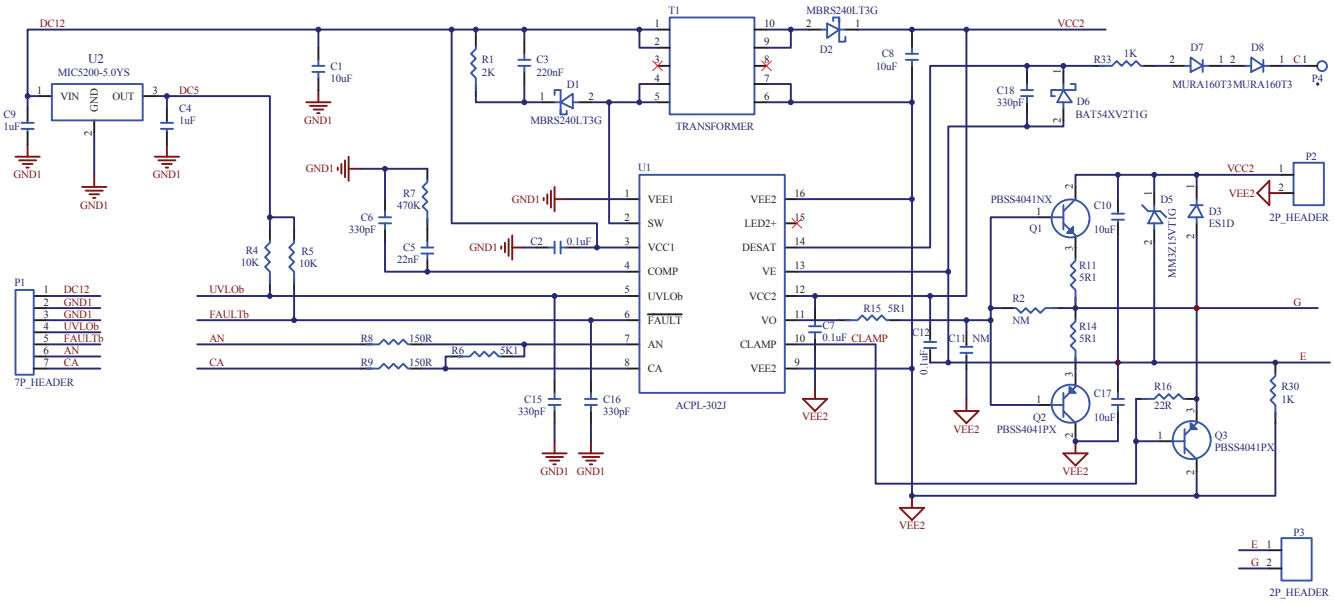

Figure 3. Schematics of ACPL-302J Evaluation Board

Practical Connections of the evaluation board (2 Evalboards needed)

Using IGBT for Actual Inverter Test (Half-bridge Inverter configuration plus load are as shown)

1. To drive top Inverter IGBT1 at collector, gate and emitter points ,respectively, connect the C pin at P4, G and E pins at P3 of the first eval board (Eval board 1).
2. Connect a +12V DC supply (PS1) across +12 V and GND1 terminals of P1. Check that a proper +20 V DC output voltage is obtained at P2 using a voltmeter.
3. Repeat Step 1 with a second eval board (Eval Board 2) and use it to drive bottom Inverter IGBT2.
4. Repeat Step 2 by connecting the same PS1 to +12V and GND1 terminals of P1 on the second eval board (Eval Board 2) .
5. To drive the top inverter IGBT Q1, connect a 10 kHz 5 V PWM input signal (at < 50% duty) from a microcontroller across the AN and CA pins of P1 of Eval Board 1.
6. To drive the bottom inverter IGBT Q2 , connect an inverted PWM input signal w.r.t. Step 5 from the same microcontroller across the AN and CA pins of P1 of Eval Board 2.
7. To monitor the waveforms, use a multichannel digital oscilloscope at the following points:
   a. Input PWM signal across the AN and CA pins of P1.
   b. V_G representing the gate drive voltage of ACPL-302J (U1) at G (gate) pin of IGBT1. Monitoring of this signal must be done through a HV differential probe.
   c. Desat signal at pin 14 of U1 representing the Desat voltage of IGBT1's C (collector) pin during turn-on. Monitoring of this signal must be done through a HV differential probe.
   d. Miller Clamp voltage of IGBT1 at pin 10 of U1. Monitoring of this signal must be done through a HV differential probe.

   For monitored results, see "Output Measurement". Repeat Step 7 for Eval Board 2.
8. Once the normal operating outputs are confirmed, the protection features of ACPL-302J can be checked:
   a. With a HV differential probe at V_O, monitor the /UVLO status signal when V_{out} is briefly shorted.
   b. With two HV differential probes at V_G and Desat voltage (at pin 14 of U1), monitor the /Fault status signal when C pin of P4 is briefly disconnected from IGBT1's Collector.

   For protection test results, see "Output Measurement".

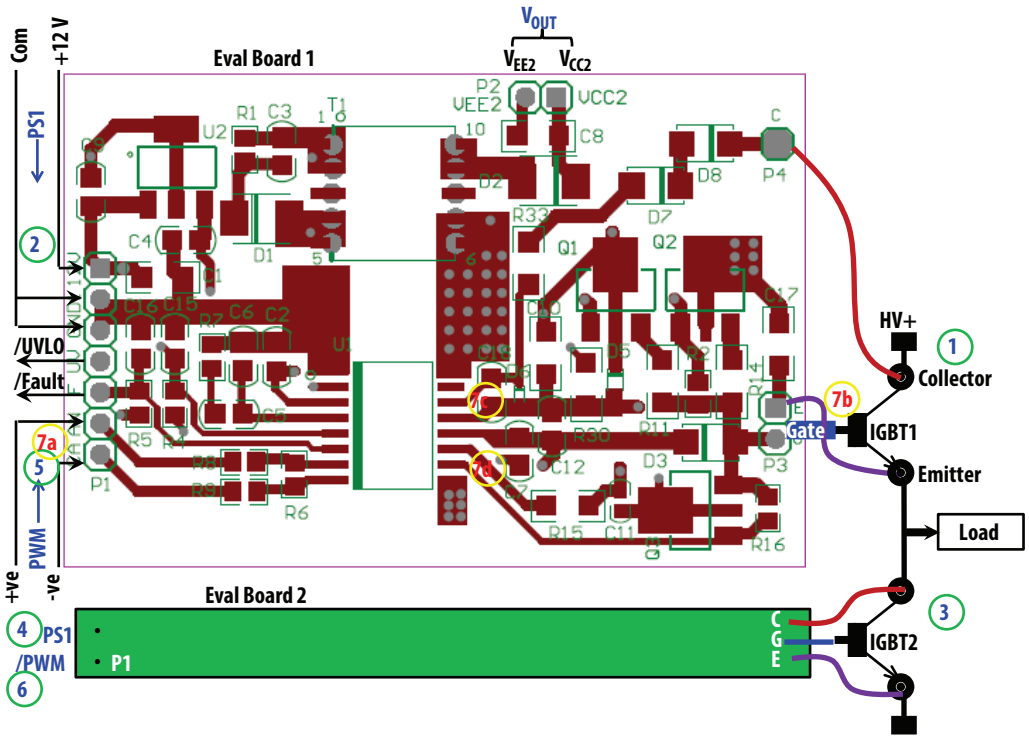

Figure 4. Connection of Evaluation Boards in Actual Applications to Drive Inverter IGBTs

Application Circuit Description

ACPL-302J is an isolated Gate Driver that provides 2.5 A output drive current, with integrated voltage mode controller for DC/DC conversion. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving of IGBT, with ratings up to 1000 V/100 W. ACPL-302J is also designed to drive different sizes of buffer stage, which will make the class of IGBT scalable. ACPL-302J provides a single isolation solution suitable for both low and high power ratings of motor control and inverter applications. With just a properly designed pulse transformer (Avago has recommendations for 20 V 60 mA output transformers for 2500 V_{rms} and 3750 V_{rms} Hi-pot rated applications), the secondary driver-side DC supply can easily be obtained by using the integrated control signal.

Each ACPL-302J evaluation board, as shown in Figure 5, accommodates an ACPL-302J IC. The board is sufficient to drive an Inverter arm. This allows the designer to easily test the performance of gate driver in an actual application solution. Operating the evaluation board requires just an inverter drive signal from the microcontroller, plus a common +12 V DC Supply (PS1) on the input side, and an isolated +20 V DC output will be generated on the driver side.

Once the input LED of ACPL-302J (through AN and CA pins on P1) is driven by a +5 V inverter drive signal at 10 mA current typically from the microcontroller, output at Pin 11 is activated with a positive pulse voltage and ready to drive the external IGBT's gate through a gate resistor R15 (5R1 Ω). Assuming that the voltage supply at V_{CC2} and V_{EE2} w.r.t. V_E (or E) are +15 V and -5 V, respectively, the maximum drive current is limited to 4 A peak (= $(V_{CC2} – V_{EE2})/R_G$). To drive the external IGBT directly without a buffer driver (if Q1 and Q2 removed), the drive current has to be limited to 2.5 A, the maximum output current limit of ACPL-302J. This is done by inserting a ½W 3R3 Ω resistor at R2.

By default, the eval board output at Pin 11 is designed to drive the external IGBT through a buffer driver Q1 (PBSS-4041NX) and Q2 (PBSS4041PX), and the output driving current is boosted up to 4 A with the ½W 5R1 resistors at R11 and R14 (R2 not mounted). If needed, R11 and R14 can be adjusted (lower), and Q1 and Q2 are capable of output driving current up to 12 A.

ACPL-302J is a smart gate driver with many integrated features such as:

a. IGBT collector desaturation fault protection to protect against overload as well as short circuit.

b. Active Miller Clamp to prevent false turn-on due to Miller current effect.

c. UVLO to prevent premature output turn-on due to insufficient supply voltage at V_{CC2}

d. Voltage mode DC/DC controller with error amplifier compensations

Desat Fault Protection

For normal output loading during IGBT turn-on, the collector saturation voltage should fall below 5 V (= $V_{DESAT} - I_{constant} * R_{DESAT} - V_F$), where:

V_{DESAT} = 7 V typical (protection threshold of Desat voltage)

$I_{constant}$ = 0.9 mA of internal constant current source

R_{DESAT} = 1 kΩ at R33

V_F = 1 V (typical) of D7 for MURA160T3 at 1 mA

During overload or short circuit, the collector saturation voltage is higher than 5 V and the detected voltage at the Desat Pin 14 of U1 will be higher than 7 V. This will trigger output shutdown (output soft shutdown will be initiated and at the same time the /FAULT feedback Pin 6 will be pulled Low to inform the external microcontroller that there is a Fault happening at the IGBT power switch) to turn off the IGBT to protect it from damage. So the IGBT should be selected such that its collector saturation voltage during turn-on under full load condition is less than 5 V. If the collector saturation voltage during full load is too low, e.g., < 3 V, then adding a 2 V Zener at D8 (reversed mounting) will help to provide proper overload or short circuit protection.

For other design criteria for Desat protection, refer to the application notes.

Note:

As Desat diode's breakdown voltage is rated at only 600 V, IGBT should be selected with V_{CES} < 600 V, and maximum HV+ voltage plus flyback voltage of load inductor must be < 600 V. For higher voltage-rated IGBT, the jumper at D8 must be replaced with another blocking diode commensurating with the required voltage.

Active Miller Clamp to Prevent False Turn-On by Miller Effect

Every IGBT used will have a junction capacitance between collector and gate (or Miller capacitance). Ideally, this capacitance has to be as small as possible, but it can never be eliminated. This Miller capacitance might allow transient current (by high dV/dt) to flow from collector to gate and cause the gate voltage to rise during gate turn-off. If this sudden surge of gate voltage is higher than the gate threshold voltage (usually 2 V ~ 5 V), then there might be a false IGBT turn-on.

To prevent this from happening, the IGBT gate voltage is monitored (by connecting it to the Clamp Pin 10 of U1) during turn-off. During turn-off, the gate voltage, as monitored, is pulled Low and it will drop from V_{CC2} level to V_{EE2} level. As soon as this gate voltage level drops below 2 V w.r.t. V_{EE2}, an internal clamp is activated to shunt the Clamp Pin 10 to Pin 9, which is at V_{EE2} level. By doing so, it ensures that the gate voltage has no chance of getting over 2 V again during the entire IGBT off duration. When Pin 10 is monitored, a sudden dip in voltage from 2 V (typically) to 0 V immediately will be observed, to confirm that the active Miller Clamp is working properly.

Note:

Since active Miller clamp is built-in to this ACPL-302J device, negative supply is not needed and V_E and V_{EE2} can be shorted.

The selected on-board Active Miller Clamp PNP transistor Q3 (PBSS4041Z) can sink a Miller current up to 10 A peak.

Preventing Premature Output Turn-On Through the Use of UVLO

If IGBT is allowed to turn-on immediately after gate voltage just crosses the threshold voltage (typically 2 V ~ 5 V), the collector emitter junction is operating at the linear region if gate voltage stays at this low turn-on threshold. This will cause high voltage built-up across the very same junction, especially when the load is high. The conduction power dissipation (= load current * junction voltage) of the device will be very high and IGBT can be damaged if this power dissipation is higher than the allowable limit. To prevent this high power dissipation from occurring, the designer has to ensure that the turn-on of the IGBT is prohibited until the gate voltage has reached a certain level at which collector saturation can be achieved, and usually this calls for a gate voltage to be >12 V. This is done by including a UVLO circuit inside the ACPL-302J device. This built-in UVLO circuit monitors the supply voltage at V_{CC2} w.r.t. V_E, and output stays low until V_{CC2} voltage crosses the UVLO+ threshold, typically 12.5 V. The UVLO protection circuit can be checked by varying V_{CC2} supply voltage higher than or lower than the UVLO+ or UVLO- threshold voltage, respectively. When V_{CC2} supply voltage is lower than the UVLO- threshold, the /UVLO status at Pin 4 of U1 should send out a low level, w.r.t. GND1.

Note:

Minimum V_{CC1} voltage level for ACPL-302J's internal DC/DC controller to start operation is 6 V.

Voltage Mode DC/DC Controller with Error Amplifier Compensations

ACPL-302J is the first gate driver optocoupler in the industrial market that can generate its own isolated DC power supply at the secondary side from a fixed input DC power supply at the primary side. This can come in handy when the designer has only a low voltage (8 V ~15 V) supply available but needs to drive inverter IGBTs at the high voltage side. This is achieved by the integrated 60 kHz pulse width modulation controller to drive a small external transformer for the DC/DC power conversions. With a properly designed flyback transformer, the isolated DC power supply can be ≥15 V, which is needed to drive an IGBT.

The evalboard has a built-in (by default) 2500 V_{ac} per minute hi-pot rated flyback transformer T1 and the output is designed to provide 20 V (across V_{CC2} and V_{EE2}) at full load of 60 mA. 3750 V_{ac} per minute hi-pot rated flyback transformer option is also available upon request.

When +12V is supplied across Pin 1 and Pin 2 (and/or Pin 3) of P1, the DC/DC controller of ACPL-302J (U1) starts to operate by driving the primary winding of flyback transformer T1 through the SW Pin 2 (see Figure 3) at 60 kHz duty cycle regulated pulse width signal. A regulated DC output voltage of +20 V ± 5% is obtained across P2. The feedback loop for regulation is through the V_{CC2} Pin 12, and compensation networks of C5, C6 and R7 are provided for loop compensation for stability operations. C6 and R7 forms a high frequency pole to compensate for the ESR zero from C8, while R7 and C5 forms a lower frequency zero to compensate for the load pole caused by C8 and load resistance. These compensation networks have been properly designed to work with the eval board design. Customers will need to redesign these compensation networks if they choose to use their own flyback transformer design as well as output capacitance.

A clamping network consists of D1, R1 and C3 is designed to clamp the flyback switching voltage spikes caused by leakage inductance of T1 to within 18 V above V_{CC1}.

D5 (15 V Zener) and R30 (1 kΩ) are provided to clamp V_{CC2} voltage to 15 V with respect to V_E at emitter point of IGBT. As a result, the voltage at V_{EE2} will be close to -5 V w.r.t V_E. This negative V_{EE2} voltage provides a faster turn-off for the driven IGBT (thought not required as the device ACPL-302J comes with active Miller Clamp function).

Notes:
1. U2 is a +5 V regulator to provide a 5 V supply rail from V_{CC1} for /UVLO and /Fault feedback pull-up during normal operations.
2. As can be seen on the board, the isolation circuitry (at the far left) is easily contained within a small area while maintaining adequate spacing for good voltage isolation and easy assembly.

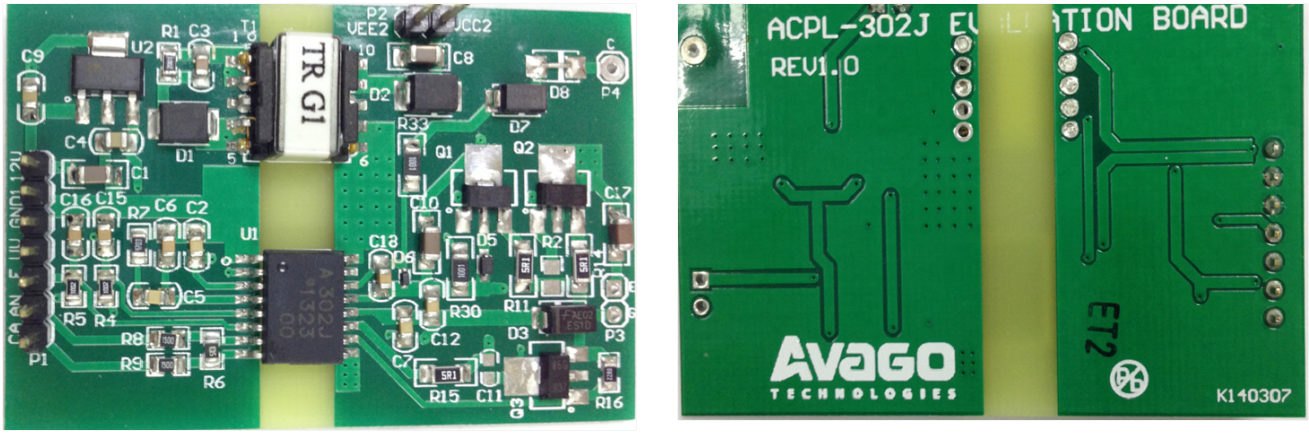

Figure 5. Top and Bottom Views of ACPL-302J Evaluation Board

Output Measurement

A sample of Input signal and various output waveforms are captured and shown in Figure 6, during IGBT gate turn-off and turn-on instants. Default setup connection is used but with external IGBT mounted. The IGBT used has a gate capacitance equivalent to 10 nF. It is observed that during normal working condition, the Desat pin voltage is much less than 7 V, and no Fault occurs.

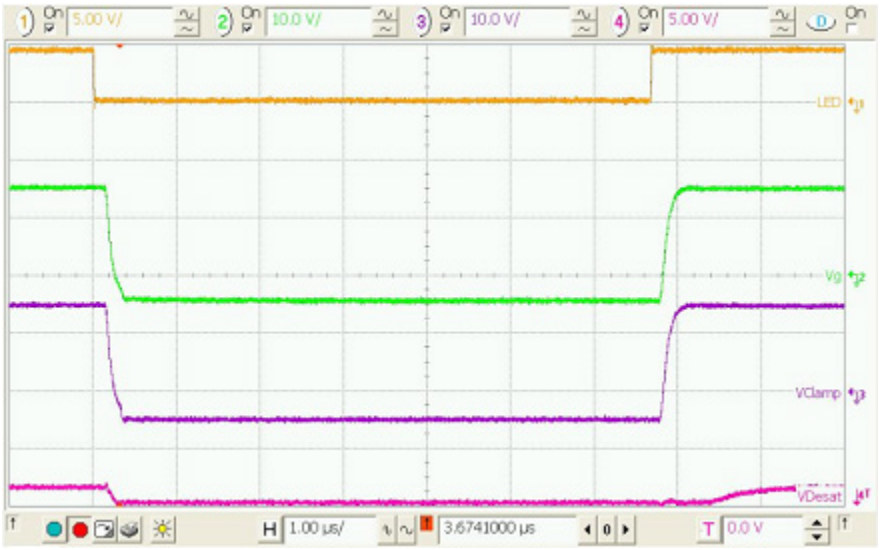

Figure 6. ACPL-302J Input and Output plus Protection Signal Waveforms

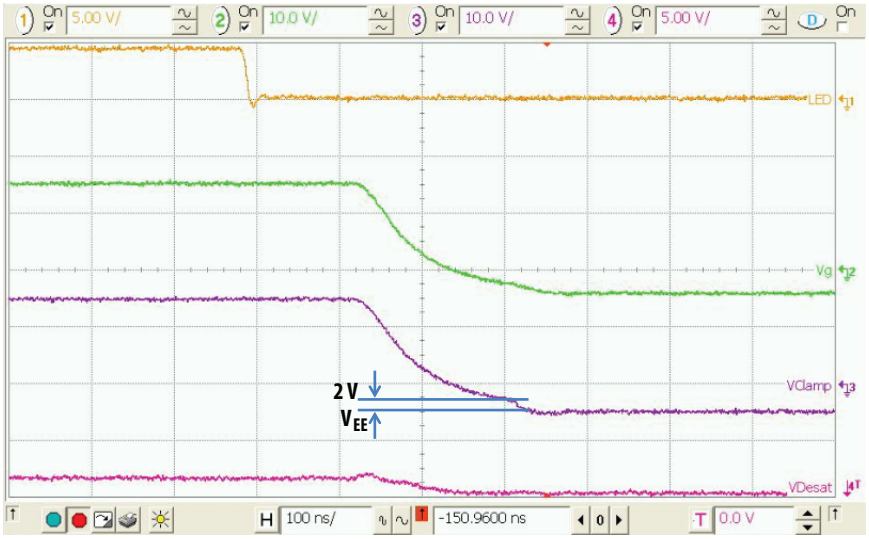

Figure 7. Exploded View of Active Miller Clamp Pin Waveform at Normal Turn-Off

Figure 7 is the exploded view of the Active Miller Clamp Pin 10 waveform during normal turn-off. It shows clearly that once the detected gate voltage drops below 2 V (typically), the gate voltage is shunt and clamped to 0 V w.r.t. V_{EE2} level during the entire turn-off duration, to ensure that the gate voltage has no chance of going above the turn-on threshold level again.

Figure 8 shows the actual Desat 7 V threshold detection that triggers the V_G output soft-shutdown as well as /Fault feedback pin voltage is pulled Low to inform the microcontroller that a fault has been detected.

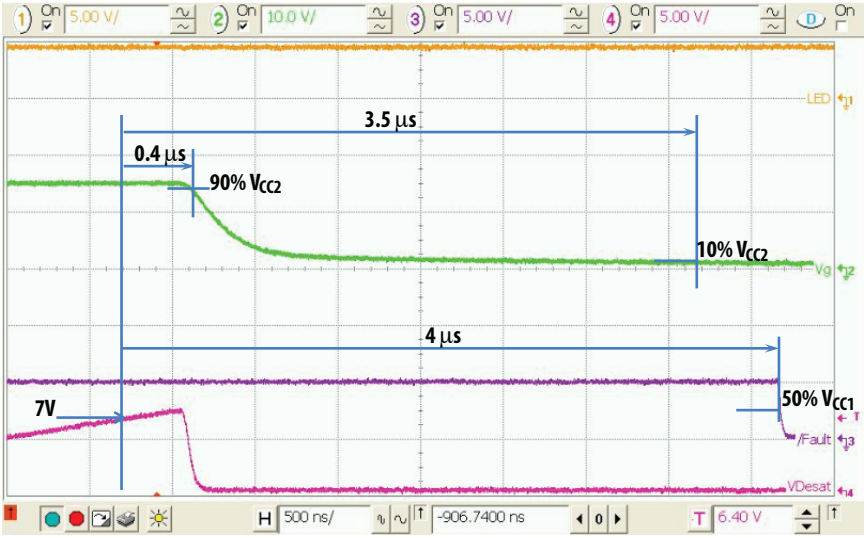

Figure 8. Desat Protection and Fault Feedback

Figure 9 shows that when V_{CC2} voltage sags below UVLO- level (between 10 V ~12.8 V) w.r.t. V_E, it triggers the UVLO protection and it shuts down the output V_O level and recovers after normal V_{CC2} voltage recovers above UVLO+ level (between 10.9 V ~ 13.8 V) w.r.t. V_E. The /UVLO pin voltage is also pulled low throughout the same duration to inform the microcontroller that a severe V_{CC2} level drop has happened.

Figure 9. UVLO Feedback

DC/DC Controller Operations

The following waveforms show switching waveform at SW Pin 2, together with +12 V DC_{in} and +20 V DC_{out} waveforms. Once DC_{in} voltage crosses the 6 V threshold, the DC/DC Controller starts operating and DC_{out} will be produced across V_{CC2} and V_{EE2} pins at P2. V_{out} is regulated at +20 V through the internal 60 kHz voltage mode pulse width modulation controller.

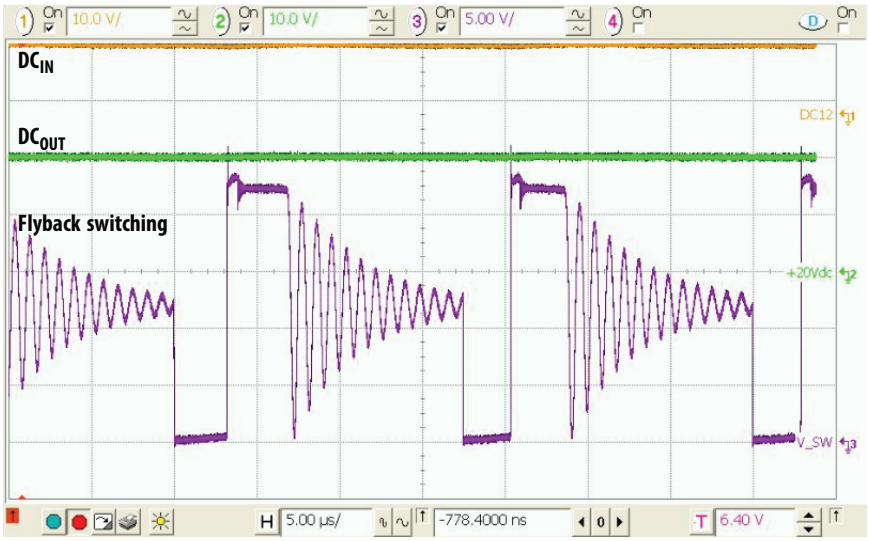

Figure 10. DC/DC Controller Waveforms

In conclusion, with these sophisticated IGBT gate driving and driver protection schemes built-in, ACPL-302J is well suited for modern IGBT applications such as Motor Control and Voltage inverters.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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