

ACPL-K71T, ACPL-K72T, ACPL-K74T, ACPL-K75T

Automotive High-Speed Low-Power Digital Optocouplers with R²Coupler Isolation and AEC-Q100 Grade 1 Qualification

Description

The ACPL-K71T and ACPL-K72T are high-speed digital CMOS optocouplers package suitable for emerging electric vehicle applications. The ACPL-K74T and ACPL-K75T are dual-channel equivalents of the ACPL-K71T and ACPL-K72T, respectively. All products are available in the stretched SO-8 package outline, designed to be compatible with standard surface mount processes.

ACPL-K71T and ACPL-K74T are high-speed mode with fastest propagation delay (maximum 35 ns at I_F = 10 mA) while ACPL-K72T and ACPL-K75T are low-power mode with lowest LED drive current of 4 mA for standard digital isolation switching.

Each channel of the digital optocoupler has a CMOS detector IC with an integrated photodiode, a high-speed trans-impedance amplifier, and a voltage comparator with an output driver.

The Broadcom[®] R²Coupler[™] provides with reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high-temperature industrial applications.

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that might be induced by electrostatic discharge (ESD).

Features

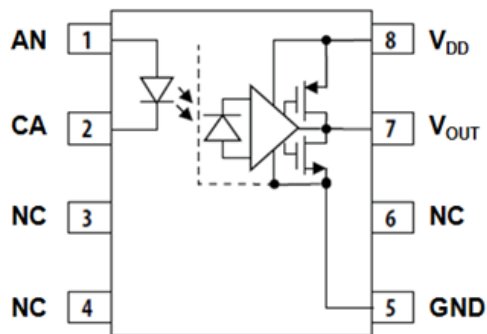
- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive wide temperature range: -40°C to 125°C
- High temperature and reliability, high-speed digital interface for automotive applications
- 5V CMOS compatibility
- 40 kV/μs common-mode rejection at V_{CM} = 1000V typ.
- Low propagation delay:
 - ACPL-K71T, ACPL-K74T: 25 ns typ. @ I_F = 10 mA
 - ACPL-K72T, ACPL-K75T: 60 ns typ. @ I_F = 4 mA
- Worldwide safety approval:
 - UL 1577 approval, 5kV_{RMS} /1 min.
 - CSA approval
 - IEC/EN/DIN EN 60747-5-5

Applications

- CAN Bus and SPI communications interface
- High-temperature digital/analog signal isolation
- Automotive IPM driver for DC-DC converters and motor inverters
- Power transistor isolation

Functional Diagrams

Figure 1: ACPL-K71T/ACPL-K72T



NOTE: The connection of a 0.1- μ F bypass capacitor between pins 5 and 8 is recommended.

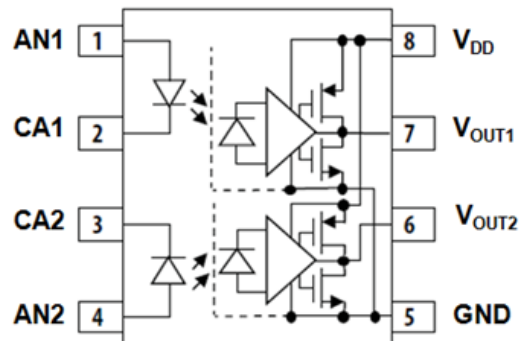
Table 1: Truth Table

LED	V _O
ON	LOW
OFF	HIGH

Table 2: Pin Assignments for ACPL-K71T/ACPL-K72T

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	AN	Anode	5	GND	Ground
2	CA	Cathode	6	NC	No Connection
3	NC	No Connection	7	VOUT	Output
4	NC	No Connection	8	VDD	Power Supply

Figure 2: ACPL-K74T/ACPL-K75T



NOTE: The connection of a 0.1- μ F bypass capacitor between pins 5 and 8 is recommended.

Table 3: Pin Assignments for ACPL-K74T/ACPL-K75T

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	AN	Anode	5	GND	Ground
2	CA	Cathode	6	NC	No Connection
3	NC	No Connection	7	VOUT	Output
4	NC	No Connection	8	VDD	Power Supply

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	UL 5000 VRMS/ 1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-K71T	-000E	Stretched SO-8	X	—	X	—	80 per tube
	-060E		X	—	X	X	80 per tube
	-500E		X	X	X	—	1000 per reel
	-560E		X	X	X	X	1000 per reel
ACPL-K72T	-000E	Stretched SO-8	X	—	X	—	80 per tube
	-060E		X	—	X	X	80 per tube
	-500E		X	X	X	—	1000 per reel
	-560E		X	X	X	X	1000 per reel
ACPL-K74T	-000E	Stretched SO-8	X	—	X	—	80 per tube
	-060E		X	—	X	X	80 per tube
	-500E		X	X	X	—	1000 per reel
	-560E		X	X	X	X	1000 per reel
ACPL-K75T	-000E	Stretched SO-8	X	—	X	—	80 per tube
	-060E		X	—	X	X	80 per tube
	-500E		X	X	X	—	1000 per reel
	-560E		X	X	X	X	1000 per reel

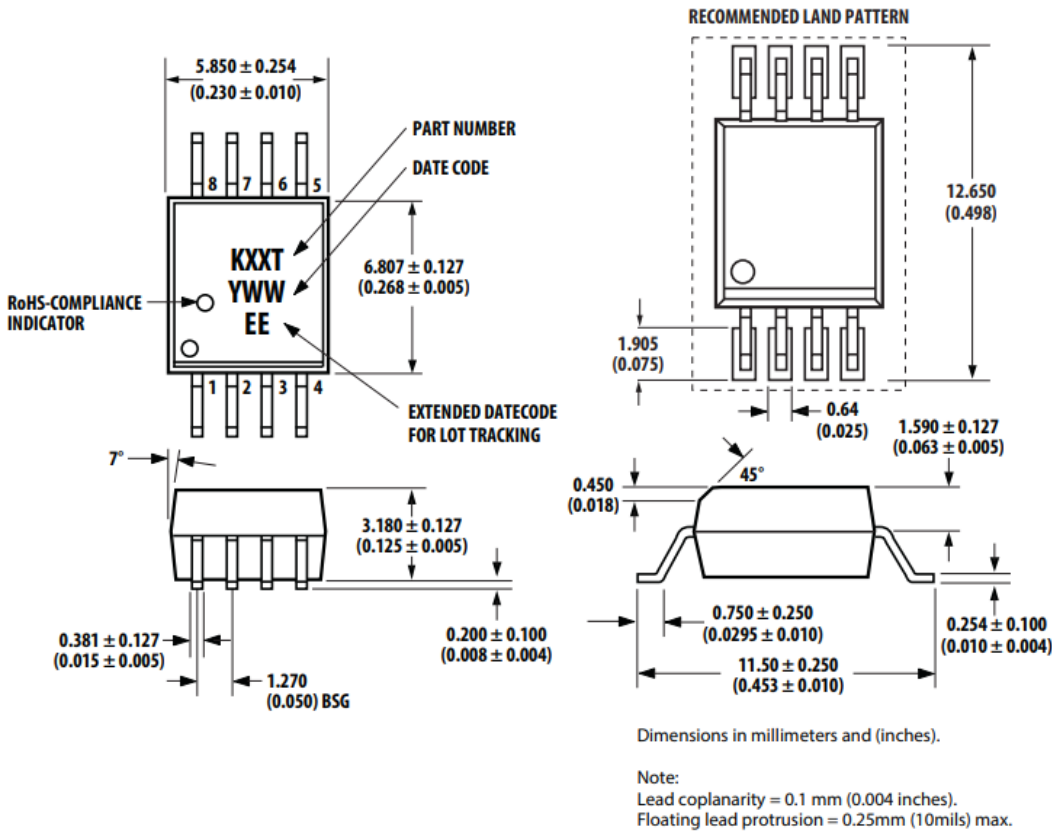
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-K71T-560E to order product of SSO-8 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Dimensions (Stretched-SO8)



Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Use non-halide flux.

Regulatory Information

The ACPL-K71T, ACPL-K72T, ACPL-K74T and ACPL-K75T are approved by the following organizations:

Table 4: Regulatory Information

UL	Approval under UL 1577, component recognition program up to $V_{ISO} = 5 \text{ kV}_{RMS}$.
CSA	Approval under CSA Component Acceptance Notice #5.
IEC/EN/DIN EN 60747-5-5	Approval under IEC/EN/DIN EN 60747-5-5.

Insulation and Safety-Related Specifications

Parameter	Symbol		Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)	—	IIIa	—	Material Group (DIN VDE 0109)

IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristic (Option 060 Only)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 For rated mains voltage $\leq 600 V_{rms}$ For rated mains voltage $\leq 1000 V_{rms}$	I-IV I-III	—	—
Climatic Classification	—	40/125/21	—
Pollution Degree (DIN VDE 0110/1.89)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{PEAK}
Input to Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ s, Partial Discharge < 5 pC	V_{PR}	2137	V_{PEAK}
Input to Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$, Type and sample test, $t_m = 10$ s, Partial Discharge < 5 pC	V_{PR}	1824	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage, $t_{inl} = 60$ s)	V_{IOTM}	8000	V_{PEAK}
Safety Limiting Values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	$^{\circ}C$
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S , $V_{IO} = 500V$	R_S	109	Ω

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Test Conditions
Storage Temperature	T _S	-55	130	°C	—
Ambient Operating Temperature	T _A	-40	125	°C	—
Supply Voltages	V _{DD}	0	6.5	V	—
Output Voltage	V _O	-0.5	V _{DD} + 0.5	V	—
Average Forward Input Current	I _F	—	20.0	mA	—
Peak Transient Input Current	I _{F(TRAN)}	—	1	A	≤1-μs Pulse Width, 300 pps
		—	80	mA	≤1-μs Pulse Width, <10% Duty Cycle
Reverse Input Voltage	V _r	—	5	V	—
Input Power Dissipation	P _I	—	40	mW	—
Output Power Dissipation	P _O	—	30	mW	—
Lead Solder Temperature	—	260°C for 10s., 1.6 mm below seating plane			
Solder Reflow Temperature Profile	—	See Solder Reflow Temperature Profile Section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V _{CC}	3.0	5.5	V	—
Operating Temperature	T _A	-40	125	°C	—
Forward Input Current	I _{F(ON)}	4	15	mA	—
Forward Off State Voltage	V _{F(OFF)}	—	0.8	V	—
Input Threshold Current	I _{TH}	—	3.5	mA	—

Electrical Specifications

Over recommended temperature T_A = -40°C to 125°C, 3.0V ≤ V_{DD} ≤ 5.5V. All typical specifications are at T_A = 25°C, V_{DD} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
LED Forward Voltage	V _F	1.45	1.5	1.75	V	I _F = 10 mA, T _A = 25°C	—	—
		1.25	1.5	1.85	V	I _F = 10 mA		
V _f Temperature Coefficient	—	—	-1.5	—	mV/°C	—	—	—
Input Capacitance	C _{IN}	—	90	—	pF	—	—	—
Input Reverse Breakdown Voltage	BV _R	5.0	—	—	V	I _R = 10 μA	—	—
Logic High Output Voltage	V _{OH}	V _{DD} - 0.6	—	—	V	I _{OH} = -3.2 mA	6	—
Logic Low Output Voltage	V _{OL}	—	—	0.6	V	I _{OL} = 4 mA	5	—
Logic Low Output Supply Current (per channel)	I _{DDL}	—	0.9	1.5	mA	—	—	—
Logic High Output Supply Current (per channel)	I _{DDH}	—	0.9	1.5	mA	—	—	—

ACPL-K71T, ACPL-K74T High-Speed Mode Switching Specifications

Over recommended temperature $T_A = -40^{\circ}\text{C}$ to 125°C , $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$. All typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5\text{V}$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
Propagation Delay Time to Logic Low Output	t_{PHL}	—	25	35	ns	$V_{IN} = 4.5\text{V}$ to 5.5V , $R_{IN} = 390\Omega \pm 5\%$, $C_{IN} = 100\text{ pF}$, $C_L = 15\text{ pF}$, $V_{THL} = 0.8\text{V}$, $V_{TLH} = 80\%$ of V_{DD}	7,8,13	a,b,c
Propagation Delay Time to Logic High Output	t_{PLH}	—	25	35	ns	—	—	—
Pulse Width Distortion	PWD	—	0	12	ns	—	—	—
Propagation Delay Skew	t_{PSK}	—	90	15	ns	—	—	—
Output Rise Time (10% to 90%)	t_R	—	10	—	ns	—	—	—
Output Fall Time (90% to 10%)	t_F	—	10	—	ns	—	—	—
Common Mode Transient Immunity at Logic High Output	$ CM_H $	15	25	—	kV/ μs	$V_{IN} = 0\text{V}$, $R_{IN} = 390\Omega \pm 5\%$, $C_{IN} = 100\text{ pF}$, $V_{CM} = 1000\text{V}$, $T_A = 25^{\circ}\text{C}$	14	d
Common Mode Transient Immunity at Logic Low Output	$ CM_L $	15	25	—	kV/ μs	$V_{IN} = 4.5\text{V}$ to 5.5V , $R_{IN} = 390\Omega \pm 5\%$, $C_{IN} = 100\text{ pF}$, $V_{CM} = 1000\text{V}$, $T_A = 25^{\circ}\text{C}$	14	e

- t_{PHL} propagation delay is measured from the 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 0.8V of V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 80% level of the rising edge of the V_O signal.
- PWD is defined as $|t_{PHL} - t_{PLH}|$.
- t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
- CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
- CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

ACPL-K72T, ACPL-K75T Low-Power Mode Switching Specifications

Over recommended temperature $T_A = -40^{\circ}\text{C}$ to 125°C , $3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$. All typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5\text{V}$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
Propagation Delay Time to Logic Low Output	t_{PHL}	—	60	100	ns	$I_F = 4\text{ mA}$, $C_L = 15\text{ pF}$, $V_{THL} = 0.8\text{V}$, $V_{TLH} = 80\%$ of V_{DD}	9,10,11, 12,15	a,b,c
Propagation Delay Time to Logic High Output	t_{PLH}	—	35	100	ns	—	—	—
Pulse Width Distortion	PWD	—	25	50	ns	—	—	—
Propagation Delay Skew	t_{PSK}	—	—	60	ns	—	—	—
Output Rise Time (10% to 90%)	t_R	—	10	—	ns	—	—	—
Output Fall Time (90% to 10%)	t_F	—	10	—	ns	—	—	—
Common Mode Transient Immunity at Logic High Output	$ CM_H $	25	40	—	kV/ μs	LED Driving Circuit Fig.13, $V_{IN} = 0\text{V}$, $R1 = 350\Omega \pm 5\%$, $R2 = 350\Omega \pm 5\%$, $V_{CM} = 1000\text{V}$, $T_A = 25^{\circ}\text{C}$	16	d
Common Mode Transient Immunity at Logic Low Output	$ CM_L $	25	40	—	kV/ μs	LED Driving Circuit Fig.14, $V_{IN} = 04.5\text{V}$ to 5.5V , $R1 = 350\Omega \pm 5\%$, $R2 = 350\Omega \pm 5\%$, $V_{CM} = 1000\text{V}$, $T_A = 25^{\circ}\text{C}$	16	e

- t_{PHL} propagation delay is measured from the 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 0.8V of V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 80% level of the rising edge of the V_O signal.
- PWD is defined as $|t_{PHL} - t_{PLH}|$.
- t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
- CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
- CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

Package Characteristics

All typical at $T_A = 25^{\circ}\text{C}$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Notes
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{RMS}	$RH \leq 50\%$, $t = 1\text{ minute}$, $T_A = 25^{\circ}\text{C}$	a,b
Input-Output Resistance	R_{I-O}	—	1014	—	Ω	$V_{I-O} = 500\text{V dc}$	a
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	$f = 1\text{ MHz}$, $T_A = 25^{\circ}\text{C}$	a

- Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $> 6000V_{RMS}$ for 1 second.

Performance Plots Typical Logic Low Output Voltage vs. Logic Low Output

Figure 3: Typical Diode Input Forward Current Characteristic

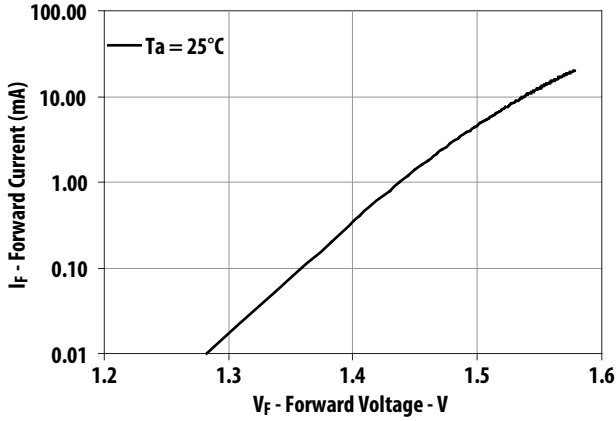


Figure 4: Typical Output Voltage vs. Input Forward Current

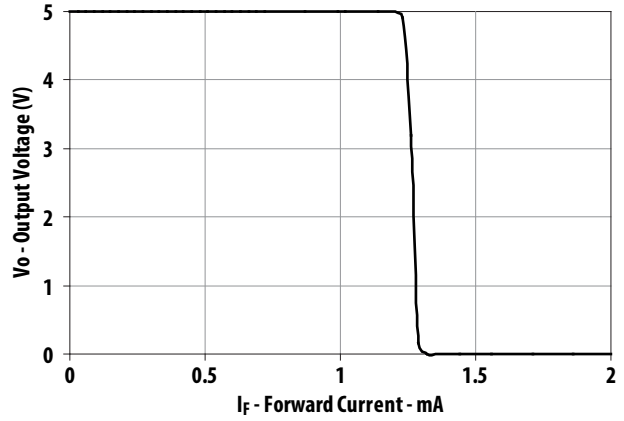


Figure 5: Typical Logic Low Output Voltage vs. Logic Low Output Current

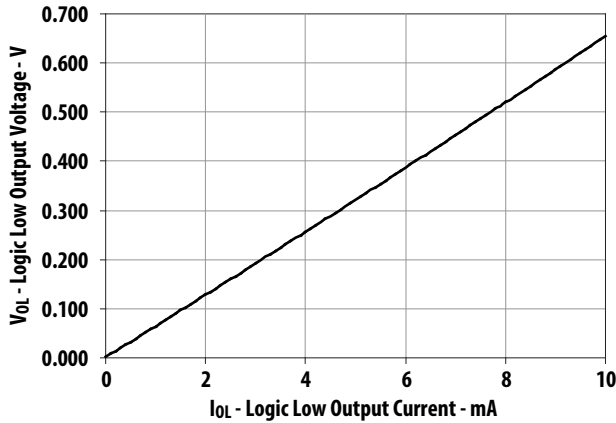


Figure 6: Typical Logic High Output Voltage vs. Logic High Output Current

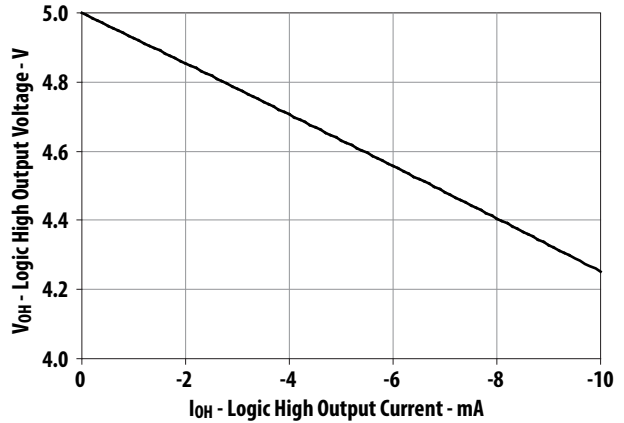


Figure 7: ACPL-K71T/K74T (High Speed) Typical Propagation Delay vs. Temperature

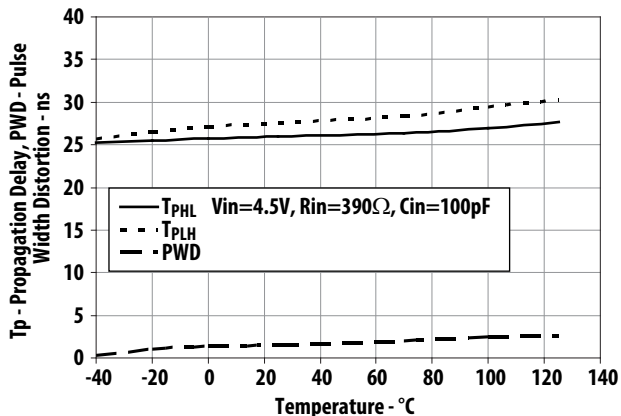


Figure 8: ACPL-K71T/K74T (High Speed) Typical Propagation Delay vs. Input Forward Current

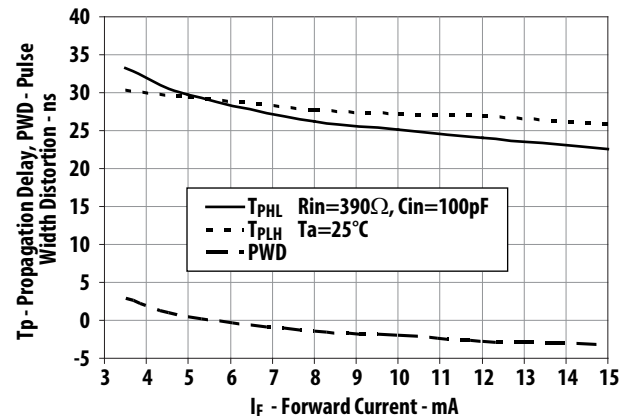


Figure 9: ACPL-K72T/K75T (5V) Typical Propagation Delay vs. Temperature

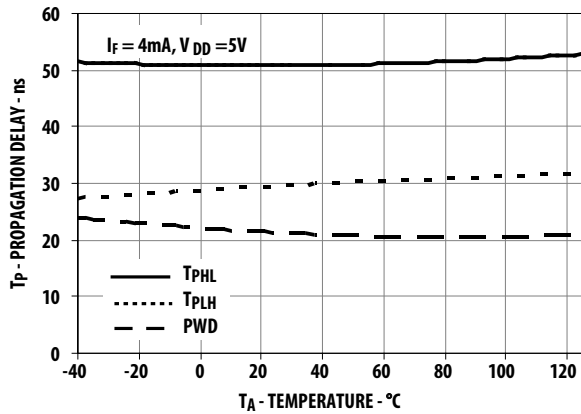


Figure 10: ACPL-K72T/K75T (5V) Typical Propagation Delay vs. Input Forward Current

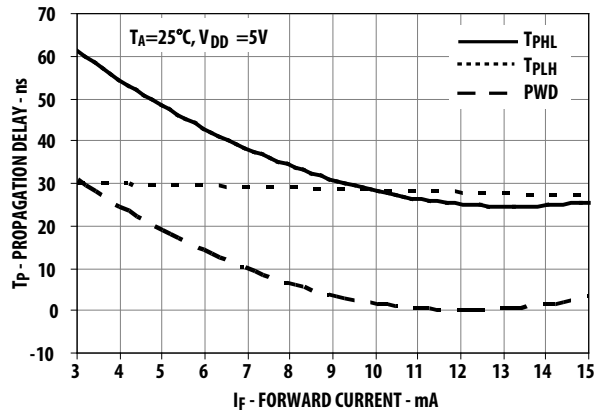


Figure 11: ACPL-K72T/K75T (3V) Typical Propagation Delay vs. Temperature

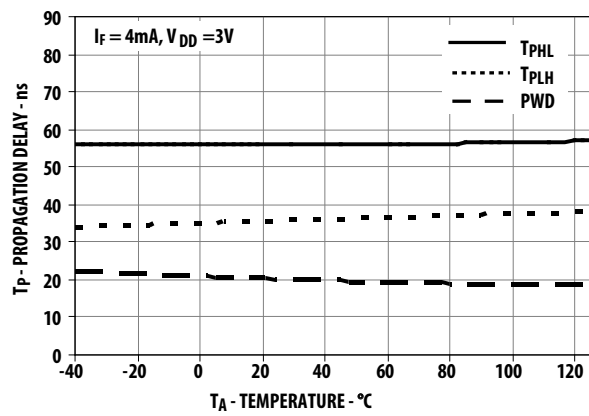
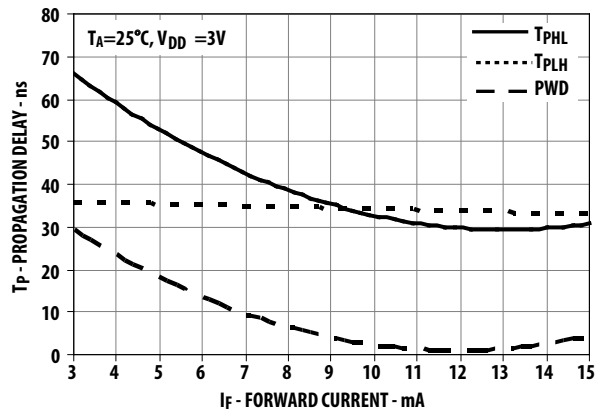


Figure 12: ACPL-K72T/K75T (3V) Typical Propagation Delay vs. Input Forward Current



ACPL-K71T/K74T High-Speed Mode

Figure 13: High-Speed Mode Switching Test Circuit and Typical Waveform

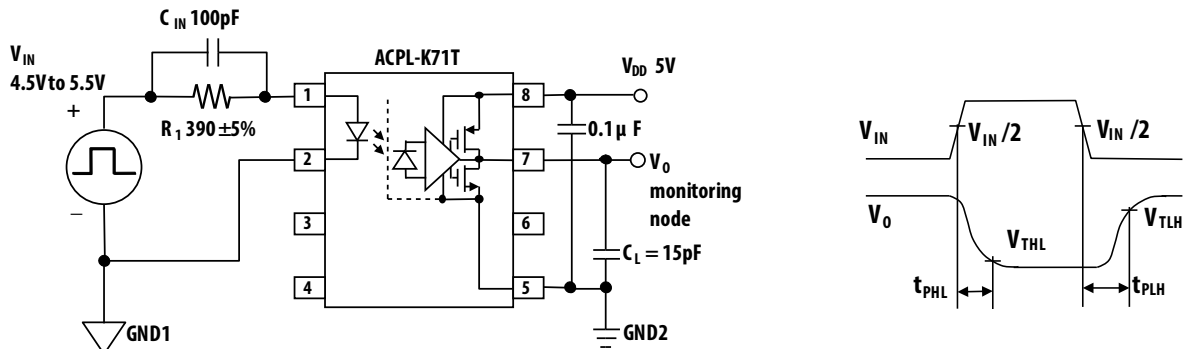
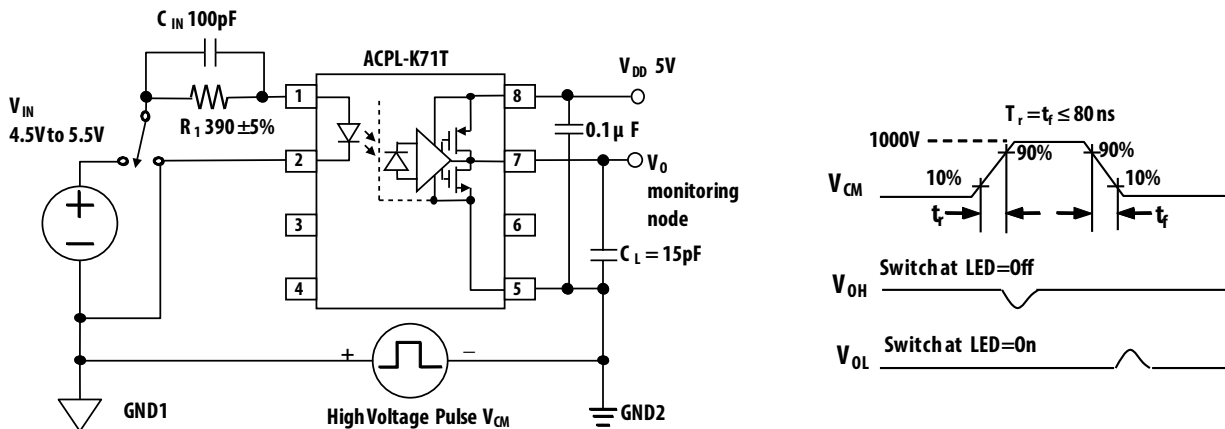


Figure 14: High-Speed Mode CMR Test Circuit and Typical Waveform



ACPL-K72T/K75T Low Power Mode

Figure 15: Low-Power Mode Switching Test Circuit and Typical Waveform

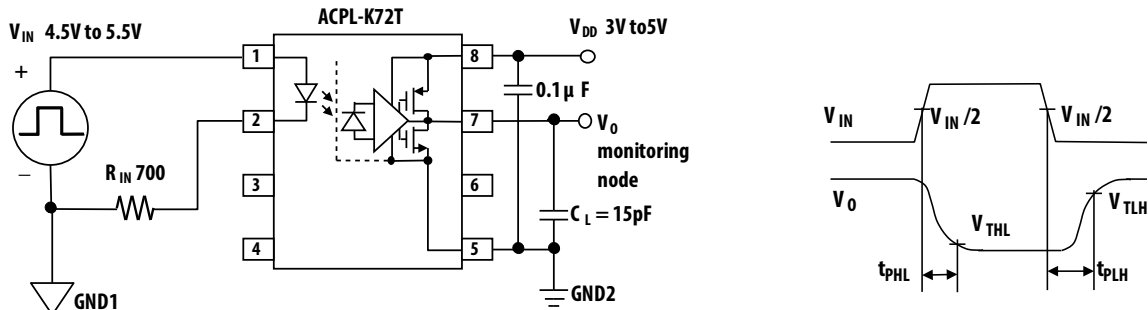
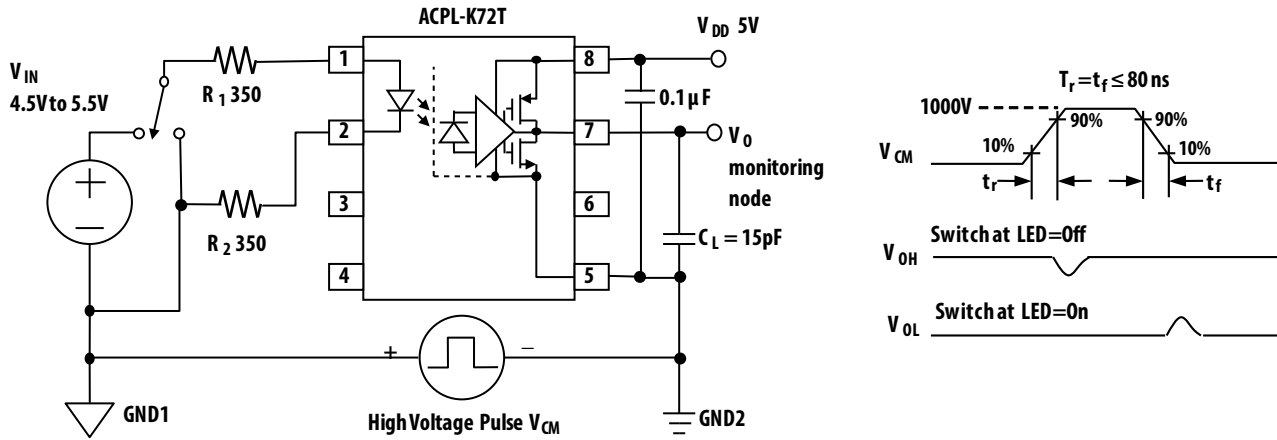
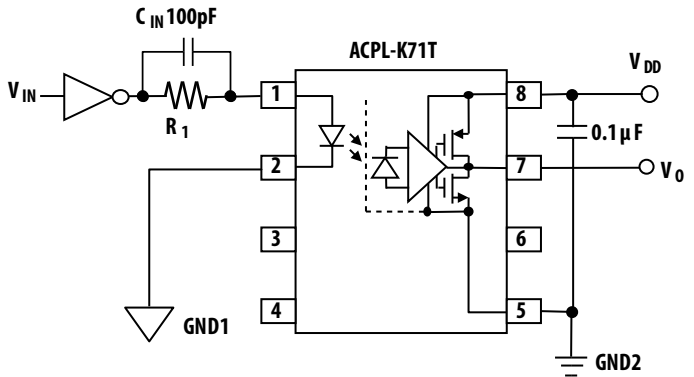


Figure 16: Low-Power Mode CMR Test Circuit



Recommended Application Circuits

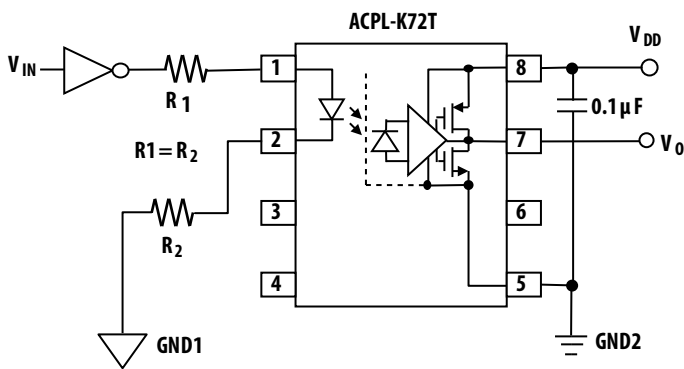
Figure 17: Recommended Application Circuit for ACPL-K71T/K74T High-Speed Performance



Truth Table

V _{IN}	LED	V _O
LOW	ON	LOW
HIGH	OFF	HIGH

Figure 18: Recommended Application Circuit for ACPL-K72T/K75T Low-Power Performance



Truth Table

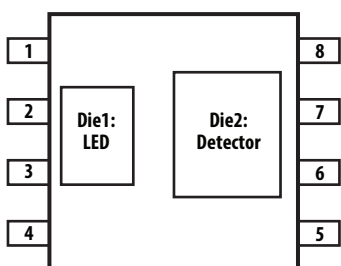
V _{IN}	LED	V _O
LOW	ON	LOW
HIGH	OFF	HIGH

Thermal Resistance Model for ACPL-K71T/K72T

The diagram of ACPL-K71T/K72T for measurement is shown in [Figure 19](#). Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 2 by 2 matrix for our case of two heat sources.

$$\begin{vmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{vmatrix} \times \begin{vmatrix} P_1 \\ P_2 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \end{vmatrix}$$

Figure 19: Diagram of ACPL-K71T/K72T for Measurement



R_{11}	:Thermal Resistance of Die1 due to heating of Die1 (°C/W)
R_{12}	:Thermal Resistance of Die1 due to heating of Die2 (°C/W)
R_{21}	:Thermal Resistance of Die2 due to heating of Die1 (°C/W)
R_{22}	:Thermal Resistance of Die2 due to heating of Die2 (°C/W)
P_1	:Power dissipation of Die1 (W)
P_2	:Power dissipation of Die2 (W)
T_1	:Junction temperature of Die1 due to heat from all dice (°C)
T_2	:Junction temperature of Die2 due to heat from all dice (°C)
T_a	:Ambient temperature (°C)
ΔT_1	:Temperature difference between Die1 junction and ambient (°C)
ΔT_2	:Temperature difference between Die2 junction and ambient (°C)
T_1	$= (R_{11} \times P_1 + R_{12} \times P_2) + T_a$
T_2	$= (R_{21} \times P_1 + R_{22} \times P_2) + T_a$

Measurement data on a low K board:

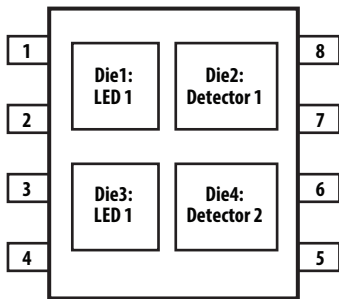
$$R_{11} = 160^\circ\text{C/W}, R_{12} = R_{21} = 74^\circ\text{C/W}, R_{22} = 115^\circ\text{C/W}$$

Thermal Resistance Model for ACPL-K74T/K75T

The diagram of ACPL-K74T/K75T for measurement is shown in [Figure 20](#). Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second, third and fourth die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4 by 4 matrix for our case of two heat sources.

$$\begin{vmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{vmatrix} \times \begin{vmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{vmatrix}$$

Figure 20: Diagram of ACPL-K74T/K75T for Measurement



- R_{11} :Thermal Resistance of Die1 due to heating of Die1 (°C/W)
- R_{12} :Thermal Resistance of Die1 due to heating of Die2 (°C/W)
- R_{13} :Thermal Resistance of Die1 due to heating of Die3 (°C/W)
- R_{14} :Thermal Resistance of Die1 due to heating of Die4 (°C/W)
- R_{21} :Thermal Resistance of Die2 due to heating of Die1 (°C/W)
- R_{22} :Thermal Resistance of Die2 due to heating of Die2 (°C/W)
- R_{23} :Thermal Resistance of Die2 due to heating of Die3 (°C/W)
- R_{24} :Thermal Resistance of Die2 due to heating of Die4 (°C/W)
- R_{31} :Thermal Resistance of Die3 due to heating of Die1 (°C/W)
- R_{32} :Thermal Resistance of Die3 due to heating of Die2 (°C/W)
- R_{33} :Thermal Resistance of Die3 due to heating of Die3 (°C/W)
- R_{34} :Thermal Resistance of Die3 due to heating of Die4 (°C/W)
- R_{41} :Thermal Resistance of Die4 due to heating of Die1 (°C/W)
- R_{42} :Thermal Resistance of Die4 due to heating of Die2 (°C/W)
- R_{43} :Thermal Resistance of Die4 due to heating of Die3 (°C/W)
- R_{44} :Thermal Resistance of Die4 due to heating of Die4 (°C/W)
- P_1 :Power dissipation of Die1 (W)
- P_2 :Power dissipation of Die2 (W)
- P_3 :Power dissipation of Die3 (W)

- P_4 :Power dissipation of Die4 (W)
 T_1 :Junction temperature of Die1 due to heat from all dice (°C)
 T_2 :Junction temperature of Die2 due to heat from all dice (°C)
 T_3 :Junction temperature of Die3 due to heat from all dice (°C)
 T_4 :Junction temperature of Die4 due to heat from all dice (°C)
 T_a :Ambient temperature (°C)
 ΔT_1 :Temperature difference between Die1 junction and ambient (°C)
 ΔT_2 :Temperature difference between Die2 junction and ambient (°C)
 ΔT_3 :Temperature difference between Die3 junction and ambient (°C)
 ΔT_4 :Temperature difference between Die4 junction and ambient (°C)
 $T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + T_a - (1)$
 $T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + T_a - (2)$
 $T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + T_a - (3)$
 $T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + T_a - (4)$

Measurement data on a low K board:

R ₁₁	R ₁₂	R ₁₃	R ₁₄	R ₂₁	R ₂₂	R ₂₃	R ₂₄	R ₃₁	R ₃₂	R ₃₃	R ₃₄	R ₄₁	R ₄₂	R ₄₃	R ₄₄
160	76	76	76	76	115	76	76	76	76	160	76	76	76	76	115

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