

Driver and Receiver Circuits for Avago SFH Series Plastic Fiber Components (PFC)



Application Note 5341

SFH Series Components

In addition to data transmission at 820 nm and 1300 nm, transmission at 650 nm is very popular because of cost-effective component availability. To meet the market demand, Avago offers specially designed transmitters and receivers for 650 nm transmission that feature a very easy fiber coupling mechanism. The cut fiber only has to be inserted into the plastic package, which has an aperture for standard 2.2 mm fibers. No connector-mounting is necessary. The Avago solution greatly reduces assembly costs.

There are two versions of each SFH component available – with and without a “Direct Fiber Connector Housing”. The housing allows easy coupling of an unconnectorized 2.2 mm polymer optical fiber by means of an axial locking screw. With the recommended locking torque of 15 cNm and the use of a suitable fiber, a pullout force of approximately 50 N can be reached. This force should be sufficient to support most applications, assuming the components are properly handled.

Fiber

Transmission suitable optical fibers, often called cables, are needed for information transport in the form of light pulses.

Avago offers plastic optical fiber (POF) for 650 nm applications. Typical fiber attenuation is approximately 0.2 dB/m at 25° C. For power budget calculations, fiber properties are an important factor. For example, high temperature and humidity increase fiber aging factors. Possible coupling losses are also an important factor for dimensioning the optical transmission link. All these factors, and even more, make proper fiber selection a critical factor in designing a safe and reliable transmission link.

Avago offers all the necessary fiber link components for a reliable and cost-effective data transmission system.

SFH Series Components

Product	Ordering Information	Feature	Max. Data Rate	Wave-length	Direct Fiber Connector Housing
SFH757	SP000063871	Transmitter Diode	100 MBd	650 nm	No
SFH757V	SP000063858	Transmitter Diode	100 MBd	650 nm	Yes
SFH250	SP000063866	Receiver (analogue out), Photodiode	100 MBd	650 nm	No
SFH250V	SP000063852	Receiver (analogue out), Photodiode	100 MBd	650 nm	Yes
SFH551/1-1	SP000063860	Receiver (digital out), Photodiode + TIA*	5 MBd	650 nm	No
SFH551/1-1V	SP000063855	Receiver (digital out), Photodiode + TIA*	5 MBd	650 nm	Yes

* Includes an integrated transimpedance amplifier (TIA) and Schmitt trigger

Transmitter Driver Circuits

The emitter is stimulated into emission by current flowing in the forward direction. There are several possibilities for the design of the driver circuit, which has the task of adjusting and stabilizing the current flow. Figure 1 shows the basic drive circuits. In the simplest example (Figure 1a), the LED is connected in series with a resistor "R" to the supply voltage "Vcc". The current "If" depends on the forward voltage "Vf" of the LED and the actual Vcc- and R-values.

$$I_f = (V_{cc} - V_f) / R$$

The diode may also be driven using the output transistor of a TTL gate or a separate driver transistor (Figure 1b), in which case the collector-emitter voltage should be taken into account. In this configuration the current passed by the transistor is given as:

$$I_f = (V_{cc} - V_f - V_{CE}) / R$$

In order to keep the current and thus the optical power constant, it is preferable to control the current flow (Figure 1c). For this example as with the others, it is necessary to ensure that sufficient voltage is provided.

How an efficient driver circuit for high-speed LEDs should be designed and under which conditions a LED works fine are described next. The following is a step-by-step guide for designing an LED driver circuit. Techniques for making LED drive circuits faster and more stable are also given.

All following statements refer to the typical behavior of Avago's SFH757 transmitter, and SFH551/1-1 and SFH250 receivers in combination with the described components, such as peripheral drivers. This application note should help to understand the typical behavior of LEDs like the SFH757 and photodiodes like the SFH250.

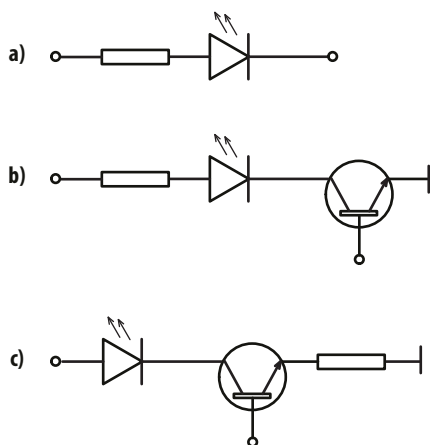


Figure 1. Basic LED driver circuits

The SFH757 and SFH757V are Class 1 Laser products (Protection Class III). Accessible Emissions Limits for the Laser Class 1 can be exceeded for forward current values larger than 80 mA and/or rated ambient temperature below 10°C. Compliance of the transmitter is to be verified in the end use application. The installation has to be carried out according to the installation instruction accompanying the product. Evaluated under consideration of hazard level measurements and calculations according to EN 60825-1:2007.

Please note that the absolute maximum forward current of the SFH757 is 50 mA DC.

Texas Instruments "SN7545BD" is a standard peripheral driver for high-current switching at high speeds – suitable for versatile applications in the optical transmission sector, especially for LED driver circuits. Either AND or NAND gates can be used. Generally only the availability, price and needed logic determines the logic type. In the following circuits an AND gate and the SFH757V as a 650 nm-LED transmitter are used.

Figure 2 shows a simple driver circuit with two smoothing capacitors (C1 = 100 µF and C2 = 10 µF) and a pull-up resistor of 1 kΩ for a stable high level on one of the two inputs of the used AND gate. Experience shows that in most applications a combination of 100 nF and 10 µF capacitors in parallel are sufficient for filtering.

The 50 Ω resistor, which is parallel installed to the Data In port reduces reflections between "Data source" (assumed source output impedance 50 Ω) and input port of the used AND gate.

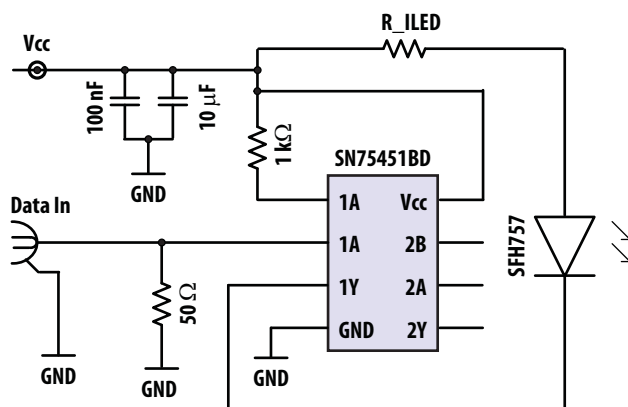


Figure 2. SFH757 characterization circuit

The resistor “R_ILED” is the only significant element in the drive circuit (Figure 2) that limits the current through the LED, apart from the gate’s output port. Depending on the actual gate used the voltage drop on the output port Vport should not be neglected.

$$I_{LED} = \frac{V_{CC} - V_f - V_{port}}{R_{ILED}}$$

The forward voltage value, Vf, of the LED depends on the desired LED current and on the temperature (Figure 3). This behavior must be taken into account for the calculations.

With an R_ILED of 100 Ω resistor installed in the characterization circuit, the following switching times are typical:

Rise Time (average) t _{rise} (10%..90%) [ns], T _A = 25° C, Figure 2	Fall Time (average) t _{fall} (90%..10%) [ns], T _A = 25° C, Figure 2
14	16

Higher LED current will increase the optical output power of the LED (Figure 4). The needed intensity of the emitted light depends on the optical receiver sensity and the link distance. Longer fiber cable has higher effective fiber attenuation.

Figure 5 shows the eye diagram of the opto/electrical converted output of the SFH757V at the end of a 1 m POF cable. The driver circuit of Figure 2 was used with a 100 Ω resistor for R_ILED and Vcc of 5.0 V.

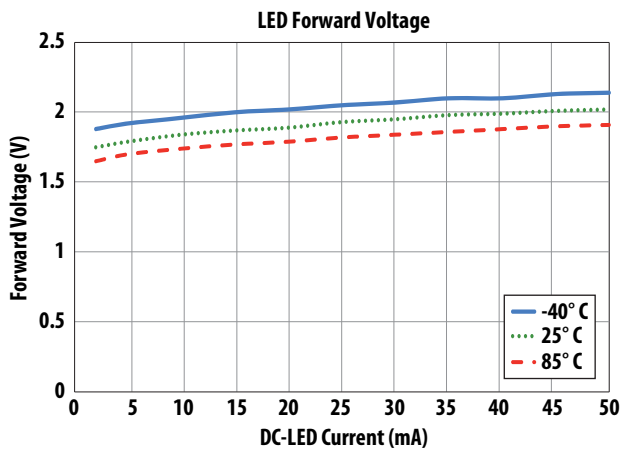


Figure 3. Typical forward voltage of the SFH757 transmitter

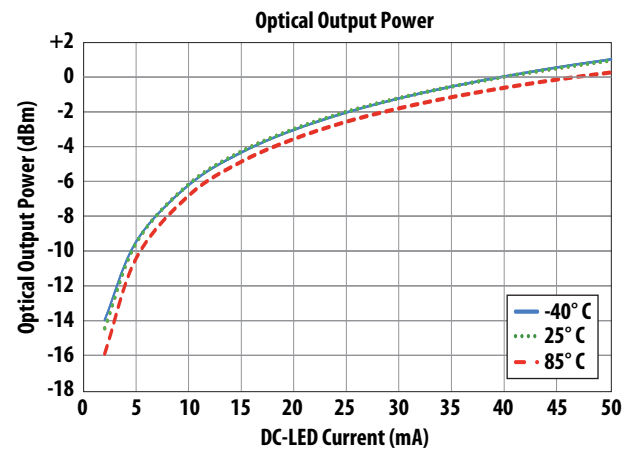


Figure 4. Typical SFH757 Optical output power

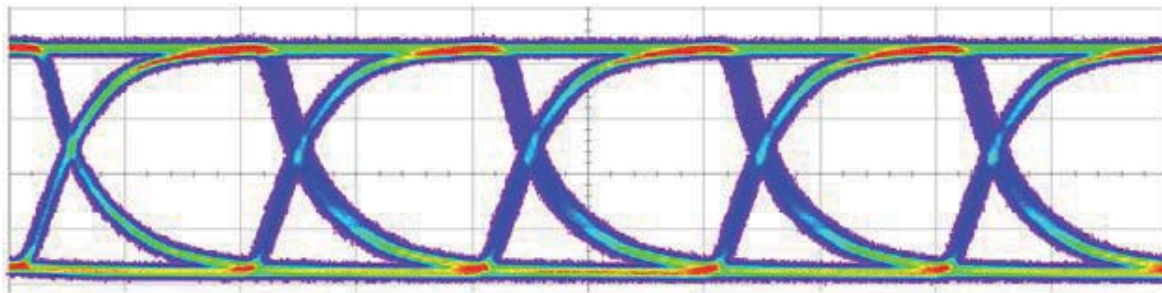


Figure 5. Typical SFH757 eye diagram at 25 MBd

Optimizing the driver circuit for a specific application requires environmental influences like temperature, humidity, link length and fiber type be considered and a specific calculation be done.

A simple example calculation shows the process. An optical output power of -3 dBm at an operating temperature of 25° C and at supply voltage of 5.0 V is needed. Figure 4 shows that an LED current of approximately 20 mA would be needed for an optical output power of approximately -3 dBm. The corresponding forward voltage to this LED current is approximately 1.9 V (Figure 3). Because of the relative small value of the voltage drop on the output port of the used AND gate, this influence can be ignored in most cases.

Note that a high LED current reduces the switching times significantly!

A higher ambient temperature will increase switching times. Both rise and fall time will increase with increasing temperature.

By switching the anode of the LED, as shown in Figure 6, LED fall time is reduced. This results from the clamping effect of the semiconductors.

If a 100 Ω resistor for R_LED is used, the following switching times are typical:

Rise Time (average) t _{rise} (10%..90%) [ns], T _A = 25° C, Figure 6	Fall Time (average) t _{fall} (90%..10%) [ns], T _A = 25° C, Figure 6
14	6.5

This improvement of fall time has no influences on the rise time of the LED and is at the expense of power consumption, therefore it is only partially suitable. The total current consumption of this driver circuit with an input pattern of PRBS2^14-1 is almost double that of the circuit shown in Figure 2, but therefore the Vcc is loaded evenly.

For transmission quality both rise and fall times should have similar values. Therefore the rise time must be improved. This can be realized by a certain combination of RC elements and with faster peripheral drivers, such as Fairchild Semiconductor's "74ACTQ00". ACT stands for "Advanced CMOS TTL" and should be preferred over the less optimized "HCT" versions (High speed CMOS TTL).

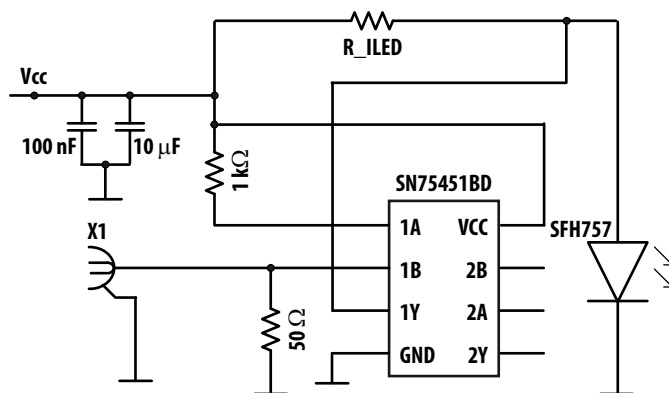


Figure 6. Modified LED-driver circuit for faster fall time

LED Drivers with NAND Gates

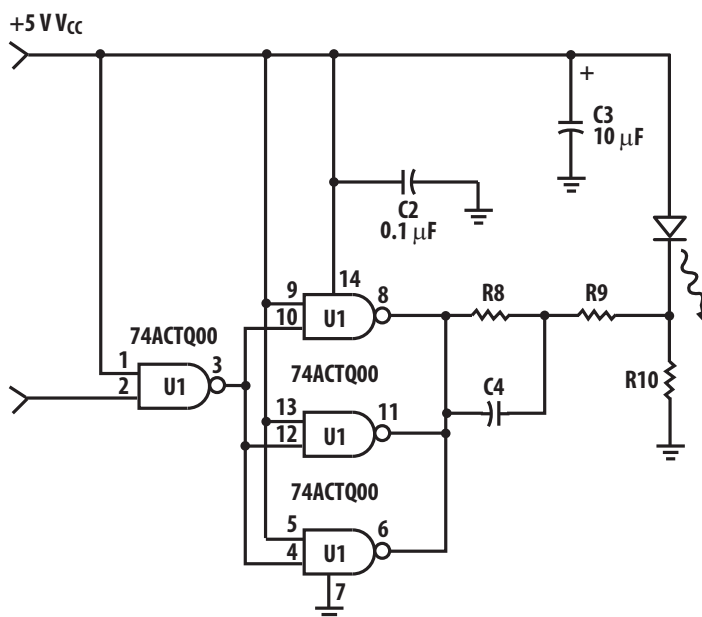
For data rates up to 100 MBd the switching times need further improvement and both values should be closer together. The circuit shown in Figure 7 is one possible way to design an LED driver for the Avago 100 MBd SFH757 transmitter. A quad 2-input NAND gate, 74ACTQ00, is used because of its switching times, which are lower than the switching times of the SN75451BD AND gate.

This is a very cost-effective and often used circuit for high-speed applications. It is possible to realize simple peaking with this circuit. The 74ACT-logic gates can be used to implement a shunt drive configuration to current-modulate the LED. An LED current up to 50 mA DC is typical to drive the SFH757. Ordinary bipolar TTL gates generally do not have sufficient capability to sink and source 50 mA DC. A simple high-speed LED driver can be constructed by connecting the active output of the 74ACT logic to the LED, as shown in Figure 7.

The formulas beside the recommended driver circuit for high data rates (Figure 7) are based on empirical values. The "If" value represents the average LED current during transmission (data input: PRBS $2^{14}-1$). The results of these calculations are only approximate values and should be seen as a "first trial" on the way to a completely optimized driver circuit specifically designed for the current application. The calculated resistor values of "R10", "R9" and "R8" are theoretical values, depending on the available resistor values. The final resistor values should be chosen greater than or equal to the calculated. This ensures that a higher LED current is not used. The final value for C4 should be chosen less than or equal to the theoretical value; otherwise the peaking effect is too strong, and the mean peak current level could be to high.

To hold the source load on a low level the electrical data out of the pattern generator is connected to the first NAND gate of the "74ACTQ00" IC. The output of this gate is connected to three other gates that share the load of the main part of the LED current. To reduce the switching times of the LED, especially the rise time, a more efficient circuit with RC-components must be designed, as shown in Figure 7. The RC combination (R8, C4 and R9) is called a "peaking circuit" because of the typical behavior of this combination – generating a temporary peak current. To improve the switching times further, a quiescent LED current is helpful. For this reason resistor R10 is used. With it, the LED emits light, even when there should be a "Light OFF" condition. The result is a DC load to the optical receiver because of the permanent light emitting of the LED, but this helps to reduce the response time. An offset compensation could be needed for the receiver circuit. The simplest way would be a coupling capacitor placed at the data output.

The total current consumption of the example circuit in Figure 7 is very dependent on the actual data rate and input pattern itself. For example, a "HIGH" signal at the data input (pin 2) will results in a "HIGH" potential at the gate output pins 8, 11 and 6. The current through the LED is limited by the voltage divider given by the resistor R8, R9 (both parallel to the SFH757) and resistor R10. In this case the adjusted forward voltage value is very low and the LED is only slightly illuminated. If a "LOW" signal is present at pin 2, the R8 and R9 resistors are connected to GND via the gates. Therefore the current through the LED is now limited by the effective resistance of R8 and R9 parallel to R10.



$$R10 = \frac{(V_{cc} - V_f) \times 1.9^*}{I_f}$$

$$R9 = \frac{R10}{6.46^*} - 1 \Omega$$

$$R8 = \frac{R10}{3.22^*}$$

$$C4 = \frac{15 \times 10^{-9}^*}{R8}$$

* Empirically determined values
(only for SFH757/74ACTQ00)

Note: The "If" value stands for the
average LED current (data pattern:
PRBS $2^{14}-1$)

Figure 7. Driver circuit for high data rates with the Avago 100 MBd SFH757 transmitter

With installed components for $I_f = 25$ mA, following driver circuit (Figure 7) characteristics are typically for a 10 MBd data rate:

Input Pattern	Typ. Total Current Consumption (mA)	Typ. Optical Output Power (dBm)	Typ. I_f (mA)
"1111"	17	-31	0.2
"0000"	45	1	45
"1010"	35	-2	25

LED driver circuit conditions: $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$ and Data rate = 10 MBd. Installed components for $I_f = 25$ mA.

The circuit stabilizes the switching times and the optical output power level. The used data rate has almost no influence on these values.

If the RC-components are calculated as shown in Figure 7, the following switching times are typical:

Installed Components for Calculated "If" of...	Rise Time (average) $t_{\text{rise}}(10\%\dots90\%)$ [ns], 25°C, Figure 7	Fall Time (average) $t_{\text{fall}}(90\%\dots10\%)$ [ns], 25°C, Figure 7
10 mA	8	11.5
25 mA	7	9.5

Figure 8 shows the eye diagram of the opto/electrical converted output of the SFH757V at the end of a 1 m fiber. The driver circuit is shown in Figure 7 (calculated for " I_f " = 25 mA and $V_{CC} = 5.0\text{ V}$). Total current consumption of the driver circuit with PRBS $2^{14}-1$ is approximately 35 mA with the described conditions. The overshoot on the "High" level of the eye diagram is from the "peaking effect".

The SFH757 transmitter is designed for applications with standard 980/1000/2200 μm plastic fiber. The 2.2 mm aperture holds the fiber's core centered. If fibers with a smaller core diameter than 980/1000 μm are used, the intensity of light at the end of the used fiber is different. Therefore the LED would not conform with the datasheet, especially with respect to the the actual optical output power.

Receiver Circuits

The detector is placed at the other end of the link and converts the optical signal back to an electrical signal. This receiver must be able to accept highly attenuated power down to the nanowatt levels. Subsequent stages of the receiver amplify and reshape the electrical signal back into its original shape.

Some receiver packages have a built-in preamplifier to boost the signal immediately. Detectors operate over a wide range of wavelengths and at speeds that are usually faster than the LEDs. The most important figure of merit for a detector is its sensitivity: what is the weakest optical power it can convert without error? The signal received must be greater than the noise level of the detector. Any detector has a small bit of fluctuating current running through it. This minuscule current is spurious noise and unwanted. The minimum power received by the detector must still be enough to ensure that the detector can clearly distinguish between the signal and the underlying noise. This is expressed as a signal-to-noise ratio (SNR) or a bit error rate. SNR is a straightforward comparison of the signal level and the noise level, while the bit error rate is a more statistical approach to determining the probability of noise causing a bit to be lost or misinterpreted.

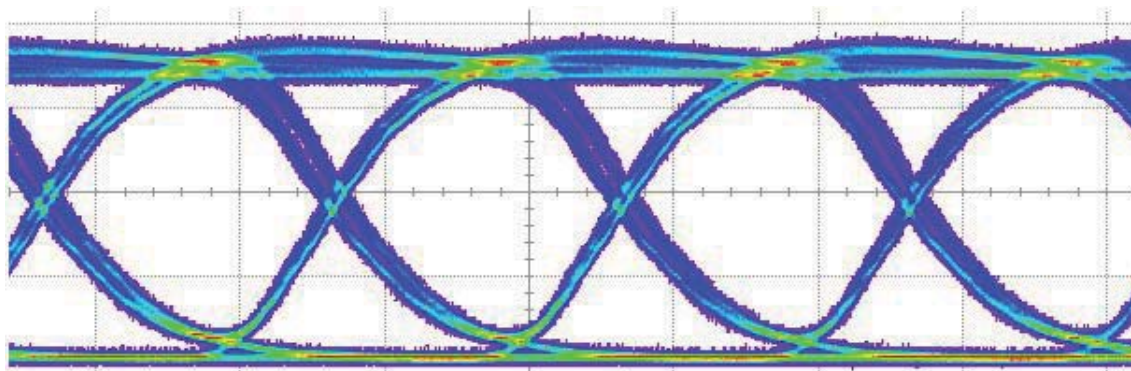


Figure 8. Typical eye diagram of a SFH757 transmitter at a 50 MBd data rate

Avago SFH551/1-1 Receiver

The SFH551/1-1 is a receiver with full a TTL compatible output stage for polymer optical fiber applications for data rates up to 5 MBd. This receiver is fully DC coupled, therefore no line code is needed. The SFH551/1-1 has an inverted input-to-output logic. If light with intensity above the threshold level is coupled into the SFH551/1-1, the electrical output will be logical "LOW" and vice versa.

The SFH551/1-1 receiver is a transimpedance amplifier with a TTL open-collector output stage, therefore a pull-up resistor of at least 330 Ω is necessary. To minimize interference a bypass capacitor (100 nF) must be placed (distance under 3 cm) between Vcc and GND. In critical applications a shorter distance is better.

The photodiode installed in the SFH551/1-1 is silicon based and directly connected to a transimpedance amplifier that works as a preamplifier. A differential amplifier is connected in series and works as a post amplifier. Its output is passed to the internal Schmitt trigger that drives a bipolar NPN transistor. The data-out signal is from the collector of this bipolar transistor.

In this example calculation an optical output power at the end of a 1 m POF of -12 dBm (mean) was chosen. This value refers to the mean value of the optical output power during an input pattern "1010".

$$P_{\text{opt}}(\text{peak}) = P_{\text{opt}}(\text{mean}) + 3 \text{ dB}$$

The optical peak power level in this example calculation would be: -12 dBm + 3 dB = -9 dBm. As in the SFH757 datasheet, an LED current of approximately 3 mA (mean) is needed to realize an optical output power of -12 dBm (mean).

In combination with the LED driver circuit shown in Figure 7 and with installed components for $I_f = 3 \text{ mA}$ [$R_{10} = 2026 \Omega$ (installed 2 k Ω), $R_9 = 312 \Omega$ (installed 300 Ω), $R_8 = 629 \Omega$ (installed 620 Ω) and $C_4 = 24 \text{ pF}$ (installed 22 pF)], the following circuit behavior is typical:

Input Pattern	Typ. Total Current Consumption (mA)	Typ. Optical Output Power (dBm)	Typ. I_f (mA)
"1111"	2	-43	0.1
"0000"	5	-9	5
"1010"	8	-12	3

LED driver circuit conditions: $T_A = 25^\circ \text{C}$, $V_{cc} = 5.0 \text{ V}$ and Data rate = 5 MBd. Installed components for $I_f = 3 \text{ mA}$.

The total current consumption of the receiver circuit (Figure 9) is more dependent on the load resistor than on the used data rate, only a slight rise in I_{cc} value can be detected at different data rates. The current consumption of the SFH551/1-1 with a pull-up resistor of 330 Ω , but without load is typically approximately 14 mA at 5 MBd. With the same conditions and a data rate of 1 MBd, current consumption is typically 12 mA.

As shown in the SFH551/1-1 datasheet, the threshold level is -40 dBm for a stable output logic "1" and an absolute maximum optical input power before overdrive of 0 dBm is fulfilled. If the temperature range from -40°C to $+85^\circ \text{C}$ is taken into account, the maximum optical input power before overdrive is -6 dBm.

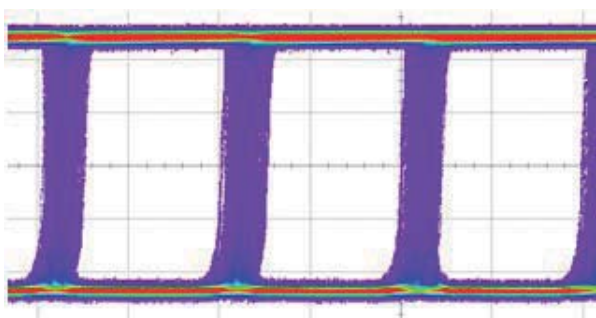
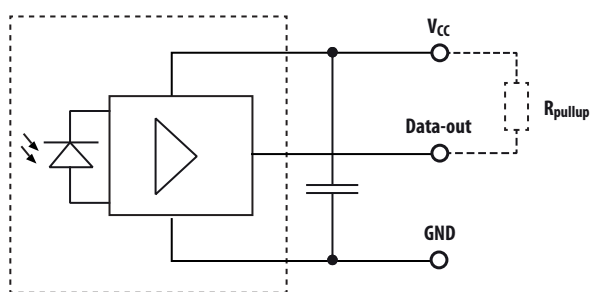


Figure 9. Test circuit and a typical eye diagram of a SFH551/1-1 at 5 MBd (25°C , 100 ns/DIV, $V_{cc} = 5.0 \text{ V}$, $R_{\text{pullup}} = 330 \Omega$)

The pulse width distortion (PWD) of the SFH551/1-1 isn't dependent on the actual data rate, but temperature and the optical input level greatly influence PWD. In this example with an optical input power of -12 dBm (mean), the typical PWD is approximately 90 ns at $T_A = 25^\circ\text{C}$, but over the temperature range the calculated PWD value can be between 55 ns and 120 ns. At a data rate of 5 MBd (input signal width = 200 ns), the typical electrical pulse width at the SFH551/1-1's output is approximately 290 ns (input signal width + PWD). With aging effects and other environmental influences this calculation is on the limits, because a distance of about 3 dB to the datasheet limits is recommended. If the transmission length is greater than 1m the fiber attenuation must be taken into account, because datasheet values of the SFH series (SFH250, SFH551/1-1, SFH757) correspond to a standard POF with a 1m fiber length. The delay times should also be examined. Generally a delay only due to the actual fiber length of about 5 ns/m can be assumed.

The SFH 551/1-1 is designed for applications with standard 980/1000/2200 μm plastic fiber. The 2.2 mm aperture holds the fiber's core centered. If fibers with a smaller core diameter than 980/1000 μm are used, the photodiode will not conform with the datasheet, the actual sensitivity especially deviates from the datasheet values.

Avago SFH250 Receiver

The SFH250 is a low cost receiver for optical data transmission with POF cable. According to the intensity of the incident light, the SFH250 generates an analog photocurrent. In typical applications the photodiode operates with reverse bias and is installed in series with a resistor. By increasing the reverse voltage, the switching times decrease and the SFH250 can be used for transmissions up to 100 MBd.

To reduce the delay time to a minimum, the SFH250 consists of a photodiode with a 2.2 mm aperture, no secondary logic is installed. The reverse current is linearly proportional to the intensity of light that is coupled into the SFH250 by standard POF cable. Since the photodiode is a current source, resistor "RL" is needed (Figure 10) to get a voltage, which can be amplified by preamplifiers.

If the SFH250 has to drive a load of greater than 200 Ω , the capacitance of the photodiode also determines the switching times. Higher load resistance slows switching times. In certain cases this can be compensated for by increasing the reverse voltage level.

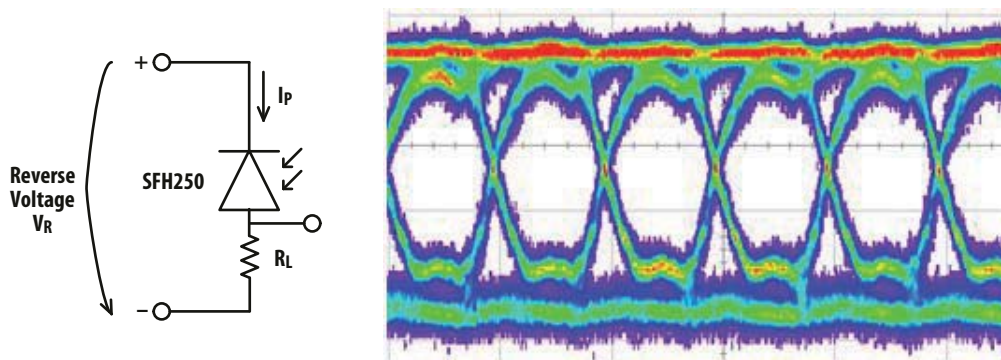


Figure 10. Test circuit and its eye diagram of a SFH250 at 100 MBd (25°C , 10 ns/DIV, $V_R = 30\text{ V}$, $R_L = 50\ \Omega$)

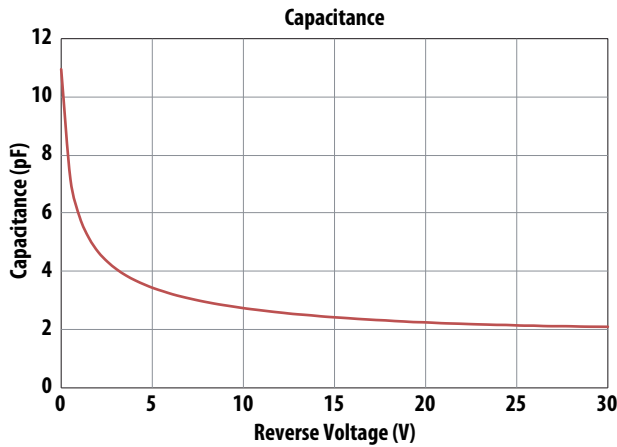


Figure 11. Typical Capacitance of an SFH250; measured at $T_A = 25^\circ\text{C}$ and 1 MHz

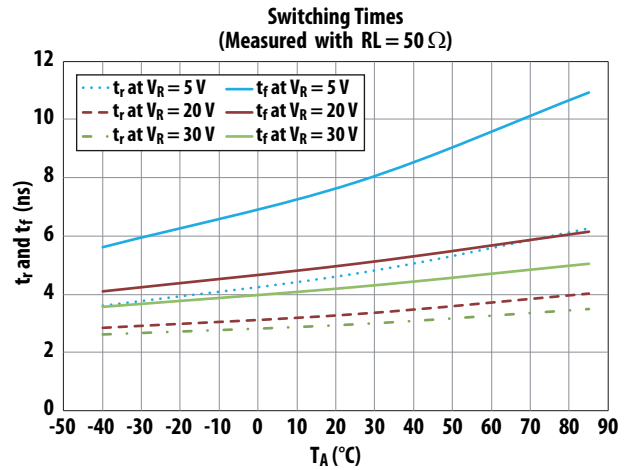


Figure 12. Typical switching times of an SFH250; measured with a "1010" pattern (5 MBd) at -4 dBm (mean) optical input power

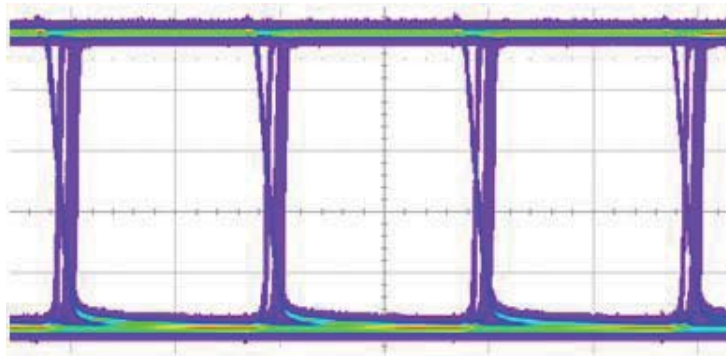
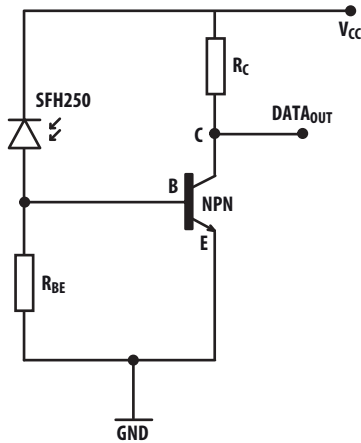


Figure 13. Basic NPN-Circuit for a SFH250 and its typical eye diagram at 500 k Bd (25°C , $100\ \mu\text{s}/\text{DIV}$, $V_{CC} = 5.0\text{ V}$)

Increasing the reverse voltage cause in a decreases of the effective diode capacitance (Figure 11), and that in turn will result in faster switching times (Figure 12). Because of the lower diode capacitance and other internal effects, the switching times will be greatly reduced. If the application supports a reverse voltage of 30 V, the switching times can be reduced to approximately 4 ns.

A very simple and inexpensive receiver circuit for photodiodes is shown in Figure 13. If the voltage drop produced by the photocurrent of the SFH250 across the resistor RBE, exceeds the typical forward breakdown voltage of the

NPN transistor of approximately 0.7 V, the output port becomes a short circuit. The used transistor here is "BF199" by Fairchild Semiconductor. Because of the relative high RBE value (high switching times) and operating conditions that are not optimized conditions (nonlinearity and PWD) transmission rates up to only 1MBd can be realized.

In Figure 14 an optimized NPN circuit is shown, which allows adjustment for better linearity and lower PWD. Typical switching times of 27 ns can be realized with this circuit.

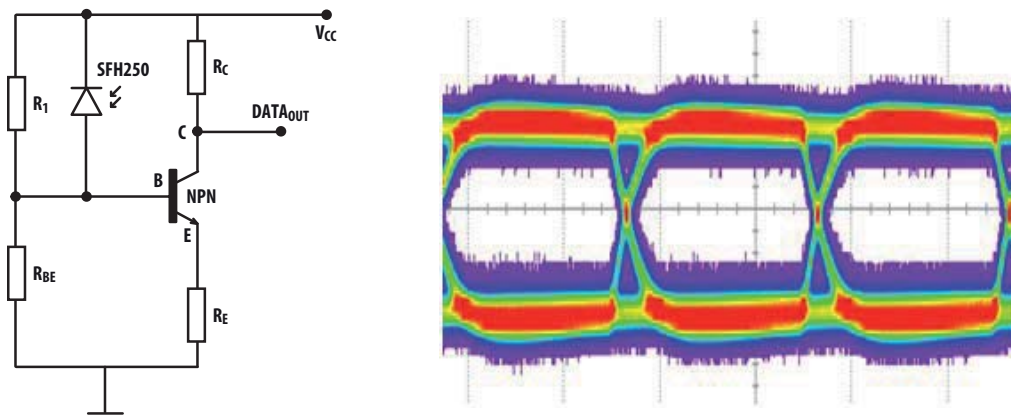


Figure 14. Advanced NPN-circuit for the SFH250 and its typical eye diagram at 5 Mb/s (25° C, 100 ns/DIV, Vcc = 5.0 V)

With the additional resistance R1 in combination with RBE, the circuit can be optimized to the operating point of the NPN transistor. Therefore the small signal behavior of the NPN can be regulated to avoid non-linear behavior. The optical data signal is modulated by the SFH250 on RBE. The "RE" and "RC" resistors must be calculated for the linear working area of the NPN. In addition RE, also provides the function of a temperature compensation. Because of the constant offset voltage at the transistors, base caused by the voltage divider R1/RBE the output port has a DC offset. This circuit allows high current loads at data-out. The limiting element is the discrete transistor, therefore transmission rates up to 5 Mb/s can be realized.

The voltage swing (dynamic part of the DATAout signal) is relatively low for application with high current load. Passing the DATAout signal to an additional amplifier unit is normal practice.

There are also full custom CMOS ICs for high-speed transmissions up to 100 Mb/s on the market that operate with the following basic principle. A resistor in the amplifier's feedback loop determines the current-to-voltage conversion. To avoid pulse disturbance, the amplifier must offer a linear performance over the entire power range of the received light. The preamplifier is followed by a postamplifier in order to achieve a logic level. There is an important difference in coupling between the preamplifier and post

amplifier. If there is DC coupling, data without restriction can be received.

The SFH250 works very well with suitable transimpedance amplifier ICs (e.g. Analog Devices Wideband Transimpedance Amplifier "AD8015") and other rail-to-rail input and output operational amplifiers that are optimized for high speed photodiodes.

SFH250 responsivity is only slightly influenced by temperature change and different reverse voltage levels. An increase in reverse voltage reduces switching times but has almost no influence on the converted photocurrent. This is valid for temperatures between -40° C to 85° C.

SFH250 photodiode current is linearly proportional to the incident light as long as the load resistor value is not too great.

Photocurrent can be easily calculated:

$$\text{Photocurrent } [\mu\text{A}] = \text{Responsivity } (\mu\text{A/mW}) \times \text{Optical Input Power (mW)}$$

As shown in Figure 15, the responsivity value and thus also the photocurrent value (Figure 16) is relatively constant up to certain RL values. But above this certain RL the voltage drop on the RL is in the near of Reverse Voltage level, thereby lower potential difference cause in lower reverse current. A non linear behavior regarding the optical input power is the result, if a too high RL value is set.

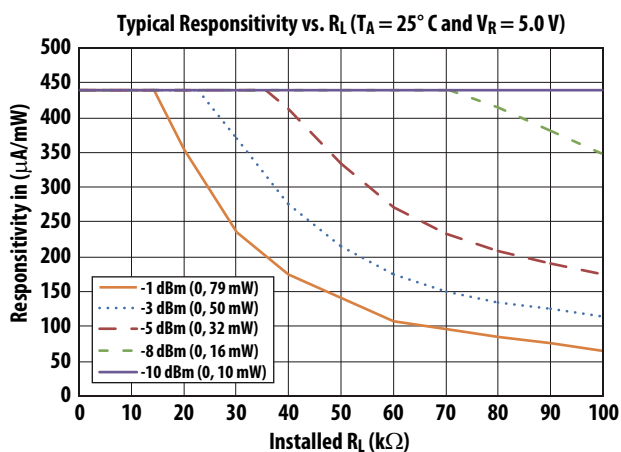


Figure 15. Typical responsivity of a SFH250

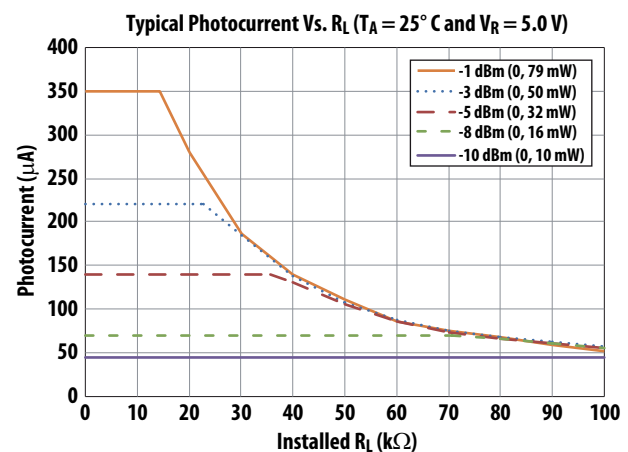


Figure 16. Typical photocurrent of a SFH250

Figure 16 shows, for example, that with an optical input power of -3 dBm (0.50 mW), a typical photocurrent of 220 μ A (440 μ A/mW \times 0.50 mW) can be generated if the load resistor is not greater than about 22.7 k Ω . For higher load resistor values, the generated photocurrent is reduced because of the higher voltage drop and the limited reverse voltage value.

That also means that a linear voltage swing at the load resistor, up to the reverse voltage value, can be realized, if the circuit shown in Figure 10 is used.

Optical Input Power (dBm(peak) at 650 nm)	Typical Photocurrent (μA)	Max. RL (kΩ) at VR = 5.0 V
-1	350	14.3
-3	220	22.7
-5	139	36
-8	70	71.4
-10	44	113.6

It should be pointed out again that a higher load resistor value will increase the switching times of the SFH250.

The SFH250 is designed for applications that use standard 980/1000/2200 μ m POF cable. The 2.2 mm aperture holds the fiber's core centered. If fiber cable with a core diameter less than 980/1000 μ m is used, the photodiode will not conform to the datasheet. Specifically, the responsivity, or in other words the reachable photocurrent value, will be different than datasheet values.

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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