Introduction

High common-mode noise is a significant problem that automotive system designers must overcome when designing a practical and reliable powertrain drive system. Common-mode noise (also known as dV/dt noise) is generated naturally within a system when there is high-frequency switching in the high-voltage power inverters and other power supplies. This article will discuss the various sources of dV/dt noise in a hybrid powertrain drive and suggest several approaches to minimize the effects of the noise on the drive electronics.

Sources and Effects of Powertrain Drive Common-Mode Noise

In a typical hybrid powertrain drive subsystem, there are High-side and Low-side portions of the motor drive subsystem, with each side providing three phases of high current to power the motor (Figure 1). When the gate drivers switch the High-side and Low-side IGBTs in sequence, high dV/dt noise is generated. For example, a typical powertrain that is connected to a high-voltage (400V DC) supply with the switching rise and fall time of 50ns, will generate a dV/dt noise of 400V/50ns, or ~ 8kV/μs whenever the gate-driver switches.

If a short-circuit condition should occur due to some faults, additional overshoot voltage ($V=L\cdot di/dt$) will add on to the DC rail voltage due to a large short-circuit current transient, $di/dt$, that flows through the circuit stray inductance, $L$. The gate-driver circuits must be capable of handling this additional dV/dt noise so they can maintain control and execute the correct protection protocol. Additionally, the requirements for higher DC-rail supply voltages to power larger hybrid vehicles, such as trucks and buses, and faster switching frequencies to reduce conduction loss are all leading to increasing the system requirement to incorporate higher dV/dt noise rejection. Today, hybrid powertrain drive circuits with a dV/dt noise rejection of 15kV/μs are employed to maintain overall system performance, reliability and robustness.
The \( \frac{dV}{dt} \) noise becomes a threat when it couples through parasitic capacitances within the system and causes undesired voltage transitions (Figure 2). Transitions coupled through the parasitic paths could cause the system to lose control by inadvertently triggering a function or causing false feedback, etc. Although \( \frac{dV}{dt} \) noise is very much unwelcome, it exists naturally within the powertrain drive as explained earlier. To minimize its impact designers must identify and tackle all possible coupling paths of \( \frac{dV}{dt} \) noise.

**Solutions**

So, if parasitic capacitances are a significant source of noise feed through, the obvious option is to try to eliminate as much of the parasitic capacitance as possible. That can drastically reduce the \( \frac{dV}{dt} \) noise.

A good starting point is, of course, good circuit design and board layout. A designer should first aim to minimize the gate driver external/layout parasitic capacitance through good layout design. It is essential to maintain the minimum isolation spacing between two adjacent low-voltage and high-voltage regions of the circuit board. Insufficient spacing will reduce the effective isolation and increase parasitic coupling that will degrade common mode rejection performance.

Additionally, high-impedance signal lines which are more sensitive to \( \frac{dV}{dt} \) noise (i.e. \( V_{IN+} \), \( V_{IN} \), and DESAT pins of an optoisolator such as the ACPL-38JT from Avago), should be kept as far away as possible from adjacent isolated region to avoid parasitic coupling. It is always recommended to place bypass capacitors close to the driver supply pins to keep the supply current loop as small as possible and minimize the stray inductance coupling by common mode transient current. Figure 3 compares two board layouts -- a \( \frac{dV}{dt} \) sensitive layout in Figure 3a and a recommended layout in Figure 3b.
After layout issues are dealt with, designers should deal with the Miller-capacitance coupling. The dV/dt noise that couples through the Miller capacitance during switching will induce transient noise current. This transient noise current will flow through the stray inductance that exists along the layout paths from IGBT gate to the gate driver. This inductance affects the gate control voltage. To minimize the effect of dV/dt noise through Miller coupling and to provide cleaner switching waveforms, designer should keep the IGBT gate charging and discharging loop as small as possible. An example of gate driver current buffer circuit to the IGBT is shown in Figure 4a; a recommended printed-circuit board layout is shown in Figure 4b.

After dealing with the Miller effect parasitic capacitance, attention should focus on the selection of the best isolator for the application. The isolator should limit or reject the common-mode noise coupled through the internal parasitic capacitances. There are various isolation techniques available in the market, such as optical isolation (also known as optocouplers), magnetic (transformer) isolation, capacitive isolation, etc. See Figure 5 for basic internal block diagrams of optocoupler, transformer isolator and capacitive isolator.

Among the options, the optocoupler is one of the most popular and effective isolation techniques that provides high common-mode rejection. Enhancements to the basic optocoupler offered by Avago Technologies improve the coupler’s common-mode rejection capability. Some of the enhancements include:

- Low impedance LED drive. LED shows low impedance when it turns on, therefore it is less susceptible to common-mode transient current induced by dV/dt noise. Besides that, the LED junction capacitance of ~80pF helps to reject the high-frequency common-mode noise.
- Internal shield at the photodiode and IC side of the optocoupler. A transparent shield allows optical signal to transmit and at the same time, helps to redirect the common-mode transient current to the ground from affecting the detector and IC circuit.

An internal shield is usually not implemented in transformer and capacitive isolators. This is mainly because an internal shield will block the intended magnetic signal coupling and capacitive signal coupling in both transformer- and capacitive-isolators respectively. Without the shield, unintended dV/dt noise could couple through the same channel as the signals and affect the control signal.
Benchmark CMR Tests of Different Isolators

In order to benchmark the common-mode rejection (CMR) capability of the various isolators, some isolated gate drivers have been chosen by Avago to undergo in-house benchmark common-mode rejection (CMR) testing. A typical benchmark CMR test setup for the isolated gate driver is shown in Figure 6.

The benchmark CMR test result showed that optocoupler has better CMR than transformer and capacitive isolators. Avago Technologies gate drive optocoupler (ACPL-38JT) is capable to withstand high common mode transient without failure and achieves minimum 30kV/μs CMR for both output high (CMH) and output low level (CML), when compared to supplier A (transformer isolator) and supplier B (capacitive isolator). A summary of the test results is shown in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Avago Gate drive optocoupler (ACPL-38JT)</th>
<th>Supplier A Transformer gate driver</th>
<th>Supplier B Capacitive gate driver</th>
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<tbody>
<tr>
<td>Common Mode Rejection at Output Low (CML)</td>
<td>67kV/μs @ VCM=1.5kV</td>
<td>30kV/μs @ VCM=500V</td>
<td>21kV/μs @ VCM=1kV</td>
</tr>
<tr>
<td>Common Mode Rejection at Output High (CMH)</td>
<td>67kV/μs @ VCM=1.5kV</td>
<td>2.5kV/μs @ VCM=500V</td>
<td>4.5kV/μs @ VCM=1kV</td>
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Let’s take a closer look and compare the CMH waveforms of the three different isolators. No failure is seen from the CMH waveform of Avago’s gate drive optocoupler. Avago’s gate driver optocoupler maintains the high output state at a dV/dt of 67kV/μs and VCM=1.5kV, thanks to the low-impedance LED drive and internal shielding, which effectively enhance the gate driver CMR, see Figure 7a. Supplier A, the transformer isolator, failed the benchmark CMH test, where the gate driver is not able to maintain its output at high even if VCM is set to 500V with slow rise time of 160ns (dV/dt~2.5kV/μs), see Figure 7b. Supplier B, the capacitive isolator, the CMH level drops to less than 15kV/μs when the VCM rises to 900V and failure is observed when VCM rises to 1kV and above for output high test (dV/dt~4.5kV/μs), see Figure 7c.

Figure 6. Typical Benchmark CMR Test Setup

Figure 7a. Avago Optocoupler CMH pass at VCM=1.5kV, dV/dt ~67kV/μs

Figure 7b. Supplier A transformer isolator CMH failure at VCM=500V, dV/dt ~2.5kV/μs

Figure 7c. Supplier B capacitive isolator CMH failure at VCM=1kV, dV/dt ~4.5kV/μs
The ACPL-38JT optocoupler is more than just a basic coupler – it is specifically designed for gate driving and incorporates integrated Desaturation (V_{CE}) detection and Fault-Status Feedback (Figure 8). The integrated detection and feedback helps simplify system design and makes IGBT V_{CE} fault protection easy to implement while satisfying the automotive AEC-Q100 Grade 1 semiconductor requirement. The optocouplers also include reinforced insulation and enhanced reliability to handle the performance requirements in automotive and high-temperature industrial applications.

**Figure 8. Avago Automotive Gate Drive Optocoupler, ACPL-38JT Functional Diagram**

**Conclusion**

Hybrid powertrain drives deal with substantial dV/dt noise while working in harsh automotive environment. To maintain system reliability and ensure passengers safety, designers should minimize the threat from unpredicted common-mode noise by employing good layout and system design and by choosing the right isolation device. Avago Technologies' gate driver optocouplers that incorporate low-impedance LED drive and internal shielding deliver the performance needed to reject high common-mode transient noise.