ACML-7400/7410/7420

3.3V/5V High Speed CMOS Digital Isolator

AVAGO TECHNOLOGIES

Reliability Data Sheet

Description

The reliability data shown includes Avago Technologies reliability test data from the reliability qualification done on this product family. All of these products use the similar IC, and the same packaging materials, processes, stress conditions and testing. The data in Table 1 and Table 2 reflect actual test data for devices on a per channel basis. Before stress, all devices are preconditioned at MSL 1 using a solder reflow process (260 °C peak temp) and 20 temperature cycles (-55 °C to +125 °C, 15 mins dwell, 1 min transfer). These data are taken from testing on Avago Technologies devices using internal Avago Technologies process, material specifications, design standards, and statistical process controls. **THEY ARE NOT TRANSFERABLE TO OTHER MANUFACTURERS' SIMILAR PART TYPES.**

Operating Life Test

For valid system reliability calculations it is necessary to adjust for the time when the system is not in operation. Note that if you are using MIL-HDBK-217 for predicting component reliability, the results may not be comparable to those given in Table 2 due to different conditions and factors that have been accounted for in MIL-HDBK-217. For example it is unlikely that your application will exercise all available channels at full rated power with the IC always ON as Avago Technologies testing does. Thus, your application total power and duty cycle must be carefully considered when comparing Table 2 to predictions using MIL-HDBK-217.

Definition of Failure

Inability to switch, i.e. "functional failure" is the definition of failure in this data sheet. Specifically, failure occurs when the device fails to switch ON with 2 times the minimum recommended drive current (but not exceeding the max rating) or fails to switch off when there is no input current

Failure Rate Projections

The demonstrated point mean time to failure (MTTF) is measured at the absolute maximum stress condition. The failure rate projections in Table 2 uses the Arrhenius acceleration relationship, where a 0.43 eV activation energy is used as in the hybrid section of MIL-HDBK-217.

Application Information

The data of Table 1 and 2 were obtained on devices with high temperature operating life duration. An exponential (random) failure distribution is assumed, expressed in units of FIT (failures per billion device hours) are only defined in the random failure portion of the reliability curve.

Table 1. Demonstrated Operating Life Test Performance

Stress Test Condition	Total Device Tested	Total Device Hours	Number of Failed Units	Demonstrated MTTF(hr) @ Ta = +125 °C	Demonstrated FITs @ Ta = +125 °C
Ta = 125 °C Vdd1 = 6.2V, Vdd2 = 6.2V	154	154,000	0	> 306,606	<3,262

Table 2. Reliability Projection for Device Listed in Title

Ambient Temperature (°C)	Junction Temperature (°C)	Typical (60% Confidence)		90% Confidence	
		MTTF (Hr/fail)	FITs (Fail/10^9h)	MTTF (Hr/fail)	FITs (Fail/10^9h)
125	140	334,616	2,988	133,157	7,510
120	135	387,933	2,578	154,374	6,478
110	125	527,250	1,897	209,814	4,766
100	115	728,023	1,374	289,710	3,452
90	105	1,022,559	978	406,917	2,458
80	95	1,463,019	684	582,194	1,718
70	85	2,135,512	468	849,806	1,177
60	75	3,185,620	314	1,267,686	789
50	65	4,865,904	206	1,936,338	516
40	55	7,626,948	131	3,035,068	329
30	45	12,297,419	81	4,893,635	204
25	40	15,794,894	63	6,285,421	159

Table 3. Mechanical Tests (Testing done on a constructional basis)

Test Name	Reference Standard	Test Conditions	Units Tested	Units Failed
Temp Cycling	JESD-A104	-55 to 125 °C Transfer = 1 min Dwell = 15 mins 1000 cycles	304 [1]	0
Physical Dimensions	JESD-B100	Conformance to datasheet package drawings	30	0
Solderability (RoHS condition)	JESD-B102	8hrs steam aging (93 °C), followed by solder dip (260 °C,5sec)	10	0
Preconditioning	J-STD-020 JA113	As per reference standard (to conform to MSL 3)	923	0
Preconditioning	J-STD-20 JA113	As per reference standard (to conform to MSL 1)	231	0

Table 4. Environmental Testing

Test Name	Reference Standard	Test Conditions	Units Tested	Units Failed
Temperature Humidity Bias	JESD-A101	Ta = 85 °C, RH=85% Vdd1=5.5V, Vdd2=5.5V Time = 1000 hrs	80 [1]	0
Temperature Humidity (without Bias)	JESD-A101	Ta = 85°C, RH =85% Unbiased Time = 1000 hrs	154 [1]	0
High Temperature Bake	JESD-A103	Ta = 150°C Unbiased Time = 1000hrs	231 [1]	0
High Temperature Bake	JESD-A103	Ta = 175°C Unbiased Time = 500hrs	77	0
Unbiased Autoclave	JESD-A102	Ta = 121°C, RH = 100% 15psig Unbiased Time = 96 hours	77	0

Note 1. Units are preconditioned at MSL3 @260 °C

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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