

## AFBR-5972Z

### Compact 650-nm Transceiver with Compact Versatile-Link Connector for Fast Ethernet over POF

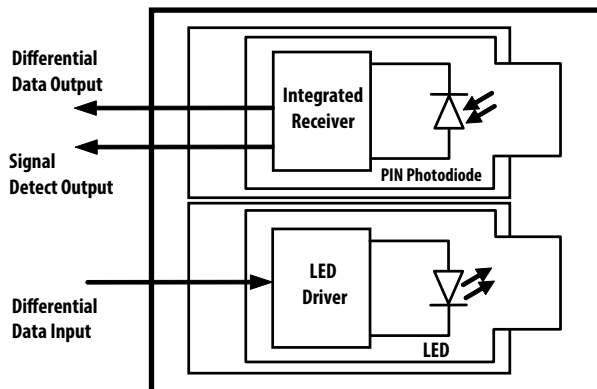


#### Description

The Broadcom® AFBR-5972Z Transceiver provides the system designer with the ability to implement Fast Ethernet (100 Mb/s) over standard bandwidth  $0.5 \pm 0.05$  NA POF. It features a compact design and has a form factor similar to the UTP connector. This transceiver features a new compact Versatile-Link duplex connector AFBR-4526Z and is compatible with existing simplex Versatile-Link connectors.

This product is lead free and compliant with RoHS.

Figure 1: Block Diagram



#### Features

- Compatible to IEEE 802.3 100BASE-FX PMA using POF PMD
- Link lengths up to 50m POF (NA0.5) or 70m POF (NA0.3)
- Compact foot print
- 3.3V operation
- LVPECL input and output data connections
- LVPECL signal detect output
- Temperature range  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

#### Applications

- Industrial Ethernet and Fast Ethernet over polymer optical fiber PMD
- Networking in harsh environments such as factory automation or power generation and distribution
- Supporting various Ethernet Fieldbus protocols

# Transmitter

The transmitter contains a 650-nm LED with an integrated driver. The LED driver operates at 3.3V. It receives an LVPECL/LVDS electrical input, and converts it into a modulated current driving the LED. The LED is packaged in an optical subassembly, part of the transmitter section. The optical subassembly couples the output optical power efficiently into POF fiber.

# Receiver

The receiver uses an Si PIN photodiode. The PIN photodiode is packaged in an optical subassembly, part of the receiver section. This optical subassembly couples the optical power efficiently from POF fiber to the receiving PIN. The integrated IC operates at 3.3V and converts the photocurrent into LVPECL electrical output.

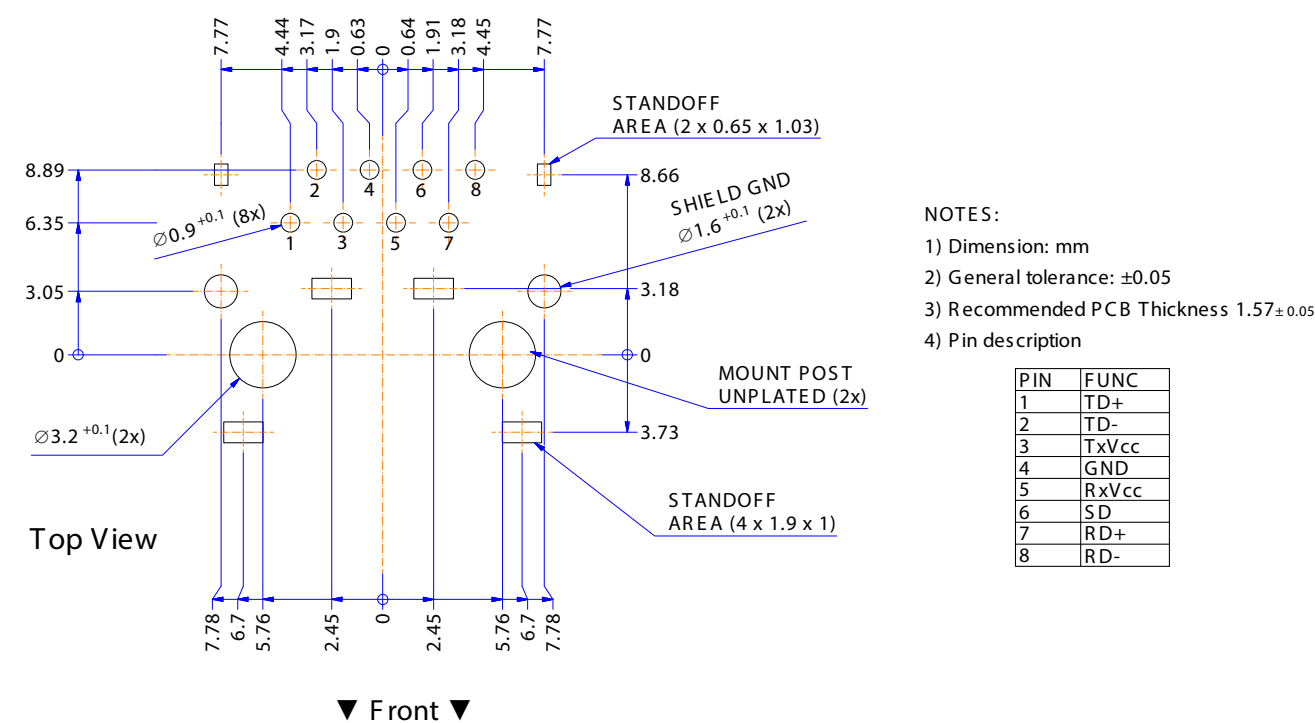
# Package

The transceiver package consists of three basic elements; two opto-electical subassemblies and the housing as shown in the block diagram in [Figure 1](#). The package outline drawing and pin-outs are shown in [Figure 2](#) and [Figure 5](#).

The opto-electrical subassemblies use a high-volume assembly process together with low-cost lens elements that result in a cost-effective building block. They consist of the active III-V devices, IC chips, and various surface-mounted passive components.

There are eight signal pins, four EMI shield solder posts and two mounting posts, which exit the bottom of the housing. The solder posts are isolated from the internal circuit of the transceiver and are to be connected to chassis ground. The mounting posts are to provide mechanical strength to hold the transceiver to the application board.

Figure 2: PCB Footprint and Pin-out Diagram



## Pin Descriptions

**Pin 1 TData+:** Transmitter data in. This input is a 3.3V LVPECL/LVDS compatible differential line.

**Pin 2 TData-:** Transmitter data in negative. This input is a 3.3V LVPECL/LVDS compatible differential line.

**Pin 3 TX Vcc:** Transmitter power supply pin. Provide +3.3V DC using a transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the Tx Vcc pin.

**Pin 4 GND:** Common ground pin. Directly connect this pin to the signal ground plane of the host board.

**Pin 5 RX Vcc:** Receiver power supply pin. Provide +3.3V DC using a receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the Rx Vcc pin.

**Pin 6 SD:** Signal detect pin. If an optical signal is present at the optical input, SD output is a logic "1". Absence of an optical input signal results in a logic "0" output. This pin drives an LVPECL input of an upstream circuit, such as Signal Detect input or Loss of Signal-bar.

**Pin 7 RData+:** Receiver data out. This data line is a 3.3V LVPECL compatible differential line, which should be properly terminated.

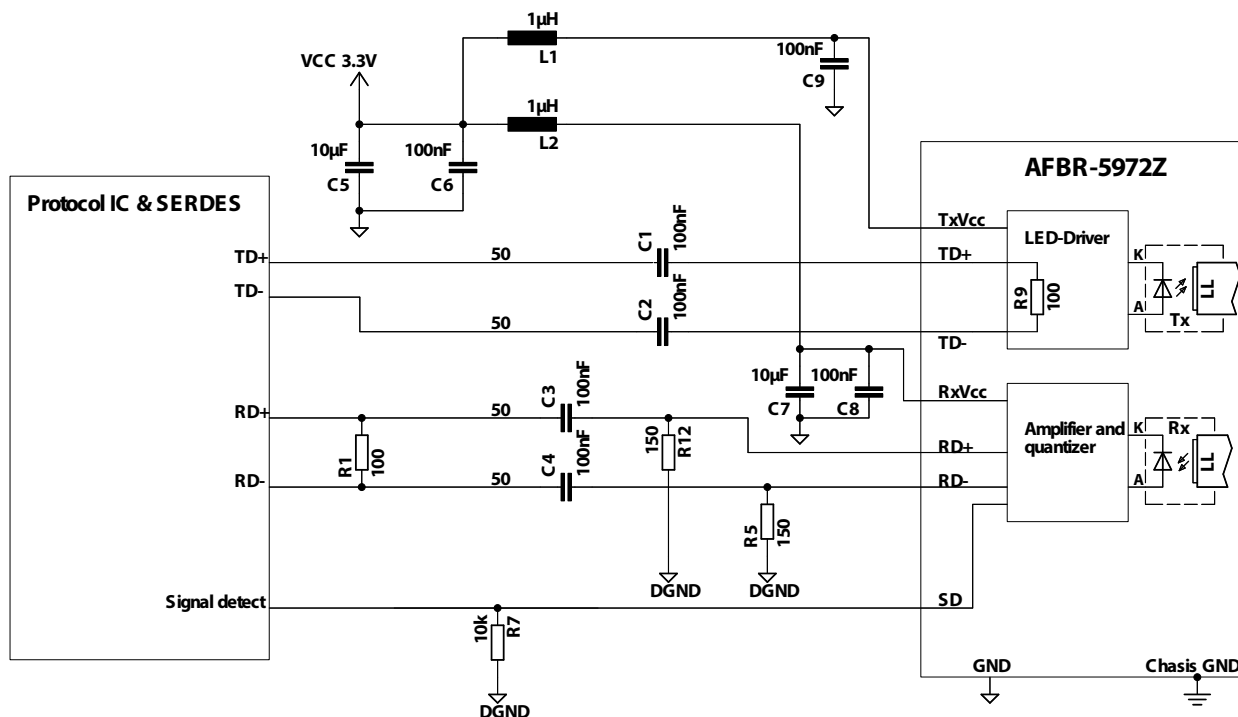
**Pin 8 RData-:** Receiver data out negative. This data line is a 3.3V LVPECL compatible differential line, which should be properly terminated. When SD is deasserted, RData+ is set to logic "0" and RData- is set to logic "1".

**Shield:** This is to be connected to the equipment chassis ground.

## Application Circuit

The recommended application circuit is shown in [Figure 3](#).

Figure 3: Recommended Application Circuit



## Board Layout – Decoupling Circuit and Ground Planes

Take care of the layout of the application circuitry to achieve optimum performance of the transceiver. Use a power supply decoupling circuit to filter out noise to assure optimal product performance. Provide a contiguous signal ground plane in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. Also, connect the shield posts to the chassis ground to provide optimum EMI, ESD, and EMS performance, which is in keeping with good high frequency board layout practices.

## Regulatory Compliance Table

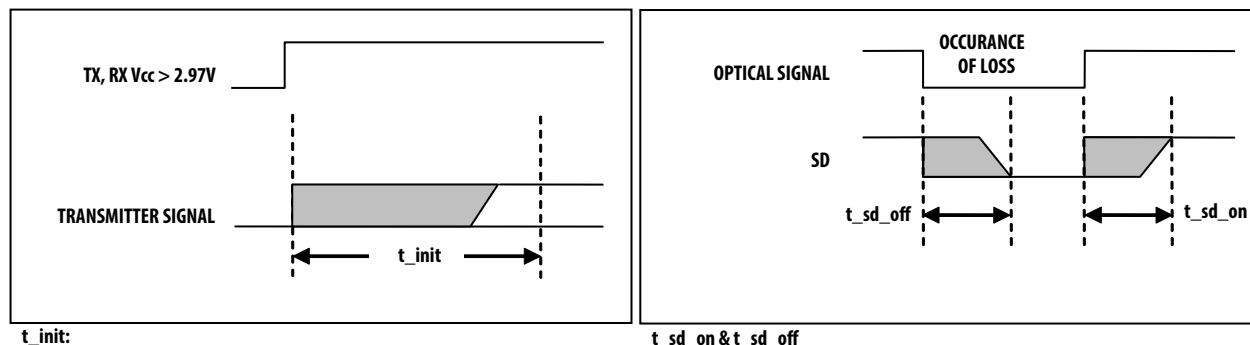
Feature	Test Method	Performance
Electrostatic discharge (ESD) to the electrical pins	JESD22-A114	Withstands up to 2000V HBM applied between the electrical pins.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 15V/m field swept from 80 MHz to 1 GHz applied to the transceiver when mounted on a circuit board without chassis enclosure.
Eye safety	EN 60825-1:52007	Laser class 1 product (LED radiation only). TÜV certificate: R 50483935. <b>CAUTION:</b> Use of controls or adjustments of performance or procedures other than those specified herein may result in hazardous radiation exposure.
Component recognition	Underwriter Laboratories	UL File #: E173874

## Transceiver Diagnostics Timing Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Time to Initialize	$t_{init}$	—	5	ms	Note <sup>a</sup> , Figure 4
Hardware SD Assert Time	$t_{sd\_on}$	—	100	$\mu$ s	Note <sup>b</sup>
Hardware SD Deassert Time	$t_{sd\_off}$	—	100	$\mu$ s	Note <sup>c</sup>

- Time from power-on to when the modulated optical output rises above 90% of nominal.
- Time from valid optical signal to SD assertion.
- Time from loss of optical signal to SD deassertion.

Figure 4: Transceiver Timing Diagrams



## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation. All other parameters having values within the recommended operation conditions. It should not be assumed that limiting values of more than one parameter can be applied to the products at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	$T_S$	−40	+100	°C	
Case Operating Temperature	$T_C$	−40	+85	°C	Notes <sup>a, b</sup>
Lead Soldering Temperature	$T_{\text{sold}}$	—	260	°C	Note <sup>c</sup>
Lead Soldering Time	$t_{\text{sold}}$	—	10	s	Note <sup>c</sup>
Supply Voltage	$V_{CC}$	−0.5	4.0	V	
Data Input Voltage	$V_I$	−0.5	$V_{CC}$	V	
Differential Input Voltage	$V_D$		2.0	V	Peak to peak
Output Current LVPECL	$I_{\text{Dout}}$	−45	45	mA	

- a. Operating the product outside the maximum rated case operating temperature range will compromise its reliability and may damage the product.
- b. The temperature is measured using a thermocouple connected to the hottest position of the housing.
- c. The transceiver is Pb-free wave solderable.

## Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Case Operating Temperature	$T_C$	−40	—	+85	°C	Notes <sup>a, b</sup>
Supply Voltage	$V_{CC}$	3.0	3.3	3.6	V	
Differential Input Voltage	$V_D$	0.22	0.8	1.6	V	Peak to peak
Input Common Mode Voltage	$V_{\text{IN\_CM}}$	GND + 0.8	—	$V_{CC} - 0.8$	V	
Data and Signal Detect Output Load	$R_L$	—	50	—	$\Omega$	
Signaling Rate (Fast Ethernet)	$B_{FE}$	—	125	—	Mbaud	4B/5B; Note <sup>c</sup>
Signaling Rate (General)	$B_G$	10	—	125	Mbaud	Note <sup>d</sup>

- a. The temperature is measured using a thermocouple connected to the housing.
- b. Electrical and optical specifications of the product are guaranteed across recommended case operating temperature range only.
- c. Ethernet autonegotiation pulses are not supported.
- d. Evaluation of 10 Mbaud was performed using a biphasic code.

## Transceiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	$I_{CC}$	—	85	110	mA	Note <sup>a</sup>
Power Dissipation	$P_{DISS}$	170	280	400	mW	Note <sup>a</sup>
Power Supply Noise Reduction	$P_{SNR}$	50	—	—	mV	Peak to peak; Note <sup>b</sup>

a. Characterized with terminations as shown in [Figure 3](#).

b. Frequencies from 0.1MHz to 100MHz.

## Transmitter Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Average Launched Power (1-mm POF; NA = 0.5)	$P_o$	−10	−6.5	−3.0	dBm	Note <sup>a</sup>
Extinction Ratio	EXT	10	—	—	dB	Note <sup>a</sup>
Central Wavelength	$\lambda_C$	635	650	675	nm	Note 7
Spectral Bandwidth RMS	$\lambda_W$	—	—	17	nm	
Optical Rise Time (10% to 90%)	$t_r$	—	1.8	3.5	ns	Notes <sup>a, b</sup>
Optical Fall Time (90% to 10%)	$t_f$	—	1.8	3.5	ns	Notes <sup>a, b</sup>
Duty Cycle Distortion Contributed by the Transmitter	DCD	—	—	1.0	ns	Note <sup>a</sup>
Data-Dependent Jitter	DDJ	—	—	0.6	ns	Note <sup>a</sup>
Random Jitter Contributed by the Transmitter	RJ	—	—	0.76	ns	Peak to peak; Notes <sup>a, c</sup>
Overshoot	Ov	—	7	25	%	Note <sup>a</sup>

a. Measured at the end of 1-meter plastic optical fiber with a PRBS  $2^7-1$  sequence.

b. 10%...90% or 90%...10%, respectively

c. Based on BER =  $2.5 \times 10^{-10}$ .

## Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Data Output Voltage – Low	$V_{OL} - V_{CC}$	—	–1.63	—	V	
Data Output Voltage – High	$V_{OH} - V_{CC}$	—	–0.99	—	V	
Data Output Voltage Swing	$ V_{OH} - V_{OL} $	500	—	900	mV	Single ended
Data Output Rise Time (10% to 90%)	$t_r$	—	0.7	3.0	ns	Note <sup>a</sup>
Data Output Fall Time (90% to 10%)	$t_f$	—	0.7	3.0	ns	Note <sup>a</sup>
Duty Cycle Distortion	DCD	—	—	1.0	ns	
Data Dependent Jitter	DDJ	—	—	1.2	ns	Note <sup>b</sup>
Random Jitter	RJ	—	—	2.14	ns	Peak to peak; Notes <sup>b, c</sup>
Signal Detect Output Voltage – Low	$V_{OL} - V_{CC}$	–1.83	–1.75	–1.50	V	Terminations as shown in Figure 3
Signal Detect Output Voltage – High	$V_{OH} - V_{CC}$	–1.16	–1.10	–0.88	V	Terminations as shown in Figure 3

a. Characterized with terminations as shown in Figure 3.

b. Contributed by Rx only.

c. Based on BER =  $2.5 \times 10^{-10}$ .

## Receiver Optical Characteristics

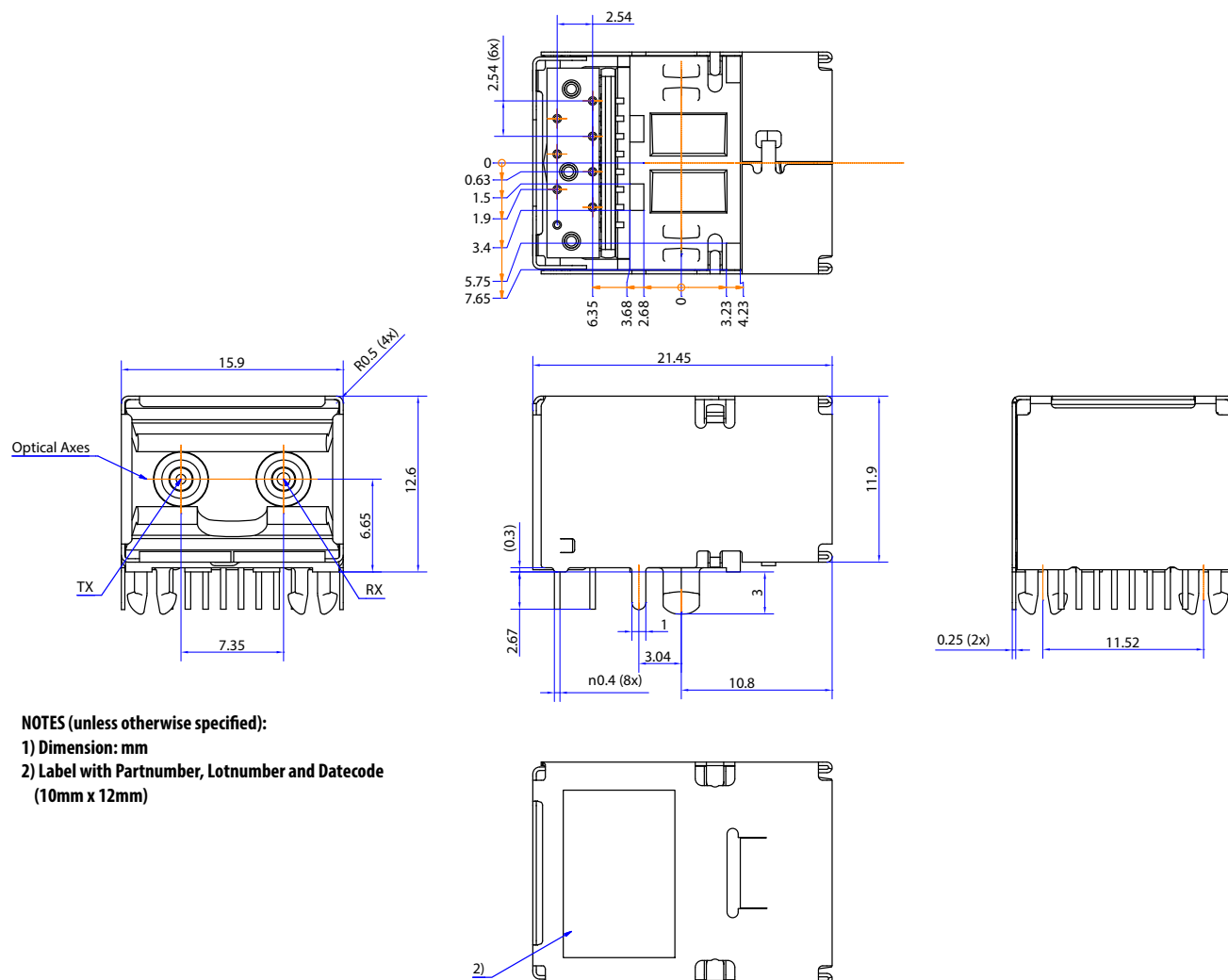
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Unstressed Receiver Sensitivity	CSEN	–26	–27	—	dBm	Note <sup>a</sup>
Input Optical Power Maximum	PIN MAX	—	—	–3.0	dBm	Notes <sup>a, b</sup>
Central Wavelength	$\lambda_C$	635	650	675	nm	Note <sup>c</sup>
Spectral Bandwidth RMS	$\lambda_W$	—	—	17	nm	Note <sup>c</sup>
Signal Detect Asserted	$P_A$	—	–31	—	dBm	
Signal Detect Deasserted	$P_D$	—	–33	—	dBm	
Signal Detect Hysteresis	$P_A - P_D$	—	2	—	dB	

a. Average power. measured with a PRBS  $2^7 - 1$  sequence. BER <  $2.5 \times 10^{-10}$ .

b. Input Optical Power Maximum is defined as the maximum optical average input power where the receiver duty cycle distortion reaches  $\pm 1$  ns.

c. Measured at the end of 1 meter plastic optical fiber with a PRBS  $2^7 - 1$  sequence.

Figure 5: Package Outline Drawing





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