Dual-band LNA Design for Wireless LAN Applications

White Paper

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Introduction

Highly integrated, cost-effective RF circuitry is becoming more and more essential to the proper operation of portable wireless equipment. The receive circuitry sensitivity is critical to the range over which the wireless network can operate. In this regard, the low-noise amplifier (LNA) plays a very important role to ensure stable reception of signals.

This paper describes the design and implementation of the MMIC and module level circuitry of a dual-band LNA that operates in the IEEE 802.11g/a bands. The complete LNA is housed in a 3mm x 3mm molded chip-on-board package and requires only two external bypass capacitors in actual operation.

Dual band LNA

A dual-band LNA that covers both the IEEE 802.11g/a bands must operate with low current, high gain and exhibit low noise figure (NF) over both the 2.4 GHz and 5 GHz band. In addition, the 5 GHz amplifier must cover a 4.9-5.9 GHz bandwidth since different countries operate in the 5 GHz band at slightly different frequencies. This implies the LNA must maintain a constant operating performance across a 20% bandwidth.

This article discusses the design of a dual-band WLAN LNA which operates at 2.4 GHz (802.11b/g standard) and 4.9 – 5.95 GHz (802.11a standard) bands. The LNA is fabricated using Avago's in-house enhancement pHEMT GaAs process and packaged in a 3 mm x 3 mm plastic package. Table 1 summarizes the key specifications for the LNA in both bands.

It is obvious that the specifications are extremely challenging technically. In addition to this, the specifications must be met with high yield in a high volume manufacturing environment.

Figure 1 shows a typical on-wafer plot of an 800 µm FET NFmin in the Avago process across different bias conditions. Measurement uncertainty is about 0.05 dB. The noise performance is outstanding.

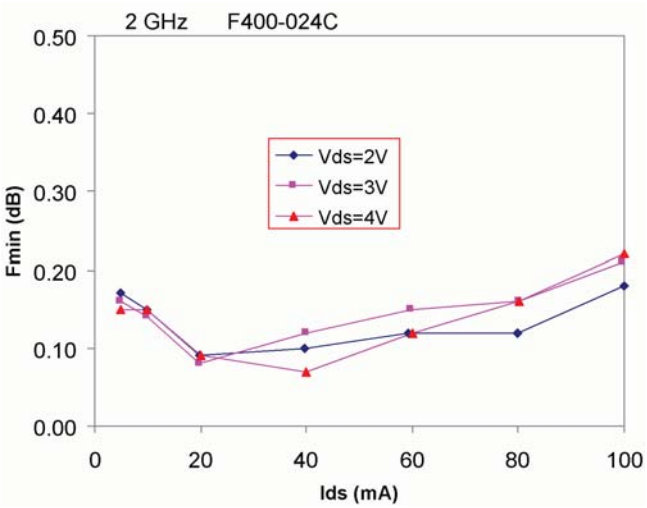


Figure 1. NFmin vs Id and Vd for a 800 µm gate width pHEMT FET

Simulation models were extracted for different device sizes that incorporate noise, small-signal and large-signal characteristics. Accurate results were obtained using the Root model in Avago's Advanced Design System (ADS) design suite. The model is scalable in size and usable over wide bias ranges. This is important as the designer will need to sweep size and bias to find the optimal design solution.

Table 1. Specification of the Dual band LNA

	2.4 GHz LNA			5 GHz LNA		
	Min	Typ	Max	Min	Typ	Max
Frequency range (GHz)	2.4		2.5	4.9		6
Gain (dB)	15			20		
S11 (dB)			-8			-8
S122 (dB)			-8			-8
Noise Figure (dB)			1			1.4
Current (mA)			15			18
Voltage (V)	3			3		

2.4 GHz LNA Design

A cascode topology is used in the 2.4 GHz LNA since it gives higher gain due to the absence of Miller capacitance and permits current reuse in what is effectively a two-stage design. In addition to that, the cascode configuration enables higher linearity to be obtained for the same current draw. Figure 2 shows the schematic.

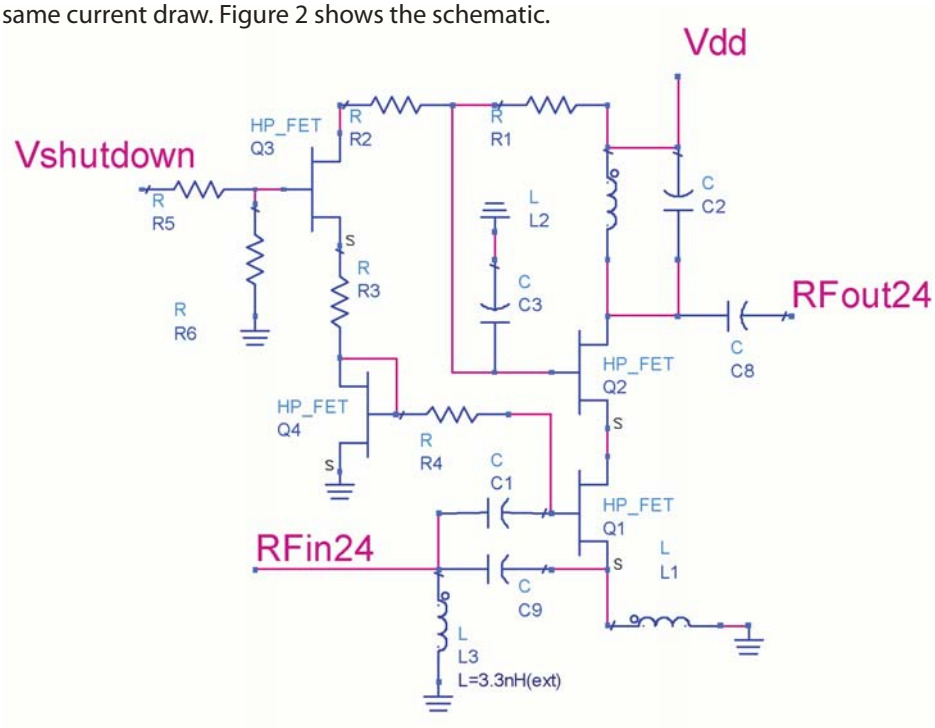


Figure 2.Cascode LNA for the 2.4 GHz band

Q1 and Q2 form the gain and cascode FET pair. Inductor L2 and capacitor C2 form an L-C resonator load used to resonate the cascode transistor output at 2.4 GHz. Source inductance to ground at Q1 acts as series feedback to simultaneously improve input match and NF. The input impedance at the Q1 gate can be approximated by:

Equation 1

$$Z_{in} = L_s \frac{g_m}{C_{gs}} + j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right)$$

where g_m is the transconductance of Q1 and Ls is the total source inductance at the source of Q1. In practice, this is the sum of bond wires connected to the die and via hole inductances in the printed circuit board (PCB). L3 is an additional off-chip SMT component to match the input of the LNA, as close as possible, to the minimum noise figure impedance Γ_{opt} . Capacitor C3 acts as an RF bypass for Q2. Capacitors C1 and C8 are DC block capacitors. FET Q4 is a current mirror for biasing. Resistive voltage divider R1 and R2 sets the gate voltage for Q2, and FET Q3 acts as a shutdown switch. To model the non-idealities of a surface mount component, s-parameter data from the manufacturer was used.

At 2.4 GHz, the effects of parasitics such as spiral inductor losses and mutual coupling of bond wire inductances can affect performance significantly. As an example, the L-C resonant tank at Q2's drain is implemented on-chip and therefore needs to be modeled rigorously. With Momentum, 2.5D E-M simulations were performed with circuit coverage as large as possible. The results of the spiral inductor simulations are shown below.

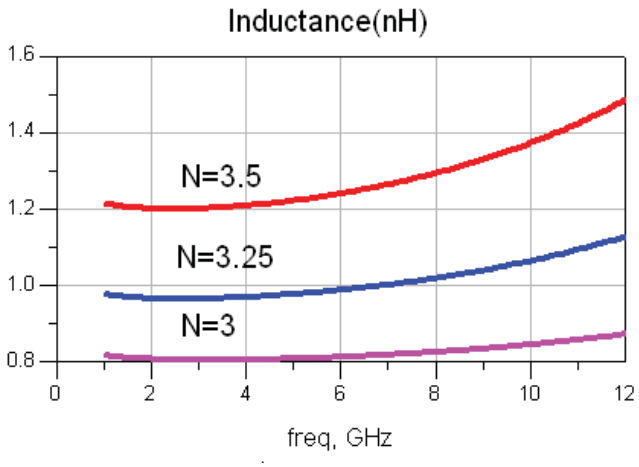
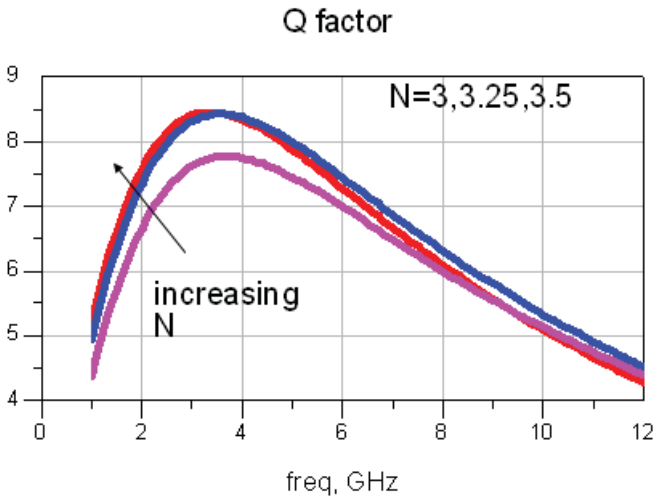


Figure 3. Inductance value vs. frequency and number of turns



Figures 3 and 4 show the plot of inductance and Q factor versus the frequency and number of turns. These simulation results were used with the circuit level components to simulate the complete LNA. Without optimizing the circuit, the result already shows that gain peaks correctly at the centre frequency of 2.4 GHz. Series resistance along the inductor is the manifestation of the skin-effect that occurs on the inductor metallization at high frequency. Gain, noise figure and return loss all still met the specifications. Further optimization on ADS shows performance can still be further improved. The following graph shows the performance of the LNA after the components value has been optimized.

Figure 4. Q factor vs. frequency and number of turns

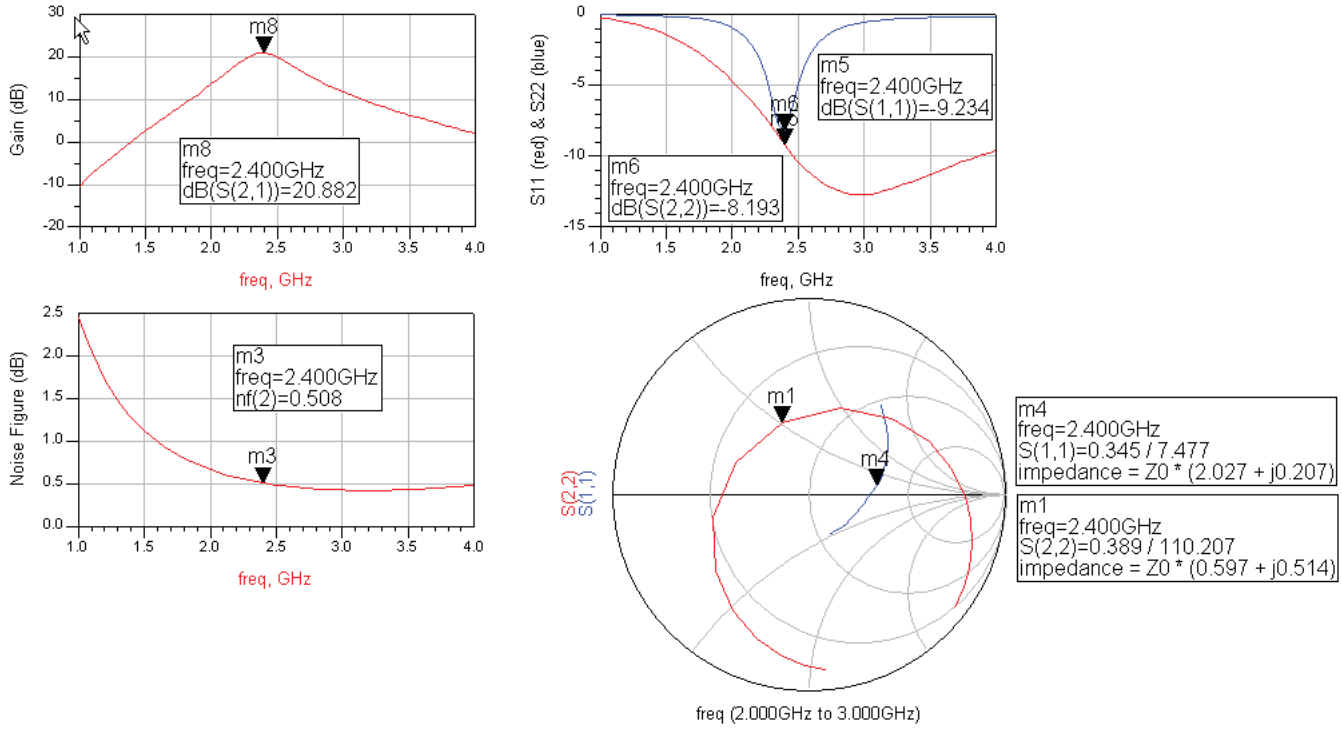


Figure 5. Gain, return loss and Noise Figure of the 2.4 GHz LNA after optimization

5 GHz LNA Design

Unlike the 2.4 GHz LNA, the 5 GHz design requires higher gain that is flat for more than 20% bandwidth at the 5 GHz band and a noise figure that is well-controlled in band. A two-stage amplifier is required to meet these specifications.

This amplifier again employs inductive loading (L2 and L4) at each of the stages, both of which are integrated on-chip. Input impedance and noise matching is again achieved in a similar manner to the 2.4 GHz version with a source inductor and shunt input inductor at the gate. Shunt R-C feedback (R10 and C3) is used in the second stage to improve the output match. Components L3 and C2 form a high pass interstage match. This match compensates the negative gain roll-off from the first stage so that the overall gain forms a band pass response centered at 5.5 GHz. Capacitor C3 acts as an RF ground for the matching network. The R-C network across C3 (R4 and C4) improves the stability of the amplifier. The Q2 source is grounded through a backside via.

ADS enable different models to be used to form non-ideal characteristics of the passive components. Bondwire coupling is significant in the 5 GHz design, and the various models enable coupling to be modeled with sufficient accuracy to mimic actual performance [1]. Figure 7 shows the simulation result of the complete 5 GHz band LNA with (a) ideal components, and (b) optimized non-ideal components value.

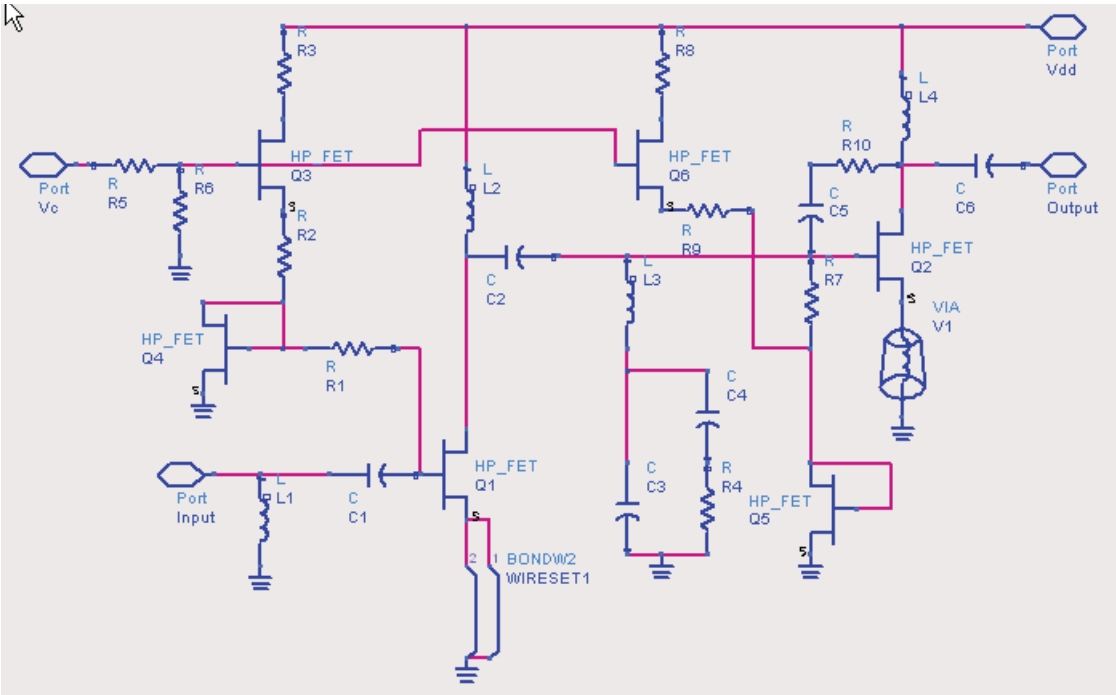


Figure 6.Schematic of a two-stage LNA for 5-6 GHz band

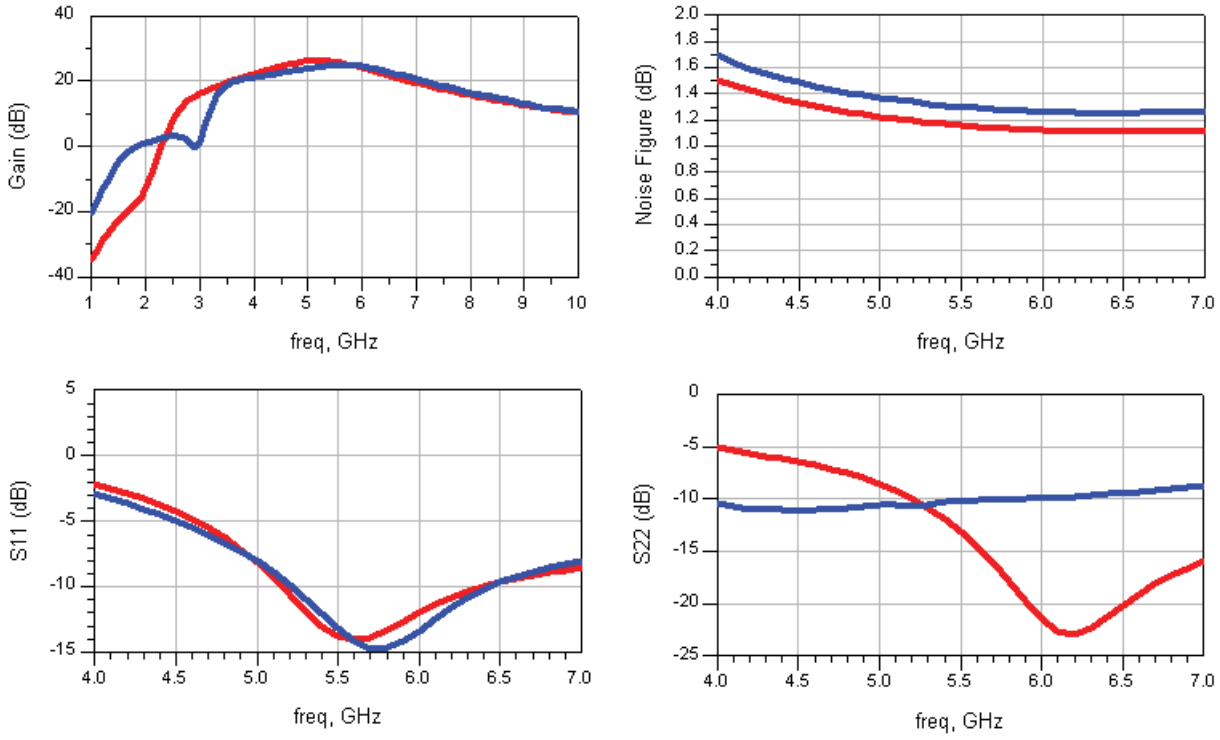


Figure 7. Gain, return loss and Noise Figure for ideal components (red) and non-ideal components (blue)

Note the significant effects on S22 and the shift in gain peaking with non-ideal models simulated in Momentum. A more complete Momentum simulation would be to simulate the complete layout and add active devices later to the multi-port s-parameter file generated by Momentum. This is shown in Figure 8.

Simulation results reveal that inductive coupling significantly affects frequency response. It also highlights regions of high current densities that can affect P1dB performance. The complete simulated results are shown in Figure 9 below.

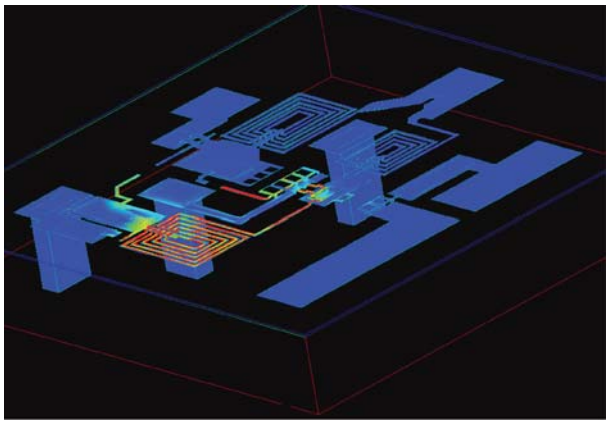


Figure 8. Momentum simulation of the complete layout

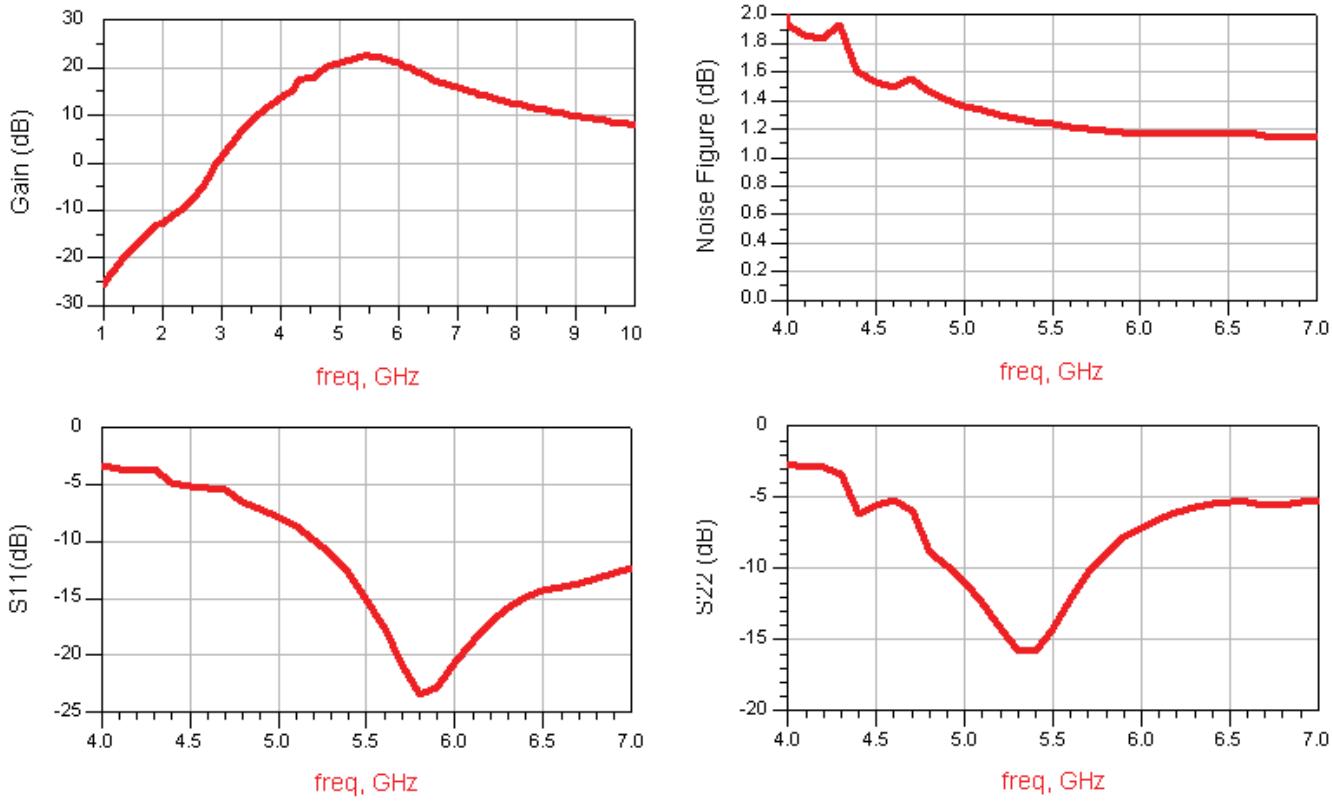


Figure 9. 5 GHz LNA simulation result with Momentum data

Figure 10 shows the die picture of the complete dual LNA.

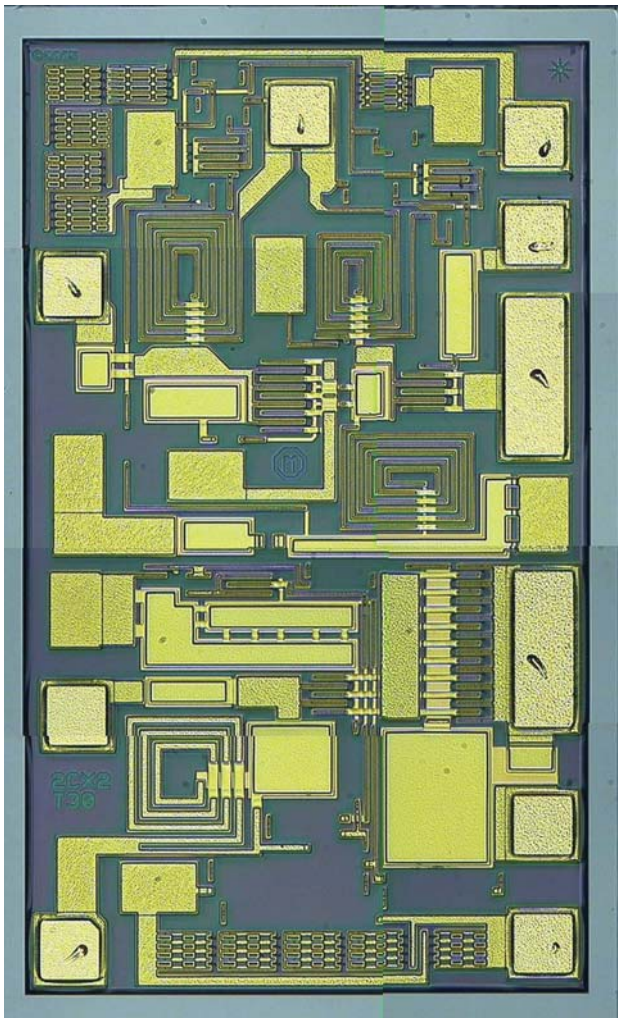


Figure 10. Fabricated die picture of the dual band LNA

The measured versus simulated results for both of the dual-band LNAs are shown in Figures 11 and 12. The discrepancies are a result of die-level and PCB ground interaction and effects of plastic molding compound over the chip. These serve to shift the frequency response curves and de-Q the circuit components, the effects of which are most pronounced in the S22 response and the high frequency gain curves. Despite these, the responses peak at the values that correspond to the WLAN frequency bands with outstanding noise and gain performance.

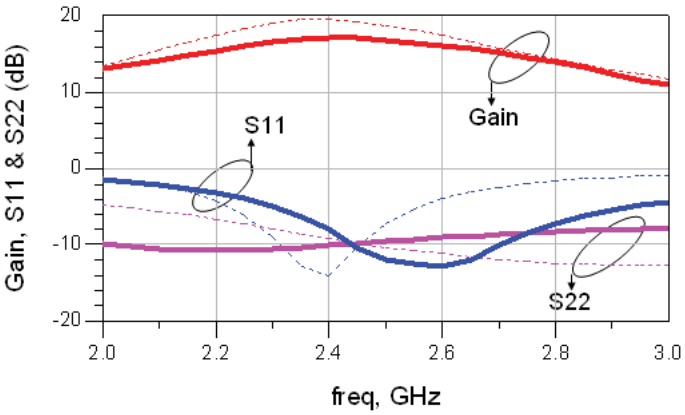
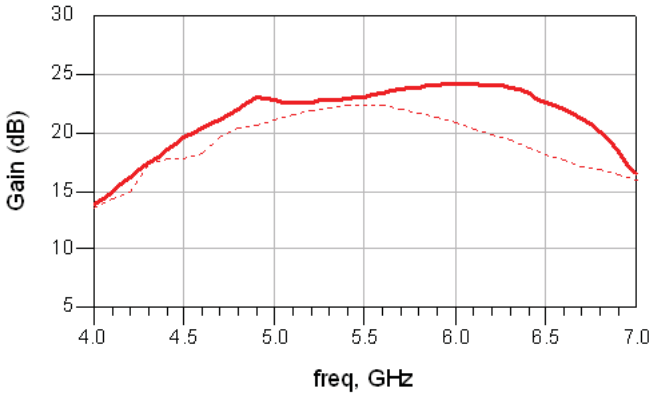


Figure 11. Measured (solid) vs. simulated (dotted) performance for 2.4 GHz LNA



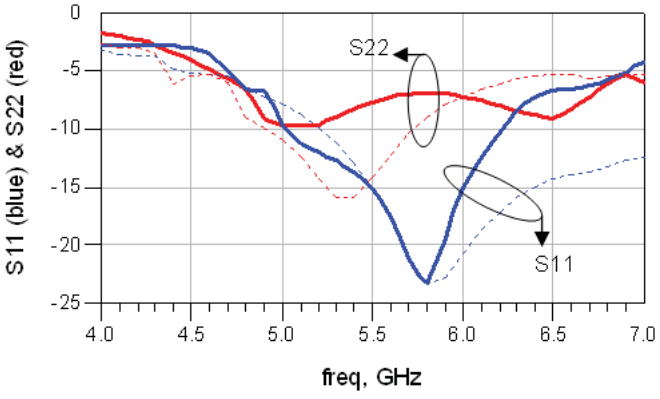


Figure 12. Measured (solid) vs. simulated (dotted) performance for 5-6 GHz LNA

Conclusions

The design and trade-offs in a dual-band WLAN LNA have been described. The article shows that E-M simulations, together with circuit level simulation tools, are indispensable for compact designs. In the 2.45 GHz band, gain is 17 dB at 14 mA current with 0.9 dB of noise figure. In the 5 GHz band, gain is 22-24 dB at 22 mA and noise figure is on average 1.5 dB. Input P1dB is –5.5 dBm for the 2.4 GHz LNA and typically –14 dBm for the 5 GHz LNA. IIP3 is +5.5 dBm for the 2.4 GHz LNA and typically –2 dBm for the 5 GHz band. The complete design uses only one RF input matching component external to the MMIC inside the module. The complete LNA is housed in a 3 mm x 3 mm molded chip-on-board package and requires only two external bypass capacitors in actual operation.

References

[1] A.O. Harm and K. Mouthaan and E. Aziz and M. Versleijen, "Modelling and Simulation of Hybrid RF Circuits Using a Versatile Compact Bondwire Model," Proceedings of the European Microwave Conference, pp. 529-534, Oct. 1998. Amsterdam.