

6N140A, HCPL-675x, 83024, HCPL-570x, HCPL-177K, 5962-89810, HCPL-573x, HCPL-673x, 5962-89785, 5962-98002

Hermetically Sealed, Low IF, Wide VCC, High Gain Optocouplers

Description

These units are single, dual, and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either commercial products or with full MIL-PRF-38534 Class H or Class K testing or from the appropriate DLA Standard Microcircuit Drawing (SMD). All devices are manufactured and tested on a MIL-PRF-38534 certified line, and Class H and Class K devices are included in the DLA Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each channel contains an GaAsP LED that is optically coupled to an integrated high-gain photon detector. The high gain output stage features an open collector output, providing both lower saturation voltage and higher signaling speed than possible with conventional photo-Darlington optocouplers. The shallow depth and small junctions offered by the IC process provides better radiation immunity than conventional phototransistor optocouplers.

The supply voltage can be operated as low as 2.0V without adversely affecting the parametric performance.

These devices have a 300% minimum CTR at an input current of only 0.5 mA, making them ideal for use in low-input current applications such as MOS, CMOS, low-power logic interfaces or line receivers. Compatibility with high-voltage CMOS logic systems is assured by specifying I_{CCH} and I_{OH} at 18 volts.

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both, that may be induced by ESD.

Features

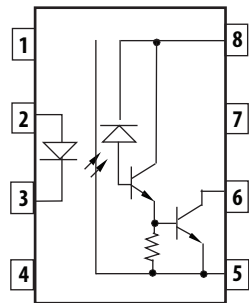
- Dual marked with device part number and DLA Standard Microcircuit Drawing (SMD)
- Manufactured and tested on a MIL-PRF-38534 certified line
- QML-38534, Class H and Class K
- Five hermetically sealed package configurations
- Performance guaranteed over -55°C to $+125^{\circ}\text{C}$
- Low input current requirement: 0.5 mA
- High current transfer ratio: 1500% typical at $I_F = 0.5\text{ mA}$
- Low output saturation voltage: 0.11V typical
- 1500 V_{dc} withstand test voltage
- High radiation immunity
- 6N138/9, HCPL-2730/31 function compatibility
- Reliability data available

Applications

- Military and aerospace
- High-reliability systems
- Microprocessor system interface
- Transportation, medical, and life critical systems
- Isolated input line receiver
- EIA RS-232-C line receiver
- Voltage level shifting
- Isolated input line receiver
- Isolated output line driver
- Logic ground isolation
- Harsh industrial environments
- Current loop receiver
- System test equipment isolation
- Process control input/output isolation

Functional Diagram

Multiple channel devices are available.



Package styles for these parts are 8-pin and 16-pin DIP through hole (case outlines P and E respectively), 16-pin DIP flat pack (case outline F), and leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options. See the [Selection Guide: Package Styles and Lead Configuration Options](#) table for details. Standard Microcircuit Drawing (SMD) parts are available for each package and lead style.

Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations and are as noted. Additionally, the same package assembly processes are used in all devices. These similarities give justification for the use of data obtained from one part to represent other part's performance for die related reliability and certain limited radiation test results.

Truth Table (Positive Logic)

Input	Output
On (H)	L
Off (L)	H

NOTE: A 0.1-μF bypass capacitor must be connected between V_{CC} and GND pins.

Functional Diagrams

8-Pin DIP	8-Pin DIP	16-Pin DIP	16-Pin Flat Pack	20-Pad LCCC
Through hole	Through hole	Through hole	Unformed leads	Surface mount
1 channel	2 channels	4 channels	4 channels	2 channels

NOTE: All DIP and flat pack devices have common V_{CC} and ground. LCCC (leadless ceramic chip carrier) package has isolated channels with separate V_{CC} and ground connections. All diagrams are top view.

Selection Guide: Package Styles and Lead Configuration Options

Package	16-Pin DIP	8-Pin DIP	8-Pin DIP	16-Pin Flat Pack	20-Pad LCCC
Lead Style	Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
Channels	4	1	2	4	2
Common Channel Wiring	V _{CC} , GND	None	V _{CC} , GND	V _{CC} , GND	None
Part Number and Options					
Commercial	6N140A	HCPL-5700	HCPL-5730	HCPL-6750	HCPL-6730
MIL-PRF-38534 Class H	6N140A/883B	HCPL-5701	HCPL-5731	HCPL-6751	HCPL-6731
MIL-PRF-38534 Class K	HCPL-177K	HCPL-570K	HCPL-573K	HCPL-675K	HCPL-673K
Standard Lead Finish	Gold Plate ^a	Gold Plate ^a	Gold Plate ^a	Gold Plate ^a	Solder Pads ^b
Solder Dipped ^b	Option #200	Option #200	Option #200	—	—
Standard Lead Finish in Tape and Reel Packaging ^{b, c}	—	—	—	—	Option -500
Butt Cut/Gold Plate ^a	Option #100	Option #100	Option #100	—	—
Gull Wing/Soldered ^b	Option #300	Option #300	Option #300	—	—
Crew Cut/Gold Plate ^a	Option #600	Option #600	Option #600	—	—
Class H SMD Part Number					
Gold Plate ^a	8302401EC	5962-8981001PC	5962-8978501PC	8302401FC	—
Solder Dipped ^b	8302401EA	5962-8981001PA	5962-8978501PA	—	5962-89785022A
Butt Cut/Gold Plate ^a	8302401YC	5962-8981001YC	5962-8978501YC	—	—
Butt Cut/Soldered ^b	8302401YA	5962-8981001YA	5962-8978501YA	—	—
Gull Wing/Soldered ^b	8302401XA	5962-8981001XA	5962-8978501ZA	—	—
Crew Cut/Gold Plate ^a	8302401ZC	—	—	—	—
Crew Cut/Soldered ^b	8302401ZA	—	—	—	—
Class K SMD Part Number					
Gold Plate ^a	5962-9800201KEC	5962-8981002KPC	5962-8978503KPC	5962-9800201KFC	—
Solder Dipped ^b	5962-9800201KEA	5962-8981002KPA	5962-8978503KPA	—	5962-8978504K2A
Butt Cut/Gold Plate ^a	5962-9800201KYC	5962-8981002KYC	5962-8978503KYC	—	—
Butt Cut/Soldered ^b	5962-9800201KYA	5962-8981002KYA	5962-8978503KYA	—	—
Gull Wing/Soldered ^b	5962-9800201KXA	5962-8981002KXA	5962-8978503KZA	—	—
Crew Cut/Gold Plate ^a	5962-9800201KZC	—	—	—	—
Crew Cut/Soldered ^b	5962-9800201KZA	—	—	—	—

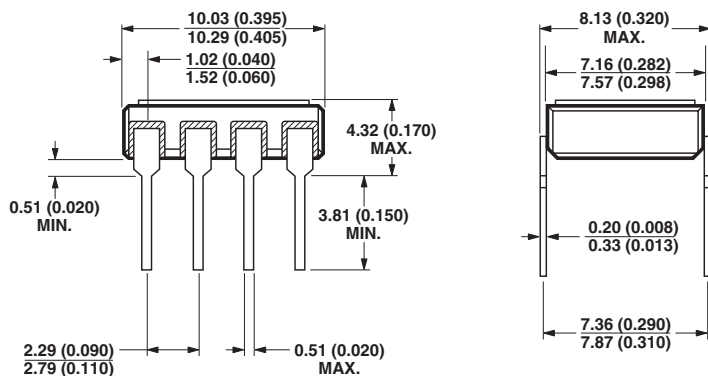
a. Gold Plate lead finish: Maximum gold thickness of leads is <100 µin. Typical is 60 µin to 90 µin.

b. Solder lead finish: Sn63/Pb37.

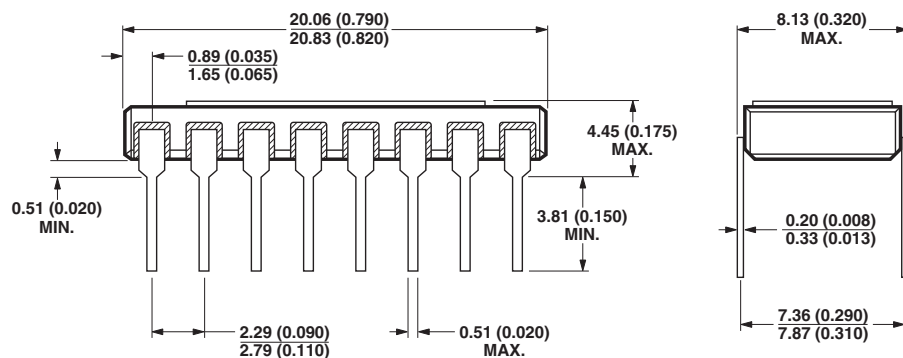
c. Standard packing quantity (SPQ) is 250 units per reel. For more details on option -500, refer to [AV02-0145EN](#).

Outline Drawings

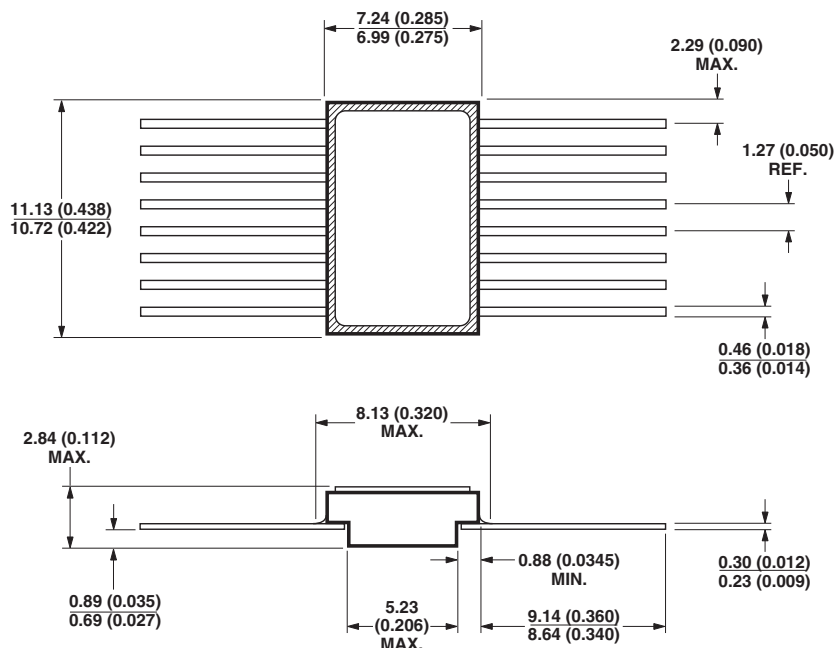
8-Pin DIP Through Hole, 1 and 2 Channel



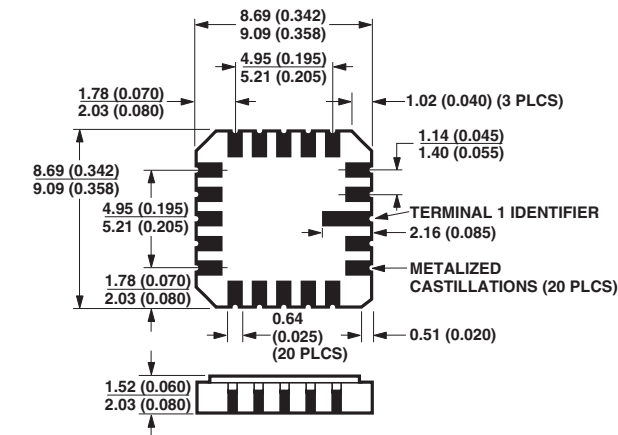
16-Pin DIP Through Hole, 4 Channels



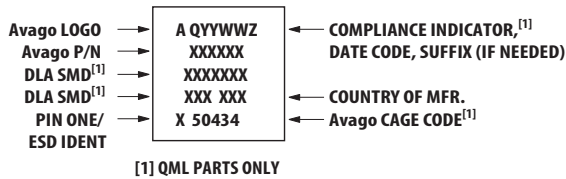
16-Pin Flat Pack, 4 Channels



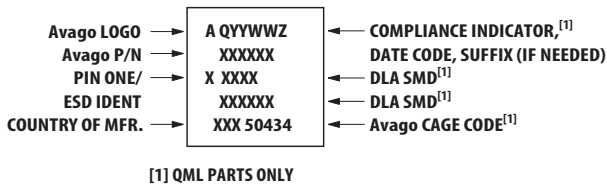
20-Terminal LCCC Surface Mount, 2 Channels



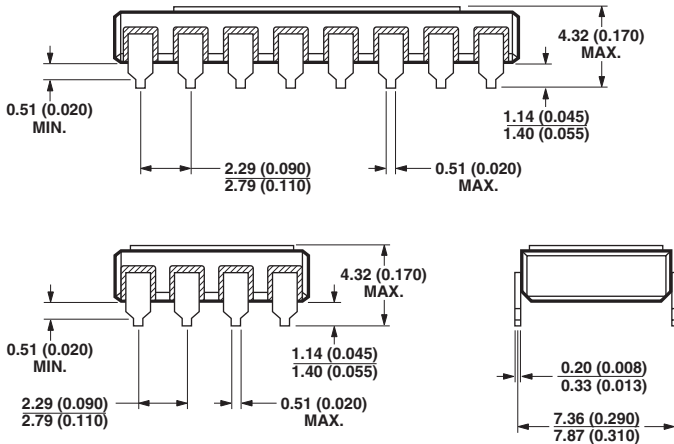
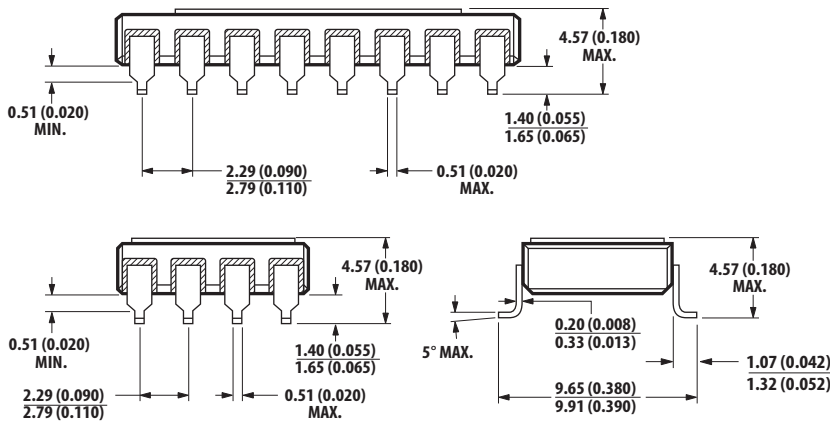
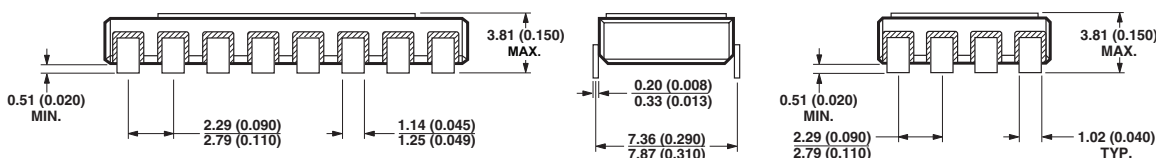
Leaded Device Marking



Leadless Device Marking



Hermetic Optocoupler Options

Option	Description
100	Surface-mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on Commercial, Class H, and Class K products in 8-pin and 16-pin DIP.  Top view dimensions: 0.51 (0.020) MIN. lead width, 2.29 (0.090) / 2.79 (0.110) pin pitch, 0.51 (0.020) MAX. lead width, 4.32 (0.170) MAX. package width, 1.14 (0.045) / 1.40 (0.055) pin height. Side view dimensions: 0.51 (0.020) MIN. lead width, 2.29 (0.090) / 2.79 (0.110) pin pitch, 4.32 (0.170) MAX. package height, 1.14 (0.045) / 1.40 (0.055) pin height. End view dimensions: 0.20 (0.008) / 0.33 (0.013) lead thickness, 7.36 (0.290) / 7.87 (0.310) package length.
200	Lead finish is solder dipped rather than gold plated. This option is available on Commercial, Class H, and Class K products in 8-pin and 16-pin DIP. DLA drawing (SMD) part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder-dipped terminals as a standard feature.
300	Surface-mountable hermetic optocoupler with leads cut and bent for gull-wing assembly. This option is available on Commercial, Class H, and Class K products in 8-pin and 16-pin DIP. This option has solder-dipped leads.  Top view dimensions: 0.51 (0.020) MIN. lead width, 2.29 (0.090) / 2.79 (0.110) pin pitch, 0.51 (0.020) MAX. lead width, 4.57 (0.180) MAX. package width, 1.40 (0.055) / 1.65 (0.065) pin height. Side view dimensions: 0.51 (0.020) MIN. lead width, 2.29 (0.090) / 2.79 (0.110) pin pitch, 4.57 (0.180) MAX. package height, 1.40 (0.055) / 1.65 (0.065) pin height. End view dimensions: 0.20 (0.008) / 0.33 (0.013) lead thickness, 9.65 (0.380) / 9.91 (0.390) package length, 1.07 (0.042) / 1.32 (0.052) lead length, 5° MAX. lead angle.
600	Surface-mountable hermetic optocoupler with leads trimmed for butt-joint assembly. This option is available on Commercial, Class H, and Class K product in 8-pin and 16-pin DIP. Contact Broadcom for the availability of this option on DLA part types.  Top view dimensions: 0.51 (0.020) MIN. lead width, 2.29 (0.090) / 2.79 (0.110) pin pitch, 1.14 (0.045) / 1.25 (0.049) pin height, 3.81 (0.150) MAX. package width. Side view dimensions: 0.20 (0.008) / 0.33 (0.013) lead thickness, 7.36 (0.290) / 7.87 (0.310) package length. End view dimensions: 0.51 (0.020) MIN. lead width, 2.29 (0.090) / 2.79 (0.110) pin pitch, 1.02 (0.040) TYP. lead width, 3.81 (0.150) MAX. package width.

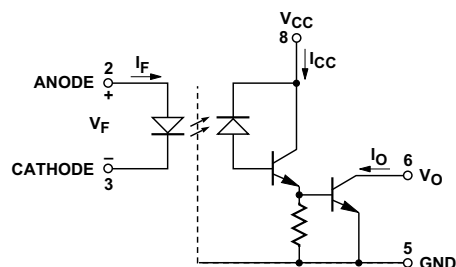
NOTE: Note: Dimensions are in millimeters (inches).

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-65	+150	°C	
Operating Temperature	T_A	-55	+125	°C	
Junction Temperature	T_J	—	+175	°C	
Case Temperature	T_C	—	+170	°C	
Lead Solder Temperature	—	—	260 for 10 seconds	°C	
Output Current, Each Channel	I_O	—	40	mA	
Output Voltage, Each Channel	V_O	-0.5	20	V	a
Supply Voltage	V_{CC}	-0.5	20	V	a
Output Power Dissipation, Each Channel	—	—	50	mW	b
Peak Input Current, Each Channel, <1-ms Duration	—	—	20	mA	
Average Input Current, Each Channel	I_F	—	10	mA	c
Reverse Input Voltage, Each Channel	V_R	—	5	V	
Package Power Dissipation, Each Channel	P_D	—	200	mW	

- GND pin should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0V, provides the lowest total I_{OH} over temperature.
- Output power is collector output power plus total supply power for the single-channel device. For the dual-channel device, output power is collector output power plus one half the total supply power. For the quad-channel device, output power is collector output power plus one fourth of total supply power. Derate at 1.66 mW/°C above 110°C.
- Derate I_F at 0.33 mA/°C above 110°C.

8-Pin Ceramic DIP Single Channel Schematic



ESD Classification

MIL-STD-883, Method 3015: HCPL-5700/01/0K and 6730/31/3K	▲▲, Class 2
MIL-STD-883, Method 3015: 6N140A, 6N140A/883B, HCPL-177K, HCPL-6750/51/5K and HCPL-5730/31/3K	●, Class 3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	2.0	18	V
Input Current, High Level, Each Channel	$I_{F(ON)}$	0.5	5	mA
Input Voltage, Low Level, Each Channel	$V_{F(OFF)}$	—	0.8	V
Output Voltage	V_O	2.0	18	V

Electrical Characteristics

$T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, unless otherwise specified.

Parameter		Symbol	Group A ^a Subgroups	Test Conditions	Limits			Unit	Fig.	Notes						
					Min.	Typ. ^b	Max.									
Current Transfer Ratio		CTR	1, 2, 3	I _F = 0.5 mA, V _O = 0.4V, V _{CC} = 4.5V	300	1500	—	%	3	c, d						
				I _F = 1.6 mA, V _O = 0.4V, V _{CC} = 4.5 V	300	1000	—									
				I _F =5 mA, V _O = 0.4V, V _{CC} = 4.5V	200	500	—									
Logic Low Output Voltage		V _{OL}	1, 2, 3	I _F = 0.5 mA, I _{OL} = 1.5 mA, V _{CC} = 4.5V	—	0.11	0.4	V	2	c						
				I _F = 1.6 mA, I _{OL} = 4.8 mA, V _{CC} = 4.5V	—	0.13	0.4			c, e						
				I _F =5 mA, I _{OL} = 10 mA, V _{CC} = 4.5V	—	0.16	0.4			c						
Logic High Output Current		I _{OH}	1, 2, 3	I _F =2 μA, V _O = 18V, V _{CC} = 18V	—	0.001	250	μA		c						
		I _{OHX}					250			μA	c, f					
Logic Low Supply Current	Single Channel and LCCC	I _{CCL}	1, 2, 3	I _F = 1.6 mA, V _{CC} = 18V	—	1.0	2	mA		g						
	Dual Channel										I _{F1} = I _{F2} = 1.6 mA, V _{CC} = 18V	—	1.0	4	4	
	Quad Channel										I _{F1} = I _{F2} = I _{F3} = I _{F4} = 1.6 mA, V _{CC} = 18V	—	1.7	4		
Logic High Supply Current	Single Channel and LCCC	I _{CCH}	1, 2, 3	I _F = 0 mA, V _{CC} = 18V	—	0.001	20	μA		g						
	Dual Channel						I _{F1} = I _{F2} = 0 mA, V _{CC} = 18V				—	40				
	Quad Channel						I _{F1} = I _{F2} = I _{F3} = I _{F4} = 0 mA, V _{CC} = 18V				—	40				
Input Forward Voltage	Single and Dual Channel	V _F	1	I _F = 1.6 mA	1.0	1.4	1.7	V	1	c						
			2		—	—	1.7									
			3		—	—	1.8									
	LCCC		1, 2, 3		1.0	1.4	1.8									
	Quad Channel		1, 2		—	1.4	1.7									
			3		—	—	1.8									
Input Reverse Breakdown Voltage		B _{VR}	1, 2, 3	I _R = 10 μA	5	—	—	V		c						
Input-Output Insulation Leakage Current		I _{I-O}	1	≤65% RH, T _A = 25°C, t = 5 seconds, V _{I-O} = 1500 VDC	—	—	1.0	μA		h, i						
Capacitance Between Input-Output		C _{I-O}	4	f = 1 MHz, T _A = 25°C	—	—	4	pF		c, j, k, l						

Parameter	Symbol	Group A ^a Subgroups	Test Conditions	Limits			Unit	Fig.	Notes
				Min.	Typ. ^b	Max.			
Propagation Delay Time to Logic Low at Output	t_{PHL}	9, 10, 11	$I_F = 0.5 \text{ mA}$, $R_L = 4.7 \text{ k}\Omega$, $V_{CC} = 5\text{V}$	—	30	100	μs	5, 6, 7, 8	c
		9, 10, 11	$I_F = 1.6 \text{ mA}$, $R_L = 1.5 \text{ k}\Omega$, $V_{CC} = 5\text{V}$	—	5	30			c, e
		9	$I_F = 5 \text{ mA}$, $R_L = 680\Omega$, $V_{CC} = 5\text{V}$	—	2	5			c, l
		10, 11				10			
		9, 10, 11				10			c, e
Propagation Delay Time to Logic High at Output	t_{PLH}	9, 10, 11	$I_F = 0.5 \text{ mA}$, $R_L = 4.7 \text{ k}\Omega$, $V_{CC} = 5\text{V}$	—	17	60	μs	5, 6, 7, 8	c
		9, 10, 11	$I_F = 1.6 \text{ mA}$, $R_L = 1.5 \text{ k}\Omega$, $V_{CC} = 5\text{V}$	—	14	50			c, e
		9	$I_F = 5 \text{ mA}$, $R_L = 680\Omega$, $V_{CC} = 5\text{V}$	—	8	20			c, l
		10, 11				30			
		9, 10, 11				30			c, e
Common Mode Transient Immunity at Low Output Level	$ CM_L $	9, 10, 11	$V_{CC} = 5\text{V}$, $I_F = 1.6 \text{ mA}$ $R_L = 1.5 \text{ k}\Omega$, $ V_{CM} = 25 V_{P-P}^l$ $ V_{CM} = 50 V_{P-P}^e$	500	1000		$\text{V}/\mu\text{s}$	9	c, m, n, o
Common Mode Transient Immunity at High Output Level	$ CM_H $	9, 10, 11	$V_{CC} = 5\text{V}$, $I_F = 0 \text{ mA}$ $R_L = 1.5 \text{ k}\Omega$, $ V_{CM} = 25 V_{P-P}^l$ $ V_{CM} = 50 V_{P-P}^e$	500	1000		$\text{V}/\mu\text{s}$	9	c, m, n, o

- Commercial parts receive 100% testing at 25°C (subgroups 1 and 9). SMD, Class H and Class K parts receive 100% testing at 25, 125, and –55°C (subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Each channel.
- Current transfer ratio is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F , $\times 100\%$.
- Not required for 6N140A, 6N140A/883B, HCPL-177K, HCPL-6750/51/5K, 8302401, and 5962-9800201 types.
- I_{OHX} is the leakage current resulting from channel-to-channel optical crosstalk. $I_F = 2 \mu\text{A}$ for channel under test. For all other channels, $I_F = 10 \text{ mA}$.
- The HCPL-6730, HCPL-6731, and HCPL-673K dual-channel parts function as two independent single channel units. Use the single-channel parameter limits.
- All devices are considered two-terminal devices; measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
- This is a momentary withstand test, not an operating condition.
- Measured between each input pair shorted together and all output connections for that channel shorted together.
- Parameters tested as part of device initial characterization and after design and process changes. Parameters guaranteed to limits specified for all lots not specifically tested.
- Required for 6N140A, 6N140A/883B, HCPL-177K, HCPL-6750/51/5K, 8302401, and 5962-9800201 types.
- CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8\text{V}$).
 CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0\text{V}$).

- n. In applications where dV/dt may exceed 50,000 V/ μ s (such as a static discharge), a series resistor, R_{CC} , should be included to protect the detector ICs from destructively high surge currents. The recommended value is:

For single channel:

$$R_{CC} = \frac{1 \text{ (V)}}{0.15 I_F \text{ (mA)}} \text{ k}\Omega$$

For dual channel:

$$R_{CC} = \frac{1 \text{ (V)}}{0.3 I_F \text{ (mA)}} \text{ k}\Omega$$

For quad channel:

$$R_{CC} = \frac{1 \text{ (V)}}{0.6 I_F \text{ (mA)}} \text{ k}\Omega$$

- o. Parameters tested as part of device initial characterization and after design and process changes. Parameters guaranteed to limits specified for all lots not specifically tested.

Typical Characteristics

All typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$.

Parameter	Symbol	Test Conditions	Typ.	Units	Note
Input Capacitance	C_{IN}	$V_F = 0\text{V}$, $f = 1 \text{ MHz}$	60	pF	a
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$	$I_F = 1.6 \text{ mA}$	-1.8	mV/ $^\circ\text{C}$	a
Resistance (Input-Output)	R_{I-O}	$V_{I-O} = 500\text{V}$	10^{12}	Ω	a, b
Capacitance (Input-Output)	C_{I-O}	$f = 1 \text{ MHz}$	2.0	pF	a, b
Dual-Channel and Quad-Channel Products Only					
Input-Input Insulation Leakage Current	I_{I-I}	$RH \leq 65\%$, $V_{I-I} = 500\text{V}$, $t = 5 \text{ seconds}$	0.5	nA	c
Resistance (Input-Input)	R_{I-I}	$V_{I-I} = 500\text{V}$	10^{12}	Ω	c
Capacitance (Input-Input)	C_{I-I}	$f = 1 \text{ MHz}$	1.0	pF	c

- a. Each channel.
b. Measured between each input pair shorted together and all output connections for that channel shorted together.
c. Measured between adjacent input pairs shorted together for each multichannel device.

Figure 1: Input Diode Forward Current vs. Forward Voltage

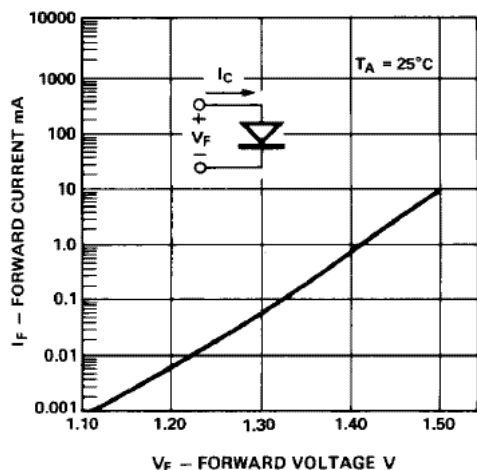


Figure 2: Normalized DC Transfer Characteristics

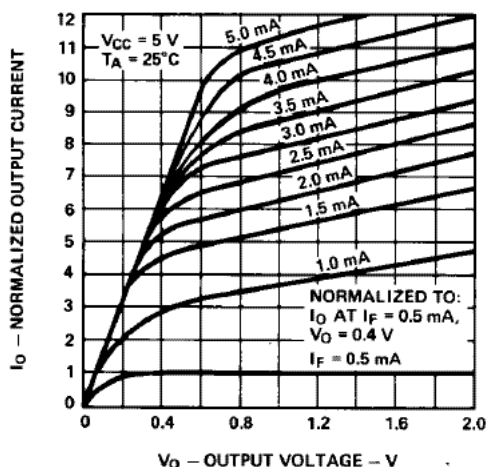


Figure 3: Normalized Current Transfer Ratio vs. Input Diode Forward Current

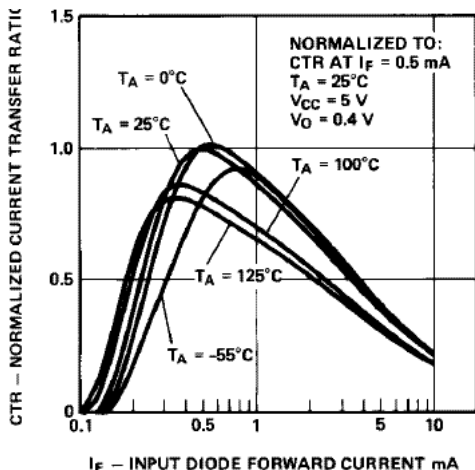


Figure 4: Normalized Supply Current vs. Input Diode Forward Current

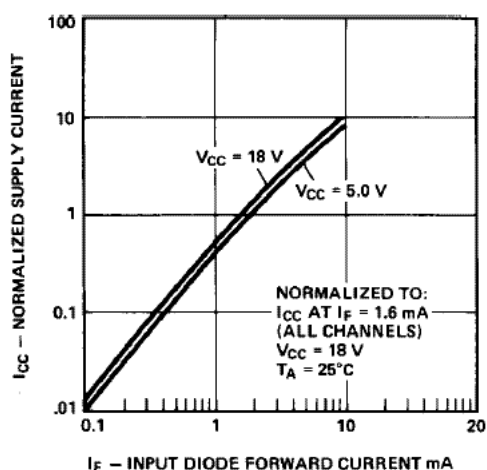


Figure 5: Propagation Delay to Logic Low vs. Input Pulse Period

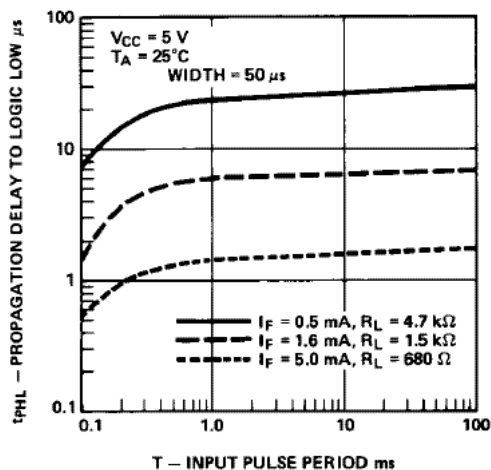


Figure 6: Propagation Delay vs. Temperature

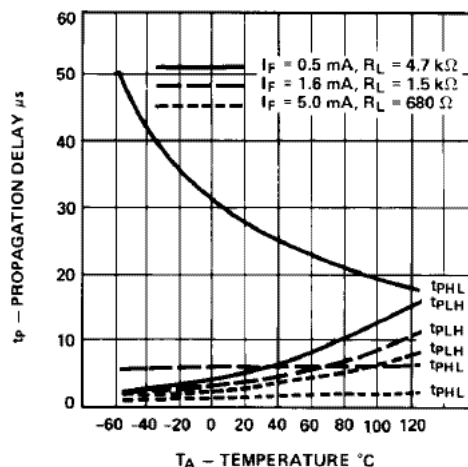


Figure 7: Propagation Delay vs. Input Diode Forward Current

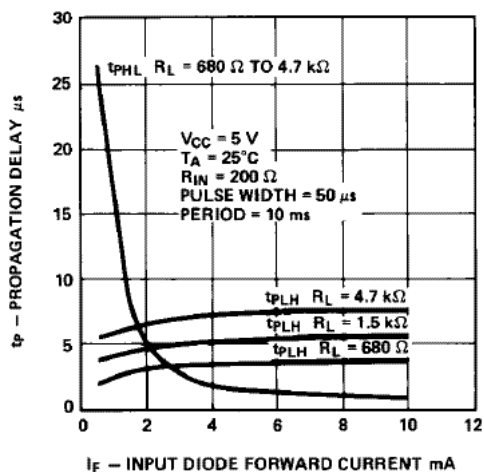
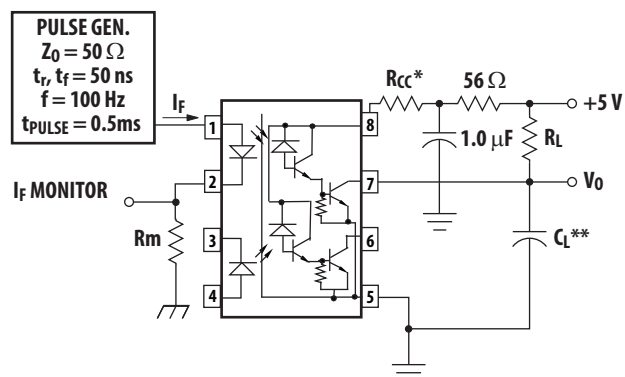


Figure 8: Switching Test Circuit



* See note n on page 10.

** C_1 includes probe and stray wiring capacitance.

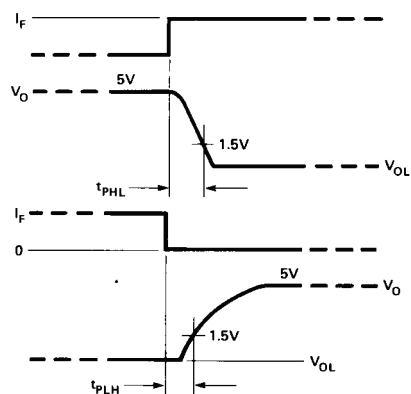
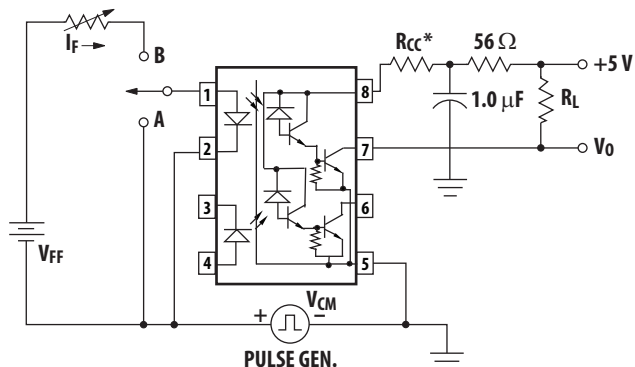
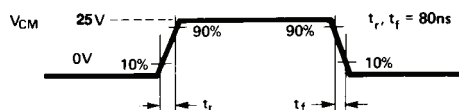


Figure 9: Test Circuit for Transient Immunity and Typical Waveforms



* See note n on page 10.



V_O 5V
SWITCH AT A: $I_F = 0 mA$

V_O V_{OL}
SWITCH AT B: $I_F = 1.6 mA$

Figure 10: Recommended Drive Circuitry Using TTL Open-Collector Logic

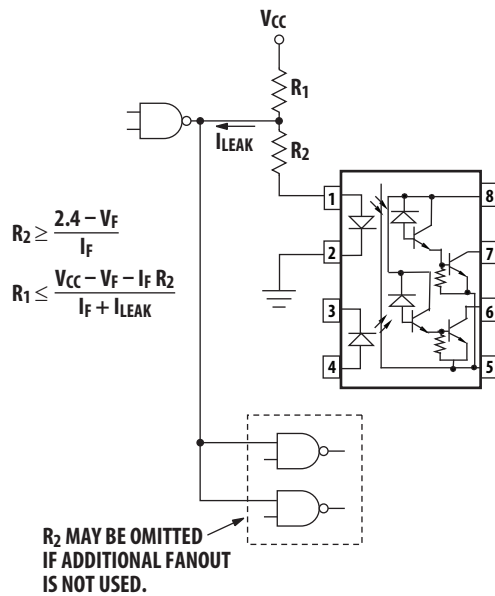
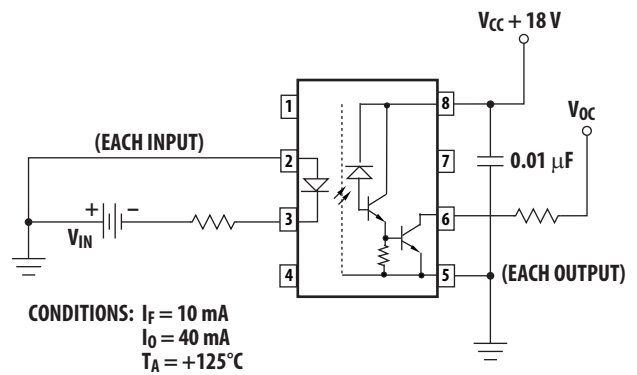


Figure 11: Operating Circuit for Burn-In and Steady State Life Tests



* ALL CHANNELS TESTED SIMULTANEOUSLY.

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